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A Comparative Study on Adders

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Abstract - In a digital circuit design adders are the most common elements used as addition is the fundamental operation in a system. For arithmetic algorithms in computers, adders play a key role .Thus the selection of appropriate adder with appropriate properties is very essential for the efficient working of the circuit. In this paper a relative study of different adders has been made based on its architectural features, technologies, and efficiency. Different adders are compared such as (RCA) Ripple Carry Adder, Carry Look- Ahead Adder, Carry Skip Adders using mainly CMOS and pass transistors.

Key Words: —(RCA) Ripple Carry Adder, (CLA) Carry Look-Ahead Adder, (CSKA)Carry Skip Adder, CMOS Transistor,(PTL) Pass Transistor Logic ,(EDP)Energy Delay Product .

1. INTRODUCTION

The addition of binary numbers logically, in various methods for memory circuit address calculation , increment and decrement operations are performed by digital circuits that is adders. It reduces the circuit complexity. Full adder is a digital circuit that adds three binary numbers, out of which one of them is input carry and output sum and output carry. They are used in ALU in processor chip to perform arithmetic and logical operations. It is considered as pliant and has become a requisite of most of the cognitive programs.

Using adders in digital circuits significantly reduces the usage of excess number of transistors in the circuit. It plays a vital role in increasing the speed, reducing power dissipation and area consumption. Some of the traditional adders like RCA, CLA, CSKA, etc. The main necessities of any digital circuit are:

- Power consumption is low
- Power dissipation is low
- Area is low
- Higher speed [1]

The most difficult part in the design of an adder is to increase the speed and to reduce the power and area. The comparative study between several adders is resulting to the fact that the CSKA is more efficient and the pass transistor logic circuits have a lesser delay and area.

2. Fundamental adders

2.1 Ripple Carry Adder

RCA consists of a series of full adders which add N-bit numbers where each of the adder takes the inputs as C_{in}, which is obtained from the C_{out} of the previous adder. Since each have carry bit, it ripples to the next full adder hence it is called as ripple carry adder. The RCA has lower consumption of area, higher period of time delay and also more consumption of power when compared with other adders. Looking at block diagram its very evident that the addition is performed using series of full adders where the carry output of previous adder is the carry output bit of the very next adder.

Equation: $S = A \text{ xor } B \text{ xor} C_{in}$

$$C_{out} = AB + BC_{in} + AC_{in}$$

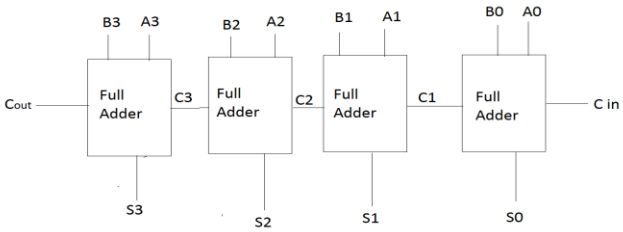

Fig -1: (RCA) Ripple Carry Adder

2.2 Carry Look Ahead Adder (CLA)

The speed of computation is made faster using a CLA. They work by creating two output signals (P & G) on each position of bit. G is the carry output of the adder where as P is the sum output of a half adder.

As the generate and propagate are calculated previously, we get a faster computation of the addition in CLA thus increasing the speed [2].The circuit diagram and equations of a CLA is given as follows.

The Equations of a CLA is given as follows:

$$P(i) = A(i) \text{ xor } B(i)$$

$$G(i) = A(i) \text{ and } B(i)$$

1.	Ripple Carry Adder	04	8.959
2.	Carry Look - Ahead Adder	04	8.920
3.	Carry Skip Adder	06	8.256

Table -1: COMPARISON OF ADDERS

S(i) = P(i) xor C (i)

C(i) = G(i-1) or (P(i-1) and C(i-1))

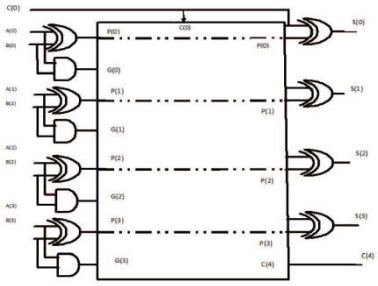

Fig -2: Carry Look - Ahead Adder (CLA)

2.3 Carry Skip Adder

The delay of RCA can be reduced with little effort by implementing carry skip adder than other adders. Here carry output of a block of N bits is the carry input of the next block. Here CSKA implements the skip logic for propagating carry which includes RCA with a faster carry chain [2]. The circuit diagram of a CSKA is as given in Fig.3

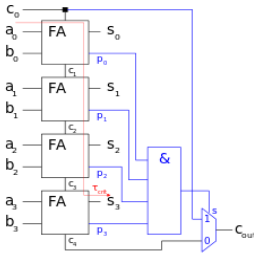

Fig -3: 4-Bit Carry Skip Adder

A and B are the two operands that are used. The first RCA is given with first two bits and the second RCA is given with the next two bits. The carry $C_{in}$is first initialized as '0' and given to first RCA .The outputs of first RCA are considered as the first two bits of the sum and the output carry is sent to the next RCA, which generates the next

3. Adders at different design logic

3.1 Static CMOS logic

Static CMOS is a logic circuit design technique where the output is always strongly driven as it is always being connected to either VCC or GND. The pull up network and the pull down network [3] control the logic. The p channel MOSFET devices are in pull up network whereas the channel MOSFET devices are in pull down network. The circuit is designed in such a way that the pull up and the pull down networks are 'ON' one after the other. Hence it ensures that the computation time is more than the pass transistor logic and there is no static power consumption.

3.2 Pass Transistor logic

It reduces the count of transistors by eliminating redundant transistors and hence they are used in the design of integrated circuits. Transistors are used as switches which pass logic levels between nodes of a circuit and thus reduce the number of active devices. At its output each transistor in series, is very low saturated. It is required to recover the signal voltage to the maximum value for conventionally constructed gate [3] , if these devices are used as a chain in series in a logic path . Pass transistor logic and the gate is shown in Fig.4.***B***

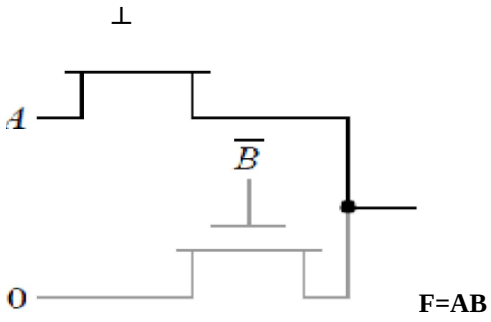

Fig -4 PTL logic and gate

4. Literature survey

BhavaniKoyadaet.al (2017)[1] , in their paper has compared different adders to know the difference in operation and performance using Xilinx tool and concluded that Carry Skip Adder consumes less area and the speed of operation is 10.985ns which is greater when compared to other adders .

SujanSarkar et.al (2017)[2],in this paper have doneComparative study of various parallel adders to improve the delay.CSA and CSKA have been designed to improve delay and have concluded that CSKA has delay performance better than CSA.

In multi input operations CSA can perform well.

Pournima Pankaj Patil et.al (2016)[3],in their paper they have compared performance parameters such as delay and average power to conclude that PTL technique is better and PDP of PTL technique is better than CMOS techniques with 10% of variation in gate length.

AlianGuyotet.al (1987)[4],in their paper have obtained the efficient Carry-Skip Adders which reduces the optimization problem and came to conclusion that the Carry-Skip Adder has lesser propagation time but has involve larger silicon area for circuit design compared to Carry-look Adder and Ripple carry Adder

.VititKantabutraet.al(1993)[5],in their paper the main objective isto design one-level carry-skip adders which allows the use of realistic component delay figures obtained by simulation.

Antonio G. M. Strolloet.al (1997)[6], the main objective of the paper is to compare two-level Carry-Skip Adder using CPL and CMOS logic and concluded that the Carry Skip Adder using CMOS technology provides 80% performance degradation w.r.t. The CPL implementation.

Amit Jainet.al (2010)[7], the objectiveof their paper is to ensure low power dissipation in VLSI chips andto improve the density of integration and haveconcluded that the Combination of both field effect transistor and single electron transistor results in hybrid SET-MOS pass transistor universal gates to improve the flexibilityfor operationfor a range of temperature .

Sujata S. Chiwande et.al (2012)[8],in their paperused Carry Skip Adder block to design reversible logic gates used for reversible operation and concluded that four bit CSKAusing Fredkin gate &TSG gate are better compared to 4-bit CSKA interms of a low power circuits that is reversible.

Yu Pang et.al (2012)[9], have designed a CSKA of a 16 bitusing an optimization of RCA andconcluded that the CSKA has advantages of 90.3ns of short delay but the area occupied is more compared to RCA.

Weng-Geng Hoet.al (2013)[10],in their paper have simplified and optimized the NMOS pass transistors to reduce the circuit area overhead and concluded that the design has reduced number of transistor count to 16% , hence the number of transistor switching is also reduced .Based on simulation the delay is reduced by 31%.

Anjali Arora et.al (2017)[11],in this paper the carry skip adder stages that are fixed stage and variable stage has beenanalyzed to obtain a new CSKA of 16-bit with high speed variable stage and concluded that power consumption and delay in the mentioned adder is reduced by 61.75% and 8% respectively with no increase in circuit complexity but more area is consumed as compared to conventional adders.

Karthik.Det.al (2016)[12],the objective is using And-Or-Inverter and OR-And-Inverter to improve the performance and efficiency of traditional Carry Skip Adder and thusthe design willsignificantly reduce the power and increases the speed by 36% and 40% respectively.

Y.Berg(2015)[13], the objective is to obtainultra low-voltage and high-speed serial adders using pass transistors and concluded that compared to standard CMOS transistor logic the delay can be reduced to less than 6% .

K.Kumaran et.al (2017)[14],the objective is to use MUX based full adder to minimize the area andreduce the propagation time of Carry Skip Adder to conclude that the Carry Skip Adder using MBFA requires less transistors and thereby the area required will be less. The delay is also reduced to 10.43ns when compared to CMOS FpgA.

SreehariVeeramachaneni et.al (2015)[16], the objective of the paper is to designan efficient adder that helps in design of floating point units by having design methodology for 2's complement block is and concluded that the design has 13.6% delay and around 6.3% improved power-delay product.

Rakesh Daset.al (2016)[17],the objective is Optical implementation of functionally reversible CSA circuit and concluded that comparing with existing optical adder circuits it clearly shows that both the designs are cost and delay efficient compared to the existing designs.

Ashish Kumaret.al (2017)[19], in their paper the objective is to compare and verify the different adder cells on different supply voltages at 100MHz operatingfrequency, according to there sults obtained by the simulation it is observed that the proposed designs will result with the maximum saving power of 93.4% with maximum reduction in delay 76.76%.

Vishal bharat R Hakki et.al (2017)[20], the objective is to analyse and compare the performance of carry skip adder using NMOS pass transistor logic configuration with respect to power dissipation , transistor count and delay , in this implementation there is reduction in number of transistor count, power dissipation and delay by 35.2%, 9.87% and 60% respectively when compared to CMOS logic.

5. Conclusion

In this paper it is evident that the comparison drawn is that the fundamental adders like Carry Skip Adder is more efficient when compared to Carry Look Ahead and Carry Skip Adders in terms of the time required for computation and the area required for the design. By comparing with the design logic used it is observed that the pass transistor logic requires lesser power than the CMOS logic. Also in PTL technique EDP is stable and good but the PTL technique will have more delay than CMOS logic.

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