A Novel Boost Converter for Plug-In HEV Charging By Current Sensing Techniques

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***Abstract*— This paper proposed an AC-DC semi-bridgeless boost Power Factor Corrected (PFC) converter with 180 degree phase shift and less number of switches. The simplified current sensing technique is applied in the converter to predict the inductor current by current synthesizing technique. The proposed converter has the advantageous features such as high efficiency at light loads and low ac input lines; minimize the charger size, charging time, and less amount and cost of electricity drawn. This project presented simulation results of a boost converter, converting the 230V ac input voltage to 400 V dc at 1kW to 3kW Load. The power factor of the proposed system is 0.9 and the THD level is below 5%. This type of converters is used for vehicle charging and residential charging application.With solar source the semi bridgeless converter can act as the dc-dc boost converter.**

***Index Terms*—AC–DC converter, boost converter, DC-DC converter, Bridgeless power factor correction (PFC), current sensing, plug in charger.**

I.INTRODUCTION

A storage system that can be recharged by connecting a plug to an external electric power source. The charging AC outlet predictably needs a plug in AC/DC charger with a power factor correction [1]. [2]. For the PFC application a multiple of circuit topologies and control methods have been developed.

The single-phase active PFC techniques can be classified into two approaches: they are single-stage approach and the two-stage approach. The single-stage approach is right for low power level applications. It can only applicable for lead acid batteries charging because of frequency ripple problem. Therefore, the two-stage approach is the suitable for high storage battery chargers used for high power applications, where the power rating is relatively high, and lithium-ion batteries [3] are used as the main energy storage system.

In the two-stage architecture, the first stage is PFC rectification where it rectifies the input ac voltage and transfers it to a dc-link. At the same time, the PFC is also achieved [4]. A phase shifted semi bridgeless PFC topology operated under continuous conduction mode as the two stage charger specifically with the ac–dc PFC converter and dc-dc converter for battery charging with various duty cycles.

A .Interleaved PFC boost topology

This boost topology uses two boost converters in parallel operating 180° out of phase [5]–[7] by switching 180° out of phase, it doubles the effective switching frequency and introduces a smaller input current ripple; thus, the input electromagnetic interference (EMI) filter can be smaller than a single PFC boost topology [8]–[10].

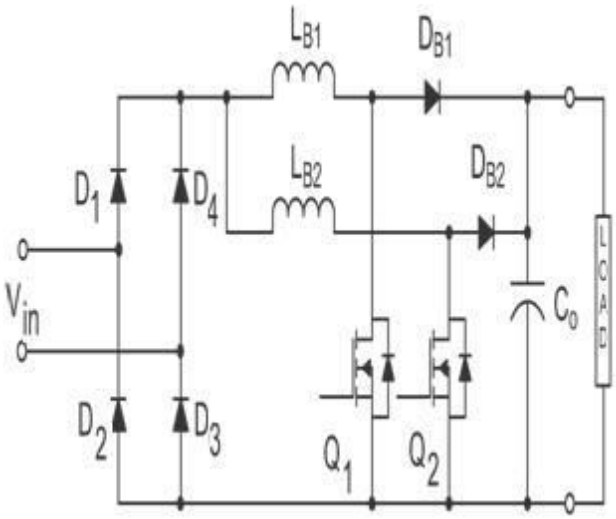


Fig .1.Interleaved topology

The drawback of this topology is the very high loss and the resultant heat management issue for the input diode bridge rectifiers. Fig. 1 shows the circuit diagram of interleaved topology.

B. Bridgeless PFC boost topology

This bridgeless boost topology avoids the need for the rectifier input bridge but maintains the classic boost topology [11]–[21]. The bridgeless boost converter, which is also called as the dual- boost PFC converter, which overcomes the problem of heat management in the input rectifier diode bridge, but it introduces increased EMI [22]–[24].

The common-mode(CM) noise generated by bridgeless PFC is much higher than the conventional boost PFC topology [24]. Drawback of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low-frequency transformer or an optical coupler.Fig2. represents the circuit diagram of bridgeless PFC topology.

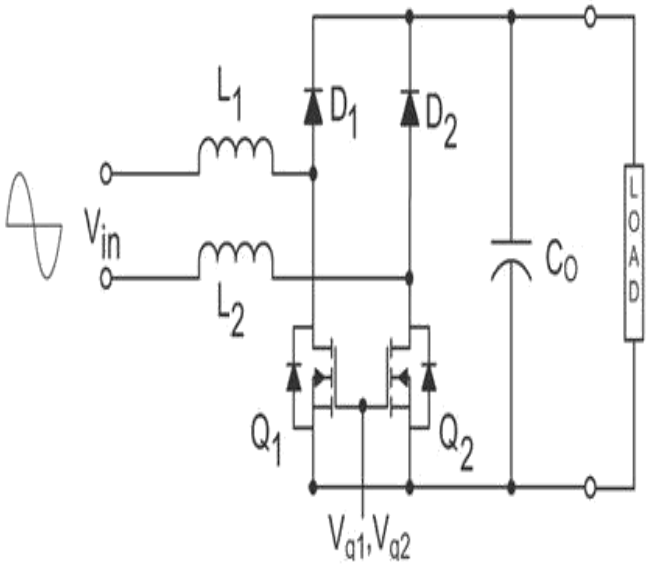


Fig.2.Bridgeless PFC topology

C. Dual-boost PFC topology

The advantage of dual-boost PFC topology is [25] minimizes the gate loss, reduces the losses at light loads, the conduction loss can be minimized. The light-load efficiency improved by external device, which leads cost expense and improve controller complexity.

D. Semi-bridgeless PFC boost topology

Semi-bridgeless PFC boost topology is the conventional bridgeless topology with two extra slow diodes, that is, D_a and D_b that connect the input to the PFC ground. The slow diodes were added to address EMI- related issues [22], [23].

The current does not return through these diodes; therefore, their related conduction victims are small. The semi-bridgeless configuration also resolves the suspended input line problem with respect to the PFC stage ground. Fig.3 represents the circuit diagram of semibridgeless PFC topology.

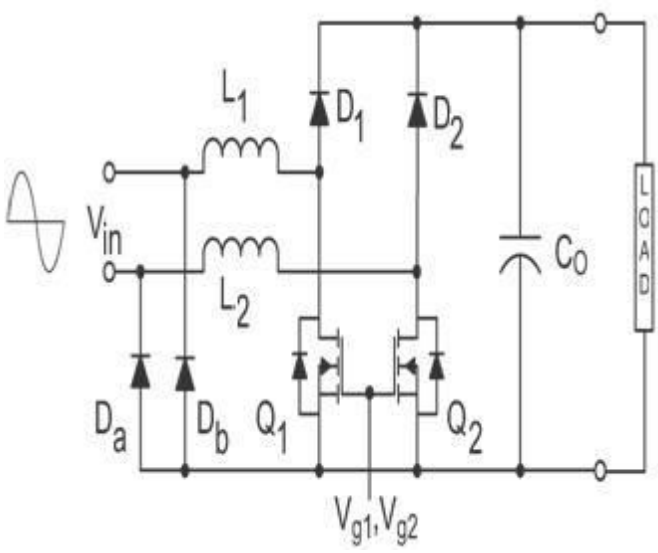
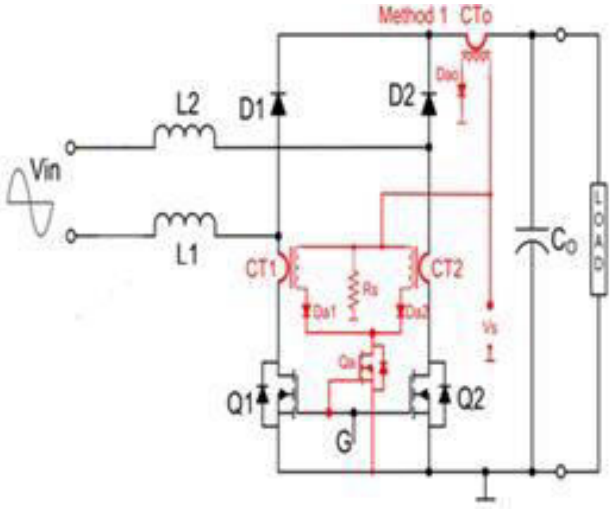


Fig3.Semi bridgeless PFC topology.

E. Current sensing techniques

Three exclusive current-sensing circuits (Methods 1–3) for the bridgeless PFC boost topology are shown in Fig. 4 to sense the current in the MOSFET and diode paths independently, as the current path does not share the similar ground throughout each half-line cycle [13], [26].

Method 1 Fig. 4(i) is the passive current-sensing scheme reported in [13], which requires three current-sensing transformers, one in series with each switch and a third in the positive dc rail to sense the collective current of the two diodes, and an supplementary signal transistor with its related difficult control circuitry. Method 2 F i g . 4 (i i) uses a simple, but costly Hall Effect sensor to straightly sense the input current.



F i g . 4 (i) current-sensing method.1 implemented with bridgeless PFC topology.

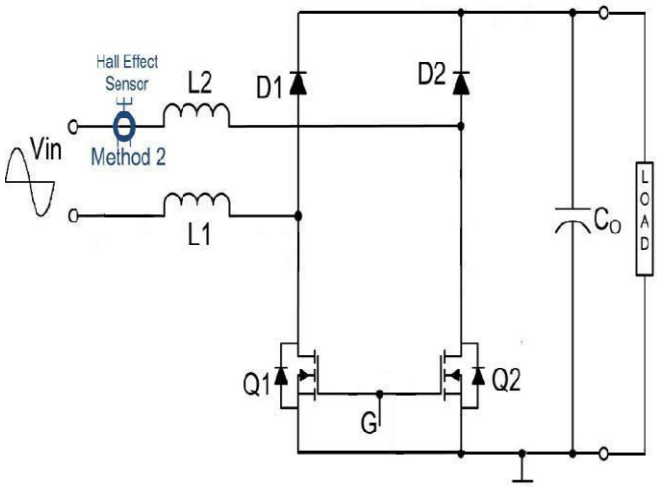


Fig. 4(ii) current-sensing method.2 implemented with bridgeless PFC topology.

Method 3 Fig.4 (iii) uses a differential-mode amplifier, which is connected in series with the input. This method is moderately less cost.

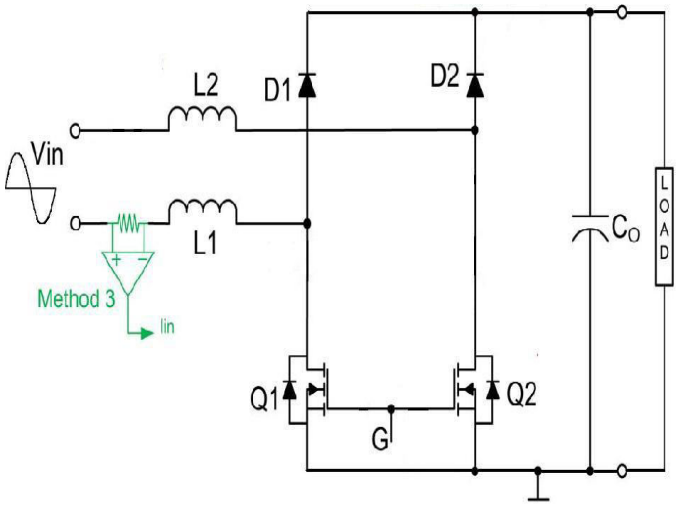


Fig. 4(iii) current-sensing method.3 implemented with bridgeless PFC topology.

Where the current-sensing voltage is small to reduce the power loss, the power factor can be ruined by the sensing noise.

II-PROPOSED SYSTEM

Vehicle storage charging is one of the applications of PSSB converter [29]. The Fig. 5 represents the block diagram of Phase Shifted boost power factor corrected converter. For the controller section PI controller is used.

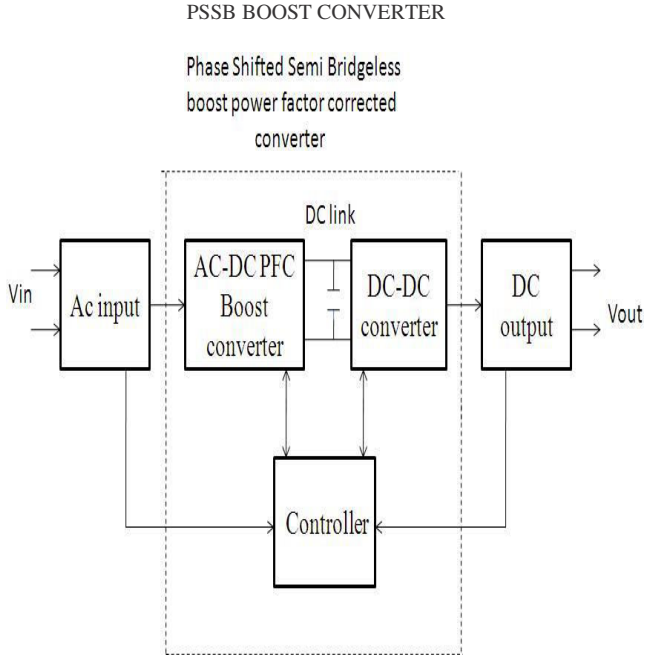


Fig.5 PSSB-block diagram

The proposed PSSB topology shown in Fig.6 is used the current sensing method [27]. This method is used to find the inductor current by sensing the MOSFET current [28].

This topology consists the decoupled MOSFET gates, it uses two slow diodes (Da and Db), like to that of the semi-bridgeless PFC boost, to link the ground of the PFC to the input line.

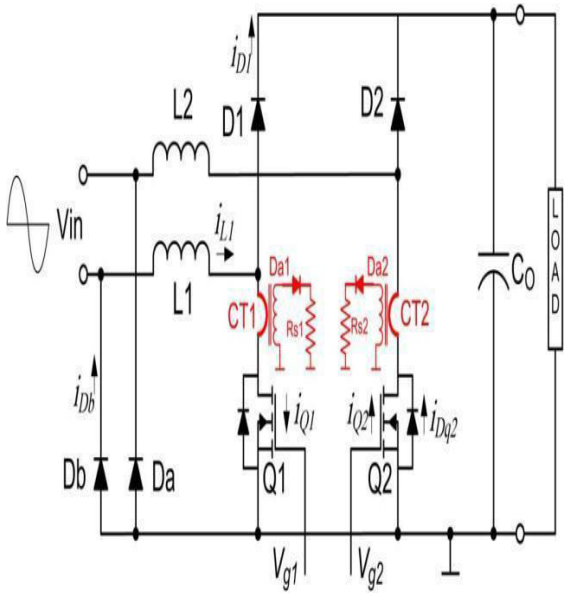


Fig. 6. Proposed PSSB PFC boost topology with a simple current-sensing circuit.

The gating signals for the MOSFETs are 180° out of phase, as shown in Fig. 7. The proposed topology consists the advantages of both the bridge- less and semi-bridgeless boost PFC topologies. Its features a r e reduced EMI, high efficiency at light loads, and low lines, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn.

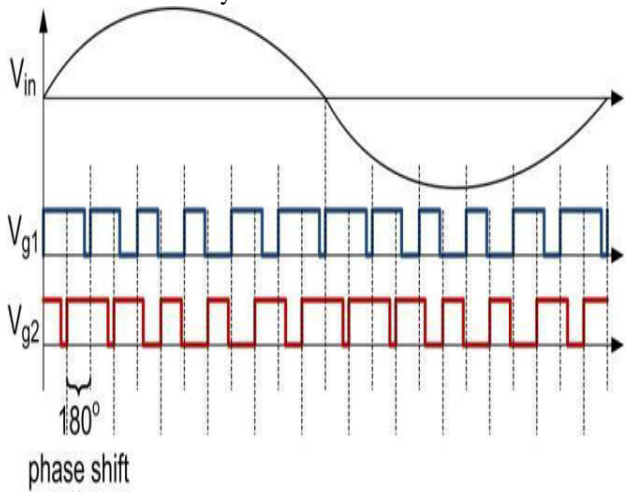


Fig. 7.Gating scheme for the PSSB PFC topology.

The following section includes operation of the proposed converter and converter simulation output.

III-OPERATINON OF CONVERTER

The proposed topology uses two slow diodes (D_a and D_b) to connect the ground of the PFC to the input line. The current does not return through these diodes, so their related conduction losses are low. The gating signals for MOSFETs are 180° out of phase. To evaluate the circuit operation, the input line cycle has been divided into the positive and negative half-cycles. The full circuit operation depends on the duty cycle.

A.POSITIVE HALF CYCLE OPERATION

During the positive half-cycle, when the input voltage is positive, Q1 turns on and current flows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns off, energy stored in L1 and L2 is released as current flows through D1, through the load and returns through the body diode of Q2/partially through Db back to the input.

The detailed operation of the proposed converter depends on the duty cycle. During any half-cycle, the converter duty cycle is either greater than 0.5 (when the input voltage is smaller than half of output voltage) or smaller than 0.5 (when the input voltage is greater than half of output voltage). The following operating intervals is for where the duty cycle is greater than 0.5.

Interval 1 [$t0 - t1$]: At $t0$, Q1/ Q2 are turns on. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split among Db, Dq2, and Q2.

Interval 2 [$t1 - t2$]: At t1, Q1 is on, and Q2 is turns off. During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides the load energy. The return current is split only between Db and Dq2.

Interval 3 [$t2 - t3$]: At t2, Q1/Q2 is turns on again, and interval 1 is repeated. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The return current is again split among D_b, Dq2, and Q2.

Interval 4 [$t3 - t4$]: At t3, Q1 is turns off, and Q2 is turns on,. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and D_b.

The following operating intervals are for which the duty cycle is less than 0.5.

Interval 1 [$t0 - t1$]: At $t0$, Q1/ Q2 are turns off,. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 2 [$t1 - t2$]: At $t1$, Q1 is t u r n s on, and Q2 is t u r n s off,. During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split only between Db and Dq2.

Interval 3 [$t2 - t3$]: At $t2$, Q1/Q2 is turns off again, and interval 1 is repeated,. During this interval, the current in series inductances L1 and L2 decreases linearly, and the energy in these inductors are released. The energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 4 [$t3 - t4$]: At $t3$, Q1 is off, and Q2 is turns on,. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.Detailed Positive Half Cycle Operation and analysis for $D > 0.5$ and $D < 0.5$ is analyzed in [29].

B.NEGATIVE HALF CYCLE OPERATION

During the negative half-cycle, when the AC input voltage is negative, Q2 turns on and current flows through L2 and Q2 and continues through Q1 and then L1, returning to the line while storing energy in L2 and L1. When Q2 turns off, energy stored in L2 and L1 is released as current flows through D2, through the load and returns split between the body diode of Q1 and Da back to the input. The operation of converter during the negative input voltage half-cycle is similar to the operation of converter during the positive input voltage half-cycle.

IV - RESULTS OF PSSB BOOST SYSTEM

The Simulation of phase shifted semi bridgeless boost PFC converter is simulated for 1KW load in MATLAB. Fig. 8 shows the gating signal for 180 degree phase shift.

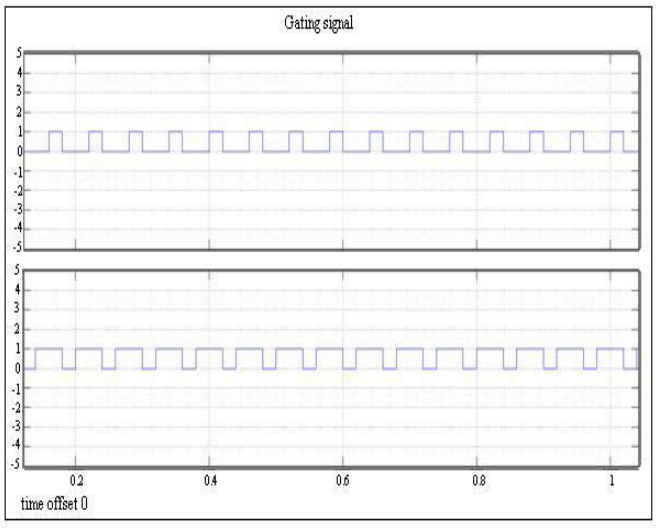


Fig.8.gate signal waveform

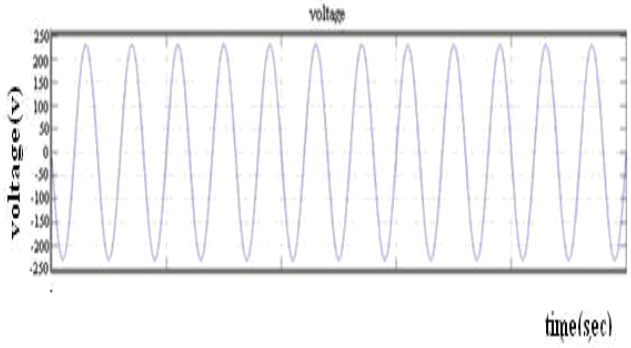


Fig.9 Input voltage

Simulation results of input voltage and output voltage shown in fig.9 input voltage, fig.10 output voltage.

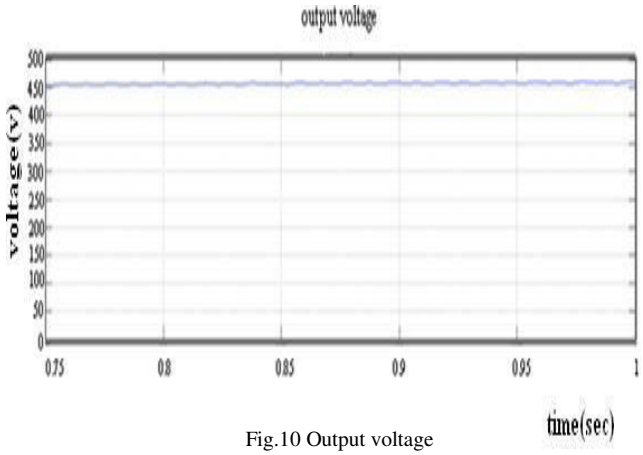


Fig.10 Output voltage

The THD value of proposed converter is below 5%.The fig.11 represents the output waveform of semi bridgeless converter with solar source. Here the converter is act as the dc-dc converter when it is connected to solar panel. The maximum power point tracking is used to achieve the maximum amount of power.

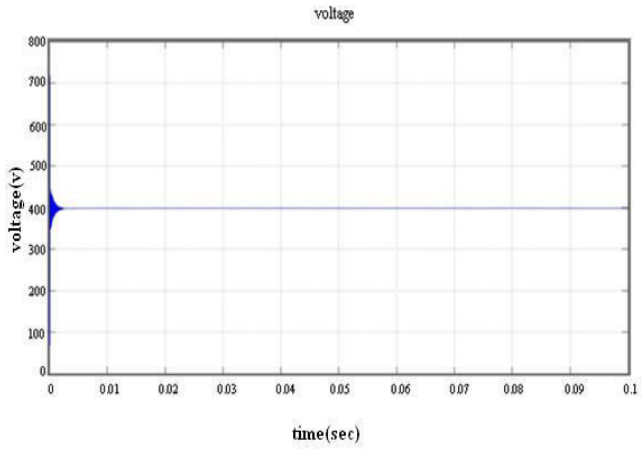


Fig.11 output voltage

V-CONCLUSION

A better-performance Phase Shifted Semi Bridgeless boost converter topology has been proposed with simplified current sensing method. The converter advantageous features are high efficiency at light-load and low-line conditions, small in charger size, less cost, less charging time, and less cost of electricity. The input supply of the converter is 230V. While using this proposed converter system current THD is less than 5% for 1KW to 3KW load. The power factor is greater than 0.9 from 50% load to full load. It can provide better out voltage while it act as the dc-dc converter.

VI -REFERENCES

[1]Y. J. Lee, A. Khaligh, and A. Emadi, ―Advanced integrated bidirectional AC–DC and DC–DC converter for plug-in hybrid electric vehicles,‖ *IEEE Trans. Veh.. Technol.*, vol. 58, no. 8, pp. 3970–3980, Oct. 2009.

[2]K. Morrow, D. Karner, and J. Francfort, ―Plug-in hybrid electric vehicle charging infrastructure review,‖ U.S. Dept. Energy—Veh. Technol. Pro-gram, Washington, DC, 2008.

[3]L. Petersen and M. Andersen,―Two-stage power factor Corrected power supplies; The low component -stress approach,‖ *in Proc IEEE APEC* 2002,vol.2,pp.1195- 1201.

[4]B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, ―A review of single-phase improved power quality AC–DC converters,‖ *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[5]M. O'Loughlin, ―An interleaved PFC preregulator for high-Power converters,‖ *in Proc. texas instrum Power Suppl Design Semin*.,2007,pp.5-1 to 5-14.

[6]Y. Jang and M. M. Jovanovic, ―Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end,‖ *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp.1394–1401, Jul. 2007.

[7]L. Balogh and R. Redl, ―Power-factor correction with interleaved boost converters in continuous-inductor-current mode,‖ in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1993, pp. 168–17

[8]C. Wang, M. Xu, and F. C. Lee, ―Asymmetrical interleaving strategy for multi-channel PFC,‖ in *Proc. IEEE Appl. Power Electron. Conf. Expo.*2008, pp. 1409–1415.

[9]P. Kong, S. Wang, and F. C. Lee, ―Common-mode EMI study and reduction technique for the interleaved multichannel PFC converter,‖ *IEEE Trans. Power Electron,.*vol. 23, no. 5, pp. 2576– 2584, Sep. 2008.

[10]C. Wang, M. Xu, F. C. Lee, and B. Lu, ―EMI study for the interleaved multi-channel PFC,‖ in *Proc. IEEE PESC*, 2007, pp. 1336–1342.

[11]B. Lu, R. Brown, and M. Soldano, ―Bridgeless PFC implementation using one cycle control technique,‖ in *Proc. IEEE Appl.Power Electron. Conf. Expo.*, 2005, vol. 2, pp.12–817.

[12]C. Petrea and M. Lucanu, ―Bridgeless power factor correction converter working at high load variations,‖ in*Proc. ISSCS*, 2007, vol. 2, pp. 1–4.

[13]U. Moriconi, ―A bridgeless PFC configuration based on L4981 PFC controller,‖ STMicroelectronics, Geneva,Switzerland, STMicroelectron. Appl. Note AN1606, 2002.

[14]J. M. Hancock, ―Bridgeless PFC boosts low-line efficiency,‖ Infineon Technol., Milpitas, CA, 2008.

[15]Y. Jang, M. M. Jovanovic, and D. L. Dillman, ―Bridgeless PFC boost rectifier with optimized magnetic utilization,‖in *Proc IEEE Appl. Power Electron. Conf. Expo.*, 2008, pp. 1017–1021.

[16]Y. Jang and M. M. Jovanovic, ―A bridgeless PFC boost rectifier with optimized magnetic utilization,‖ *IEEE Trans.Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.

[17]W. Y. Choi, J. M. Kwon, E. H. Kim, J. J. Lee, and B. H.Kwon, ―Bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems,‖*IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 769– 780,Apr. 2007.

[18]L. Huber, J. Yungtaek, and M. M. Jovanovic,―Performance evaluation of bridgeless PFC boost rectifiers,‖ *IEEE Trans Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[19]W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, ―Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction,‖ *IET Power Electron.*, vol. 1, no. 2, pp. 194–202, Jun.2018.

[20]M. Ramezani and S. M. Madani, ―New zero-voltage- switching bridgeless P, using an improved auxiliary circuit,‖

[21]J. Zhang, B. Su, and Z. Lu, ―Single inductor three-levelbridgeless boost power factor correction rectifier with nature voltage clamp,‖ *IET Power Electron.*, vol. 5, no. 3, pp. 358– 365, Mar. 2018.

[22]P. Kong, S. Wang, and F. C. Lee, ―Common mode EMI noise suppression for bridgeless PFC converters,‖ *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291–297, Jan.20.

[23]T. Baur, M. Reddig, and M. Schlenk, ―Line-conducted EMI- behaviour of a high efficient PFC-stage without input rectification,‖ Infineon Technol., Milpitas, CA, 2006, Appl Note.

[24]H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, ―Common mode noise modeling and analysis of dual boost PFC circuit,‖ in Proc IEEE INTELEC, 2004, pp. 575–582.

[25]T. Qi, L. Xing, and J. Sun, ―Dual-boost single-phase PFC input current control based on output current sensing,‖ *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2523– 2530, Nov. 2009.

[26]W. Frank, M. Reddig, and M. Schlenk, ―New control methods for rectifier- less PFC-stages,‖ in *Proc. IEEE Int. Symp. Ind.Electron.*, 2005, vol. 2,pp. 489–493.

[27]*Interleaving Continuous Conduction Mode PFC Controller*,Texas In-strum., Dallas, TX, Apr. 2011.

[28]V. S. Oknaian, ―Inductor current synthesizer for switching power sup-plies,‖ U.S. Patent 6 38159, Apr. 30, 2002.

[29]Fariborz Musavi,Wilson Eberle,, and William G. Dunford,, *"*A Phase-Shifted Gating Technique With Simplified Current Sensing for the Semi-Bridgeless AC–DC Converter*" IEEE Trans.Vech.Tech..Vol 62no 4* may 2013.