

"Review A Novel Topology for Harmonics Reduction in Photovoltaic Inverter"

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Abstract :This paper analyzes and compares two approaches for dc to ac power conversion. First approach uses cascaded H-Bridge Inverter and second uses new Multi-level Scheme having Level Modules and H-Bridge. The simulation is done in SIMULINK/ MATLAB Software. The Total Harmonic Distortion in output load voltage, active Power and reactive Power produced by both the approaches are compared. It is shown that THD produced in second scheme is better upto a certain stages of the first scheme. And the available active and reactive powers are larger for the second scheme.

INTRODUCTION :-

Nowadays solar energy is widely used as source of electrical energy. But generated electrical energy from solar panel is in the form of direct current. Conversion of DC supply into AC supply is done by using inverter technique. A solar panel is main source of DC power. Before feeding solar DC power to grid. It is essential to covert DC power into the AC form. The main technique used for this conversion is the inverter technique. There are a number of ways to implement the inverter technique like Cascaded H-Bridge MLI, Diode clamped MLI and flying capacitor MLI. The following new approach is one of the most important techniques to implement the inverter for conversion of DC power into AC power. The 2-level inverters are commonly used to produce an AC voltage from a DC voltage. The two level inverters can only form two different yields or two level of voltages. The THD in output of 2-level inverter is high, because output voltage wave form is only having two level. On the other hand, in MLI these voltage levels extend so as to decrease THD.

A. Proposedmethod:

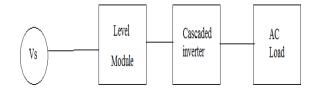


Fig.1 Propose Method

Above Fig.1 demonstrate the block diagram of multilevel method. It contains of level module, bridge inverter and the D.C. voltage source with RL load which can be isolated. The output voltage waveform level is totally dependent on the number of level modules used in circuit. If we want three levels in the output waveform the none level Module isused, and soon. Quantity of levels in the output waveforms is calculated by following method.

Level Module: -

The o/p is depending on number of level module used in the circuit.



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where,

N = Quantity of levels in the output waveform. K = Number of level module used.

In the described method three level modules are used for obtaining 15-levels in the production waveform.

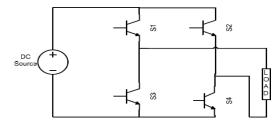


Fig. 2 Cascaded Inverter

The cascade technique is use to attain preferred AC voltage from numerous levels of DC voltages to synthesize. The H-Bridge inverter contains of 4-switches, dc source and load. Each switch in H-Bridge having conducts for period of 180°. The same gate pulses provide to diagonal switches. If the no. of stages of the converter is amplified, output stage level is also increased. For 1-stage, output is two levels. For 2- steps, output is 3 levels and so on.

B. Implementation of proposedmethod:

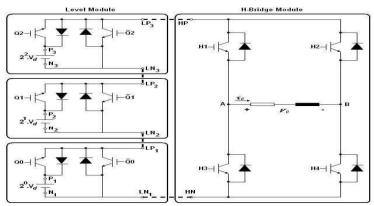


Fig. 3 Proposed Multilevel Inverter

The Fig. 3 demonstrates circuit diagram of the proposed MLI circuit comprises of Level Module, H- Bridge inverter and load connected to grid. The modulation control technique is used for providing gate pulses to Converter switches. The modulation control systems for the MLI can be separated into two categories; one is the fundamental switching frequency and second is high switching frequency. PWM such as different level carrier-based, space vector & Multilevel SPWM needs many carriers. Each DC source needs its own carrier. The no. of multi-carrier methods have been used for moderate the distortion in MLI, with the help of conventional SPWM with triangular carriers. An 'n' Level MLI (n-1) carriers are needed.



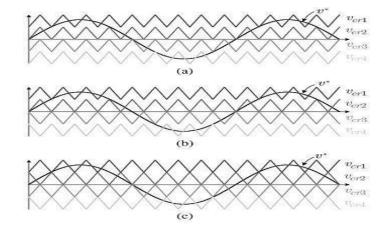


Fig.4 Carrier signal stoinc rease the number of level for inverter

Above Figure 4 shows the carrier signals to increase the number of level for inverter. As the carrier signals are increased the level of the output waveforms are increased. For 3-level the two carrier signals are used such that for 7-level six carrier signals are used soon.

		LEVEL INVERTER																
Single Stage V=7V	S.No.	$\begin{array}{c} \alpha_1 \\ (^{\circ}) \end{array}$	α ₂ (°)	α ₃ (°)	Active Power P	Reactive Power Q	THD (%)		S.No	α ₁ (°)	α ₂ (°)	α ₃ (°)	α ₄ (°)	α ₅ (°)	α ₆ (°)	P (W)	Q (VAr)	THE (%)
	-	C)	()	0	(W)	(VAr)		4 Stage	1	0	30	60	90			80.5	25.36	17.
	1	0			7.2	2.26	48.77	V=28V	2	0	25	50	75			90.0	28.3	17
	2	30			7.2	2.27	48.47		3	30	60	90	120			805	25.36	17.
Two Stage V=14V									1	0	20	40	60	80		139.7	44	15
	1	30	60		26.9	8.46	32.14	5 Stage V=35V	2	20	40	60	90	120		152.8	28.5	16
	2	45	90		24.57	7.73	29.49		3	0	25	50	75	100		120.8	38.0	14
	3	60	120		21.59	6.8	31.57		4	25	50	75	100	120		124.6	39.2	15
									1	0	15	30	45	60	75	210	66.2	16
Three Stage V=21V	1	0	40	80	46.19	14.52	22.2	6 Stage	2	0	20	40	60	80	100	178.7	56.2	12.
	2	25	50	75	57.63	4.38	24.4	V=42V	3	0	25	50	75	100	125	143.3	45	16
	3	30	60	90	53.7	16.9	22.15		4	20	40	60	80	100	120	178.8	56.2	12

For 6 Stage inverter THD of 12.34% is found to be minimum for $\alpha 1=20^\circ$, $\alpha 2=40^\circ$, $\alpha 3=60^\circ$, $\alpha 4=80^\circ$, $\alpha 5=100^\circ$, $\alpha 6=120^\circ$. For

7 Stage inverter THD of 12.14% is found to be minimum for $\alpha 1=0^{\circ}$, $\alpha 2=15^{\circ}$, $\alpha 3=30^{\circ}$, $\alpha 4=45^{\circ}$, $\alpha 5=60^{\circ}$, $\alpha 6=75^{\circ}$, $\alpha 7=90^{\circ}$.

For 8 Stage inverter THD of 9.6% is found to be minimum for, $\alpha 1=15^{\circ}$, $\alpha 2=30^{\circ}$, $\alpha 3=45^{\circ}$, $\alpha 4=60^{\circ}$, $\alpha 5=75^{\circ}$, $\alpha 6=90^{\circ}$,

α7=105°, α8=120°.

New Multilevel Approach The proposed multilevel inverter circuit consists of Level Module, H-Bridge inverter, input dc voltage and RL load as shown in Fig. 5. This load may be an isolated RL type or a grid.



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		SI	MULATI	ON RESU	LTS FOR		BLE III AND 8 ST	AGE MULT	TI LEVEL I	VERTER					S	MULATI	ON RESU	LTS FOR		BLE III AND 8 ST.	AGE MULI	ILEVEL I	NVERTER		
7 Stage V=49V	S. No	α ₁ (°)	a2 (°)	α ₃ (°)	a4 (°)	a5 (°)	а ₆ (°)	a7 (°)	a8 (°)	P (W)	Q (VAr)	THD in Voltage (%)	7 Stage V=49V	S. No	α ₁ (°)	a2 (°)	α3 (°)	α4 (°)	a5 (°)	a6 (°)	a7 (°)	α ₈ (°)	P (W)	Q (VAr)	THD in Voltage (%)
	1	0	20	40	60	80	100	120		210.4	66.2	13.2		1	0	20	40	60	80	100	120		210.4	66.2	13.2
	2	0	15	30	45	60	75	90		269.2	51	12.85		2	0	15	30	45	60	75	90		269.2	51	12.85
	3	15	30	45	60	75	90	105		198.7	63.6	12.82		3	15	30	45	60	75	90	105		198.7	63.6	12.82
	4	0	15	30	50	70	85	100		242	76	12.27		4	0	15	30	50	70	85	100		242	76	12.27
8 Stage V=56V	1	0	15	30	45	60	75	90	105	315.8	99.3	10.26	8 Stage V=56V	1	0	15	30	45	60	75	90	105	315.8	99.3	10.26
	2	15	30	45	60	75	90	105	120	454.6	119.2	9.6		2	15	30	45	60	75	90	105	120	454.6	119.2	9.6
	3	0	20	40	60	80	100	120	140	231	72.6	15.4		3	0	20	40	60	80	100	120	140	231	72.6	15.4
	4	0	10	30	40	50	60	80	90	563	197	14.02		4	0	10	30	40	50	60	80	90	563	197	14.02
	5	10	20	30	50	60	80	90	100	604.8	206.9	11.9		5	10	20	30	50	60	80	90	100	604.8	206.9	11.9

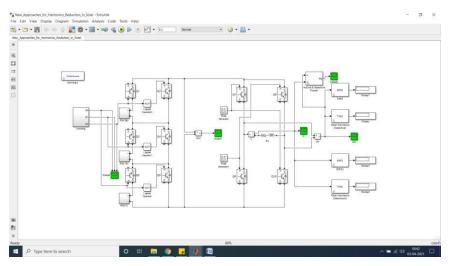
The level of output voltage shape depends on the level module used in the circuit. Output Level

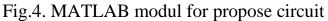
n=2(m+1)-1

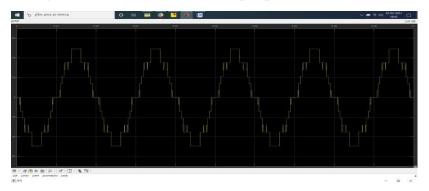
where $\,$ m is the no. of Level Module used. The no. of switches used in the circuit r=2m+4 $\,$

The input dc voltage varies as: Vk = 2(k-1)VdWhere k = 1, 2, 3, ... m.

Simulation & Result :









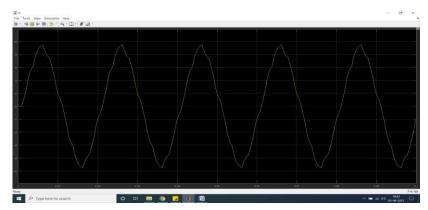


Fig5. Load Voltage & Load Current for three level in MATLAB Simulation

Conclusions :

In this paper, THD in load voltage, Active Power and Re-active Power are evaluated for a proposed inverter circuit with Solar Panel as a dc Source and also a battery using SIMULINK/MATLAB software. The performances are compared for different power factor loads keeping the dcinput voltage same without using the filter. In both cases, THD present in load voltage may always be reduced be-low 5% by the use of filter. The THD obtained from proposed inverter scheme is comparable to THD ob-tained from conventional inverter scheme but the no. of switches required is less in the proposed scheme. The overall observation is that in the range of pf from 0.8 to 0.85 the performanced PV panel connected inverter is superior to that with pure dc (battery) as input source.

References:

[1] S. J. Lee, H. S. Bae and B. H. Cho, "Modeling and control of the single-phase photovoltaic grid-connected cascaded Hbridge multilevel inverter," 2009 IEEE Energy Conversion Congress and Exposition, San Jose, CA, 2009, pp. 43-47, doi: 10.1109/ECCE.2009.5316126.

[2] M. S. Bin Arif and S. M. Ayob, "A novel single phase five-level photovoltaic based grid-connected inverter," 2014 IEEE Conference on Energy Conversion (CENCON), Johor Bahru, 2014, pp. 325-330, doi: 10.1109/CENCON.2014.6967524.

[3] A. Tariq, M. A. Husain, M. Ahmad and M. Tariq, "Simulation and study of a grid connected multilevel converter (MLC) with varying DC input," 2011 10th International Conference on Environment and Electrical Engineering, Rome, 2011, pp. 1-4, doi: 10.1109/EEEIC.2011.5874704.

[4] N. Karnik, D. Singla and P. R. Sharma, "Comparative analysis of harmonic reduction in multilevel inverter," 2012 IEEE Fifth Power India Conference, Murthal, 2012, pp. 1-5, doi: 10.1109/PowerI.2012.6479521.