International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 04 Issue: 07 | July -2020 ISSN: 2582-3930

Comparative Analysis of Logic Gates for Combinational Circuit Applications by using Microwind tool

Vignesh.R[1], Rajalakshmi.S[2], Bhuvaneshwari.S[3]

[1]vignesh.R, ECE Department, Annamalai University

[2]Rajalakshmi.S, ECE Department, Annamalai University

[3]Bhuvaneshwari.S, ECE Department, Prathyusha engineering College

---

Abstract: The logic gates are the basic building blocks of VLSI and embedded applications. These gates can be designed by some designing techniques and implemented at different levels of architectures. These papers is mainly focus on design and evaluate the performance of logic gates used in the Adders and Multiplier using various design technique like CMOS design and GDI design . These different design styles have merits and demerits with reference to performance measure as Delay, Power consumption, Area and Transistor Count. The design and simulation of logic gates is performed on Microwind tool. Comparative study between logic gates designed using CMOS and GDI technique is presented in this paper, with performance measure as Number of transistor count and Power calculations.

Key word: logic gate, CMOS design, GDI design, number of transistor, Microwind tool.

1.Introduction:

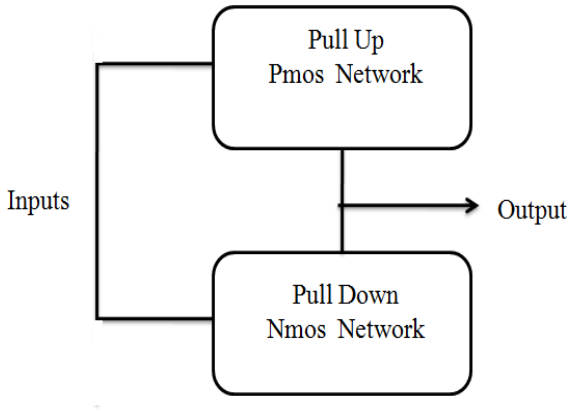
Very Large Scale Integrate (VLSI) circuits are momentous for designing of high performance and portable devices. The performance parameters like speeds, area, cost and power are the main parameters plays vital role in the VLSI technology. The logic gates are basic building components and accommodate as the structure blocks to VLSI digital logic circuits utilizing combinational logic. The major function of logic gates m used in to perform binary calculations, which in term is used within adder circuit and multiplier blocks, and also found in Comparator, Compressor, Parity checker, Error detecting or Error correcting and Code converter.

The basic principle of operation on basic gates is that the circuit operation on two voltage levels considered in to logic levels as logic low (0) and logic high (1).When applied inputs either logic 0 or logic 1 will get a output gate reproduction depends upon the particular logic of the gate. In this paper we are consider the basic logic gates are NOT, AND, NAND, OR, NOR, XOR and XNOR. The gates can be designed using different designing techniques, we have considered Complementary Metal Oxide Semiconductor (CMOS) design, and Gate Diffusion Input (GDI) design for our consideration .Comparative analysis of the gates with techniques is coated with respect to transistor count.

2.An Overview about Designing Techniques

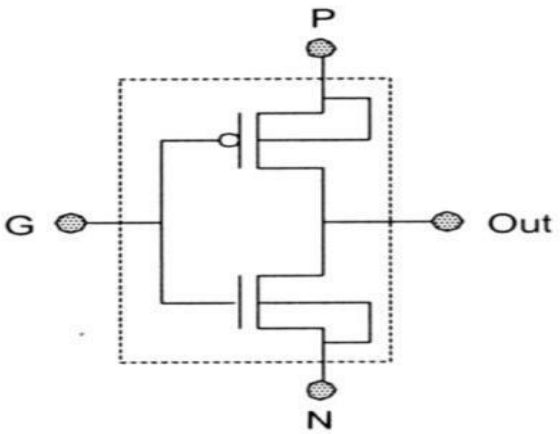
A. CMOS Design Technique

CMOS (Complementary metal oxide semiconductor) is the most commonly used technique in the digital circuits. It's a combination of pull-up PMOS network and pull-down NMOS network. Where pull up network PMOS set the output is logic high (1) and pull-down NMOS network set the output is logic low (0) respectively and the both network cannot be activated and deactivated at a time, so we can say it is mutually exclusive. The advantagof this design technique is logic gates output level is not degraded (Full swing output), scale up the operation speed (Delay reduced) and more power, area consumption because number of transistor require designing a gate.



B. GDI Design Technique

Gate Diffusion Input is same as the CMOS inverter, it has smaller area than the CMOS design and implemented in complex logic function. Construction this design style using three inputs, they are G (common input to both PMOS and NMOS), P (source or drain input of PMOS), N (source or drain input of NMOS). The supplied inputs or can of P and G can be V_{dd} or can be grounded or can be input signal depending on the circuit to be designed by using logic levels of the input and output. The advantages of this design technique are used less number of transistor compare to CMOS design technique and high performance (reduced the delay) and low power consumption. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies



3.Results and Discussion:

The design and functional verification of all the basic gates is performed on the MICROWIND TOOL Design.

A. SIMULATION RESULT:

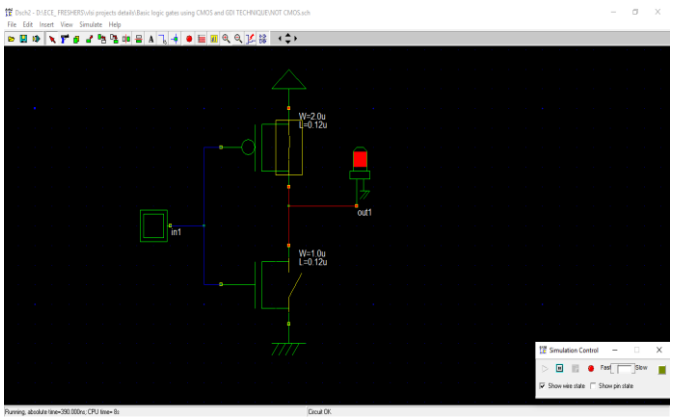


Fig-1: CMOS- GDI –NOT GATE

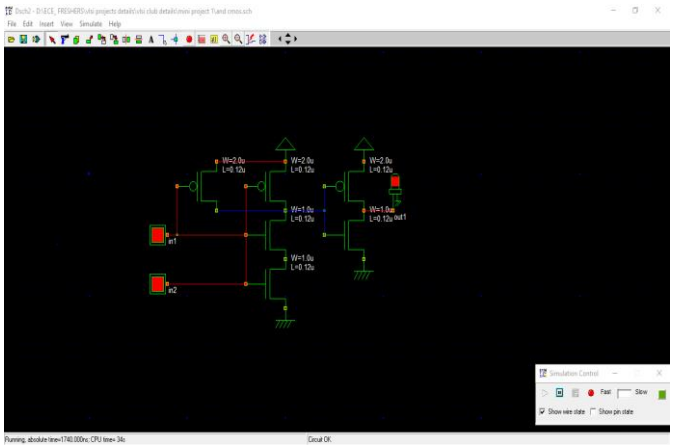


Fig-2: CMOS ANDGATE

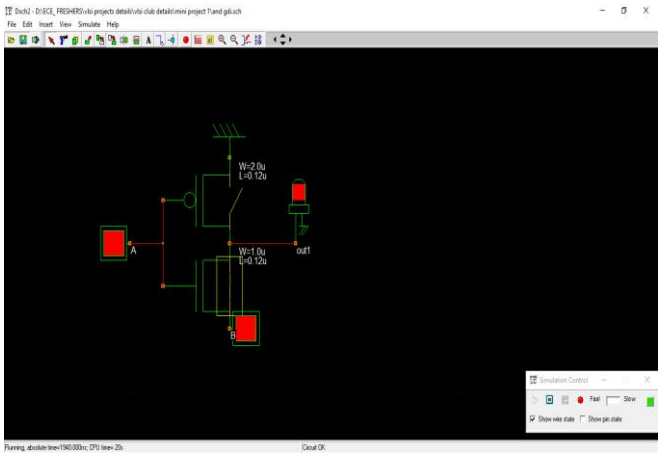


Fig-3: GDI ANDGATE

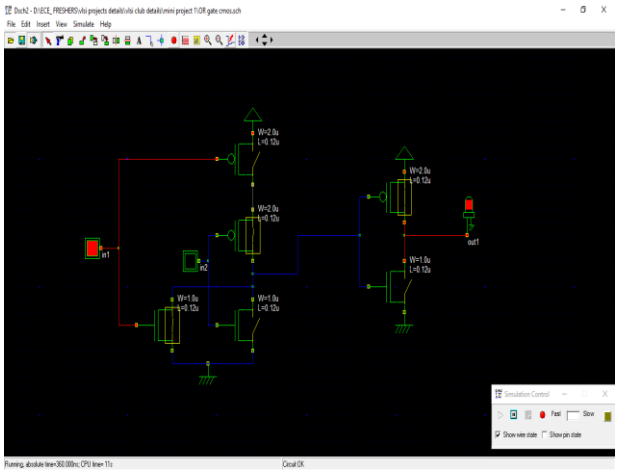


Fig-4: CMOS ORGATE

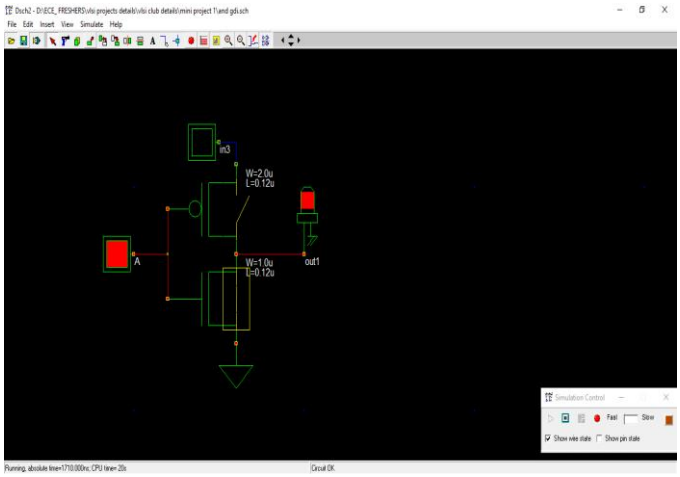


Fig-5: GDI ORGATE

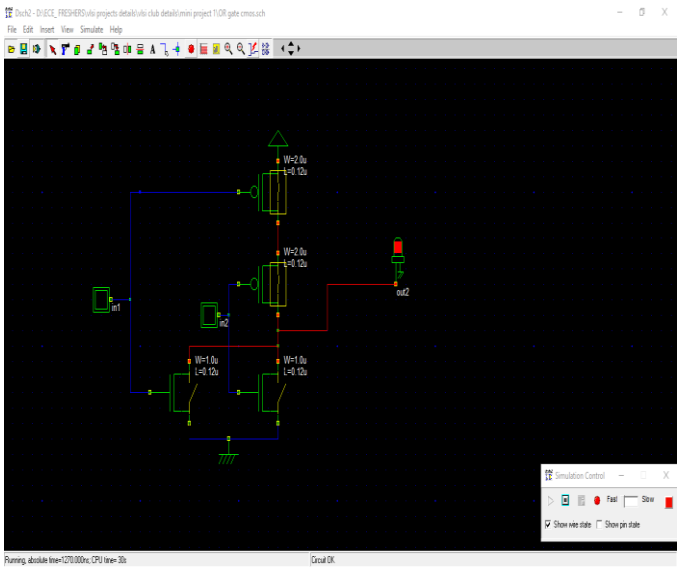


Fig-6: CMOS NORGATE

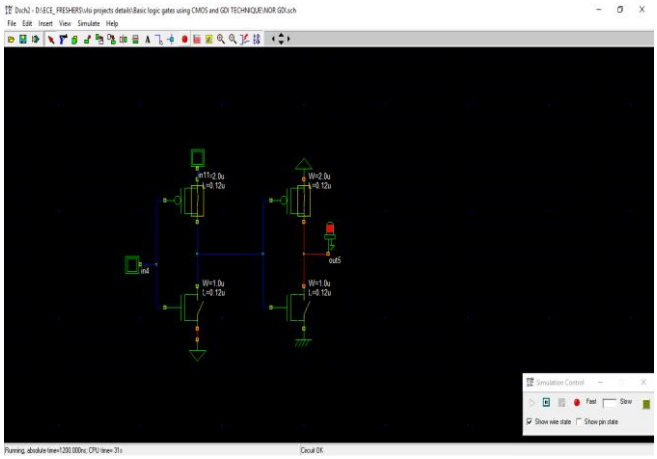


Fig-7: GDI NORGATE

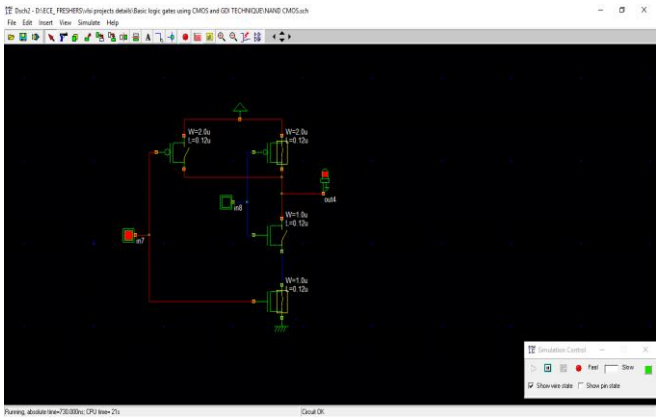


Fig-8: CMOS NANDGATE

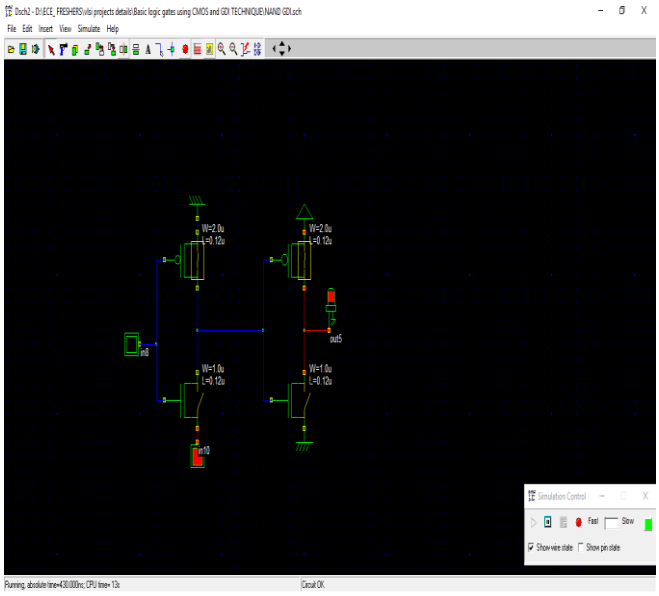


Fig-9: GDI NANDGATE

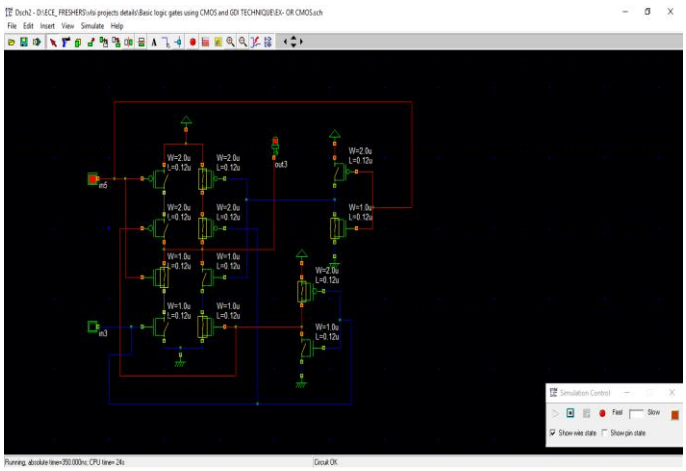


Fig-10: CMOS EX-ORGATE

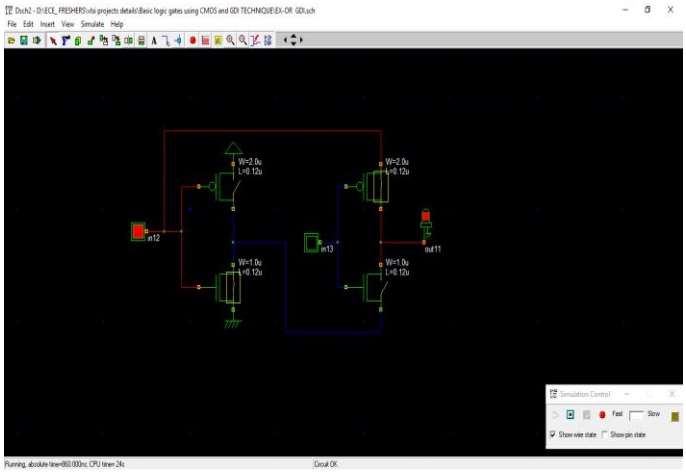


Fig-11: GDI EX-ORGATE

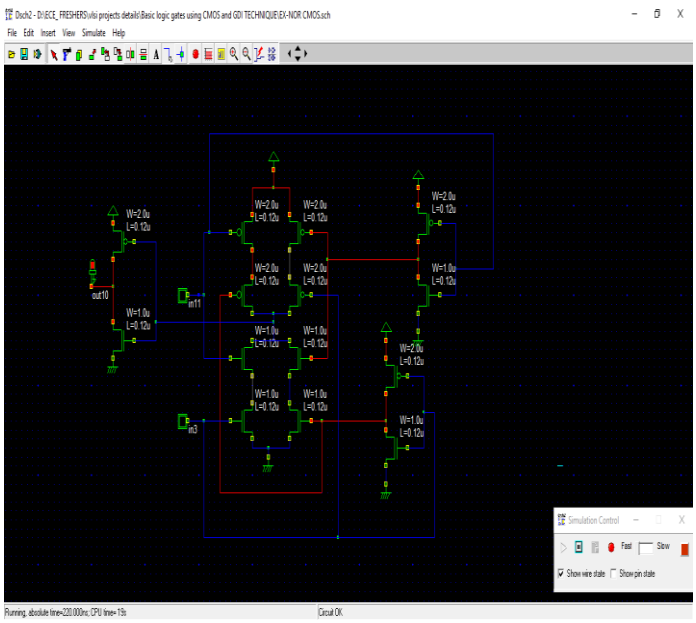


Fig-12: CMOS EX-NORGATE

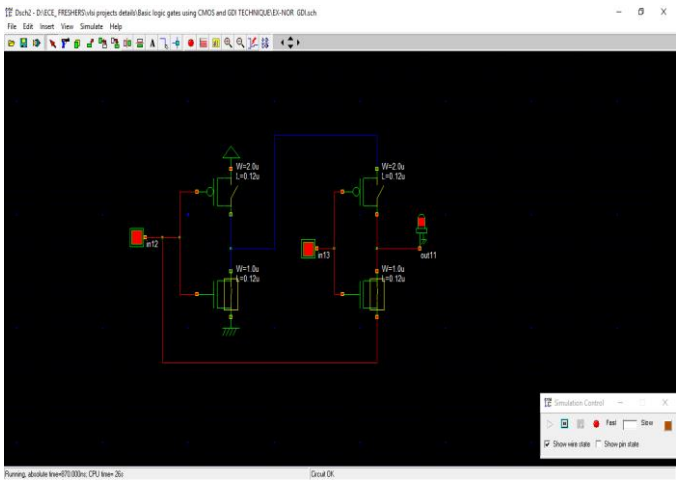


Fig-13: GDI EX-NORGATE

3.COMPARATIVE ANALYSIS:

Here, we have compared the number of transistor used in CMOS and GDI technique.

TABLE-1: Comparison of Transistor count

TYPES OF BASIC GATES	TRANSISTOR COUNT FOR CMOS	TRANSISTOR COUNT FOR GDI
NOT	2	2
AND	6	2
OR	6	2
NAND	4	4
NOR	4	4
EX-OR	12	4
EX-NOR	14	4

4.Conclusion

In this paper, we have designed basic gates like NOT, AND, NAND, NOR, OR, XOR and XNOR gates using CMOS, and GDI technique. A comparative analysis of all the basic gates is made using different design styles is mentioned here. This paper provides the base to select the design style for a logic gate to be selected for adder or multiplier based on the requirement of the design, the gate can be selected by the designer by taking the best out of performance measures considered.

These design technique are suitable for arithmetic and logic processing and in VLSI applications where a low power, high speed and area prime concern. Finally we can conclude that number of transistor count is reduced in GDI technique compared with CMOS technique and rather than CMOS if we select GDI for designing circuit, the circuit can consume less power consumption with less area and high speed of operation.

REFERENCES

1. Neha Goyal, Renu Single, Puneet Goyal, "Study and Analysis of Universal Gate using Stacking Low Power Technique",International Journal of Computer Science and Information Technology, Vol 5 (3), 2014

2. Raiz Sultane, Jagannath Samantha, "Comparison of Different Design Technique of XOR and AND Gate using EDA Simulation Tool", International Journal of VLSI and Embedded System, Vol 04, Issue 03, May-June 2013

3. A P Godse, U A Bakshi "Basic electronics- Logic gates" A introduction to basic gates and its behavior, PP 5-35 to 5-38,2015, ISBN 978-93-332-0536-8.

4. Sudeshna Sarkar,Monika Jain, Arpita Saha, Amitha Rathi, "Gate Diffusion Input: A Technique for Fast Digital Circuits (Implementation on 180 nm Technology)", IOSR Journals of VLSI and Signal Processing, Vol 4, Issue 2, Ver. IV (March-April 2014)

5. Sandeep Sangwan, Mrs Jyothi Kedia, Deepak Kedia, "A Comparative Analysis of Different CMOS Logic Design Techniques for Low Power and High Speed", International Journal of Advance Research in Electrical, Electronics and Instrumentation Engineering, Vol 2, Issue 10, October2013