International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 05 Issue: 03 | March - 2021 ISSN: 2582-3930

DESIGN AND IMPLEMENTATION OF A FIVE LEVEL INVERTER FOR REDUCTION OF SWITCHES AND REDUCING THD

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Abstract - Multilevel inverters have been widely used in industrial and electric vehicle derives because of their numerous advantages such as reduced total harmonic distortion (THD), lower voltage stress on switches compared to the classical two-level inverter. Also, multilevel inverters can operate with lower switching frequency compared to the classic two-level topologies. Recently, the single-phase multilevel inverters have become popular for low-voltage applications such as UPS, photovoltaic (PV) system. However, there are two main issues in these single-phase multilevel inverters: One is a large number of active switches, and another is neutral-point or flying capacitor voltage balancing problem. Use of large number of switches is the main drawback of conventional inverter designs. This paper presents a micro-controller based five level single-phase inverter design, using reduced number of switches i.e. six switches and lower THD. The design is simulated using MATLAB Simulink software.

Key Words*: *Multilevel Inverters, THD, MATLAB Simulink

1. INTRODUCTION

Multilevel inverters produce a step-wise waveform that has lower total harmonic distortion so it is close to sinusoidal waveform. A multilevel inverter is such an inverter that is used as an alternative to high power conditions and medium voltage in industrial applications. Nowadays some inverters have got much attention because of their structural characteristics in the electrical power industry. The purpose of using a multilevel inverter in industrial applications is to generate high output power from medium and low-voltage sources. Sources like batteries, super capacitors, and solar farms are medium or low voltage sources. One of the main features of the multilevel inverters is the improved output voltage and current quality in terms of harmonic distortions. The total harmonic distortion (THD) of the output waveform is reversely proportional to the number of output voltage levels. However, as the number of output voltage increases, the number of circuit elements as well as the conduction power losses increase. Therefore, the number of voltage levels is generally limited to five levels in most practical applications. Different five-level inverter topologies can be found in the literature. A new design of five-level voltage source inverter for high-power applications is presented in [1]. The proposed approach will make use of the redundancy switching states to balance the flying capacitor voltages in the proposed inverter. A Five-Level quasi Z-source (QZS) based neutral point clamped (NPC) for photovoltaic (PV) applications are presented in [2]. This inverter circuit is formed by integrating a dual quasi Z-source with a T-type arm and a diode clamped arm. Ref [3] proposes and analyses a 5-level inverter topology with a single DC source and a buck DC-DC converter in order to reduce the number of independent DC voltage sources. In the proposed topology, the specific input DC voltage is supplied through a single DC and a single-input single-output DC-DC converter. As the proposed topology uses a buck stage, one of the capacitors voltages, which is supplied by DC-DC converter, can be controlled. It is important to emphasize that the DC-DC converter used in the proposed topology is a partial-scale converter reducing its cost and size in comparison with the full-scale ones. A forward-mode five-level inverter is presented in [4] which combine the features of the conventional multilevel converters and forward topology. The converters can transfer high dc voltage into regulated sinusoidal voltage with low THD at arbitrary frequency. A comparative study between the two-level inverter and five-level inverter to convert super-capacitive energy for PMSM Load is discussed in [5]. In this context, super-capacitive sources are used as input sources to analyze the response of multilevel inverters to integrate with the super-capacitive energy storage devices in any system. The PMSM loads are used to compute the time response in the simulation environment. Numerical computational analysis of super-capacitive storage with different types of loads, to measure the response of five-level inverters that can be integrated with lightning energy storage systems is discussed in [6]. It shows the response of five level inverter connected with various loads as RL Load, Permanent Magnet Synchronous Machine Load and Grid. The five-level inverter has been integrated with super-capacitive storage to measure the response of inverter with super capacitor and also to measure the variation in super capacitor for various load. Paper [7] treats the design and realization of a new five-level single-phase inverter structure controlled by a microcontroller-based digital strategy. The proposed topology needs less number of switches and carrier signals and THD of the proposed topology is less compared to conventional topologies.

In comparison with conventional two-level inverter, multilevel inverter provides more than two levels of voltage to achieve high power, smoother and less distorted alternating voltage by using several semiconductor switches and lower level DC voltages as input. Among the available types of multilevel inverter topologies, the H-bridge multilevel inverter requires less number of power switching components, has higher efficiency and has simpler circuit layout. Paper [8] presents a five-level multilevel inverter with reduced switching count, discussing its design features which contribute to less switching losses and Total Harmonic Distortion for motor drives. A new single-phase five-level voltage source inverter (VSI) topology is developed in [9]

by using two-level unit and three-level unit with coupled inductor. The proposed topology can reduce the number of active switches as well as DC sources compared with the conventional single-phase five-level VSI topologies. A space vector pulse width modulation (SVPWM switching technique) is presented in [10] wherein a five-phase voltage source inverter (VSI in order to reduce THD and low order harmonics with fundamental voltage amplitude fixation). Subspace election for determination of switching time is based on smallest triangle which is surrounding the reference vector vertex. In this method, the zero vectors will be eliminated in large amplitude modulation index. Genetic algorithm (GA) is utilized in optimization process to find the best applying time sequence in switching pattern for minimizing THD and switching losses.

Paper [11] presents two control methods for single-phase five level inverter: staircase modulation (SM) and pulse width modulation (PWM). All control methods realize voltage balancing for the inverter capacitors. The control strategies presented for SM allow a minimal number of switching transitions from one state to another. The case when one capacitor is discharged in a half period and it is charged in the other half period and the other is charged in a half period and it is discharged in the other half period achieves minimal THD.

2. OVERVIEW OF MULTILEVEL INVERTERS

Multilevel inverters provide many advantages compared to the classic topologies such as lower voltage stress on switching devices and better harmonic content in the output voltage waveform. Also, multilevel inverters can operate with lower switching frequency compared to the classic two-level topologies and maintain the capability to provide output current waveform with less total harmonic distortion (THD), which has a positive impact on the energy conversion efficiency due to the decreased switching losses. Fig-1 shows the classification of multilevel inverters.

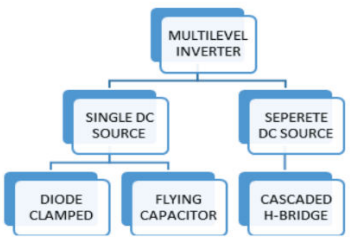


Fig-1: Classification of multilevel inverters

The most attractive features of multilevel inverters are as follows:

a) They can generate output voltages with extremely low distortion

b) They can operate with a lower switching frequency

c) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings

The most popular multilevel inverter topologies are diode clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), and Cascaded H-Bridge multilevel inverter (CHBMLI).

Diode Clamped Multilevel Inverter (DCMLI)

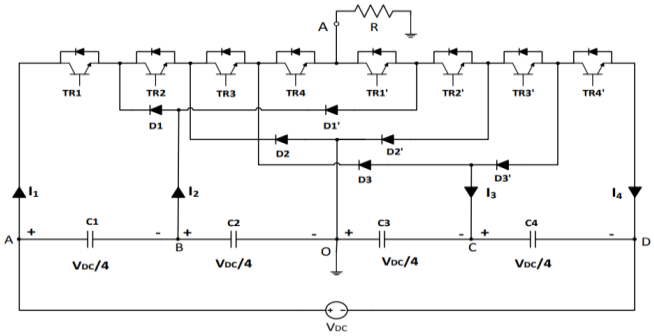


Fig-2: Five-level DCMLI leg topology

The five-level leg topology of DCMLI, depicted in Fig-2, is considered to investigate the capacitors' voltage imbalance problem. The operation of this power converter is based on the series connection of different number of capacitors with the load. When TR1, TR2, TR3, TR4 are conducting, the capacitors C1, C2 are connected in series with the load providing an output voltage with value equal to VDC/2. To obtain an output voltage with a value of VDC/4, the switching devices TR2, TR3, TR4, TR1' are turned on and the capacitor C2 is connected in series with the diode D1 and the load. Using the capacitors C3 and C4 correspondingly, the negative half-period of the multi-stepped waveform can be composed. [12]

Flying Capacitor Multilevel Inverter (FCMLI)

The five-level FCMLI topology shown in Fig-3 is deployed to study the non-desirable voltage distribution on the flying capacitors of the converter. By turning on switches TR1, TR2, TR3, TR4 the output voltage is equal to half of input voltage.

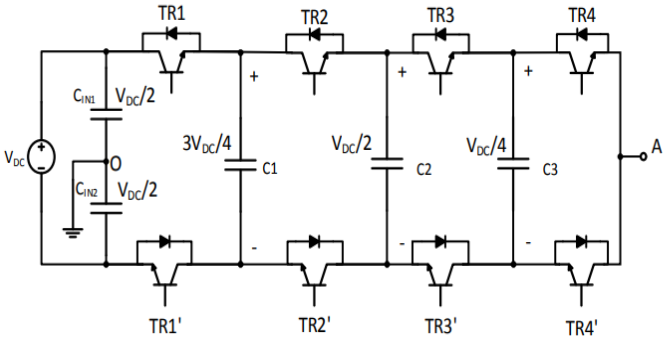


Fig-3: Five-level leg topology of a FCMLI and the output voltage waveform respectively.

To produce an output voltage with a value equal to (VDC/4) switches TR1, TR2, TR3, TR4' can be used (VAO=VCIN1-VC3), causing the charge of the capacitor C3. Another switching combination to produce the same voltage level is by turning on TR2, TR3, TR4, TR1'switches (VAO=VC1-VCIN2) causing the discharge of C1, or to turn on the switches TR1, TR3, TR4, TR2'(VAO=VCIN1+VC2-VC1) causing the charge of C1 and the discharge of capacitor C2. Switching patterns to produce

zero and the negative voltage levels can be acquired similarly, and they are mentioned in [12].

Cascaded H-Bridge Multilevel Inverter (CHBMLI)

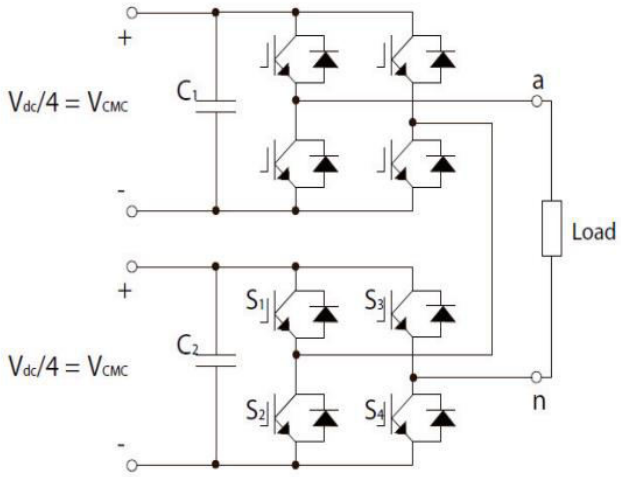


Fig 4: Circuit diagram of cascaded H-Bridge multilevel inverter

In H-bridge inverter it uses more than one DC sources. Every inverter generates output at different levels. The output voltage is the sum of all voltage levels generated by each cell. The number of levels in output voltage is = 2n+1 Where 'n' is the number of input sources. Especial feature of this inverter is that it requires lesser no of switches than diode clamped multilevel inverter. Fig-4 represents the circuit diagram of cascaded H-Bridge multilevel inverter [13].

3. LITERATURE SURVEY

Tekale Anil A. et al [2] states that a Five-Level inverter are gaining attention, exertion are being directed toward attenuating the device count for increased number of output levels. A novel topology for Five-Level inverter has been proposed in this paper to attenuate the device count. The operating principle of the proposed topology has been illustrated and mathematical formulations suiting to output voltage, source currents, voltage stresses on switches, and power losses have been eliminate. Comparisons of the proposed topology with existing topologies acknowledge that the proposed topology significantly reduces the number of power switches and associated gate driver circuits.

Durga Prasad G et al. [3]studied A symmetrical MLI with reduced power semiconductor devices has been discussed in this paper where the required number of levels can be easily achieved by duplicating one source, active and passive switch in LGM. The performance of the topology is trustworthy as it operates only one high frequency switch for each level generation. The topology is simulated to observe the performance for R, and RL loads; and the results show that the percentage THD reduces to an acceptable standard.

G. Lourds Sajitha and C. R. Balamurugan [4] examines the novel DC link coupled VL quasi Z source based reduced switch multilevel inverter. The proposed circuit has two combinations of switches that is low and high frequency switches. The VL Quasi Z Source inverter is connected in between these two switches. To analyze this circuit two references with PDPWM strategies with triangular carriers are used for generation of gate signal for switches. The proposed circuit is operated in three modes namely over modulation, under modulation and normal modulation region.

G. BhaskarRao et al [5] proposed a novel SC-based cascaded multilevel inverter. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation.

John N. Chiasson et al [6] studied how to reduce harmonic distortion for a multilevel inverters. In this paper, the seven level inverter scheme with harmonics reduction was demonstrated. The harmonic reduction was achieved by selecting appropriate switching angles. The functionality verification of the seven level inverter was done using MATLAB.

4. PROPOSED FIVE LEVEL INVERTER

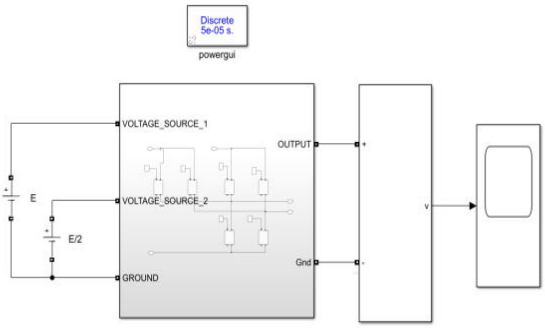


Fig-5: Block Diagram of a proposed five level inverter

This paper mainly focuses on designing a micro-controller based single-phase five level inverter. The system is simulated using MATLAB Simulink software Tool. Fig 5 represents the block diagram of proposed system. The converter consists of two DC sources E1 = 34V and E2 = E1 / 2 and 6 switches, each switch is composed of a MOSFET transistor and a diode; the MOSFET switches are used because of its fast switching capability.

Operation Mode:

The aim is to determine the values that can be taken by the output voltage 'Vab' for the different possible states of the static switches, and to show the sequences of the switches conductions 'ti'. For an N-level converter, we have N possible operating sequences to generate the N voltage levels. Particularly for five levels there are five sequences of operation. The connection function Fki translates the open or closed state of the switch ki :

Fki= 1 if k switches are closed

0 if k switches are opened

5. SIMULATION AND RESULTS

The proposed inverter power system is composed of six MOSFET switches. Each switch is controlled by the adequate pulse sequence in order to product wave voltage with five levels and of 50 Hz frequency. The input supply for each DC source is respectively 12V and 6V. The system is implemented in MATLAB Simulink environment. Fig 6 shows the waveform of the voltage obtained at the inverter output. Fig-7 illustrates the trigger signal of 6 MOSFET switches.

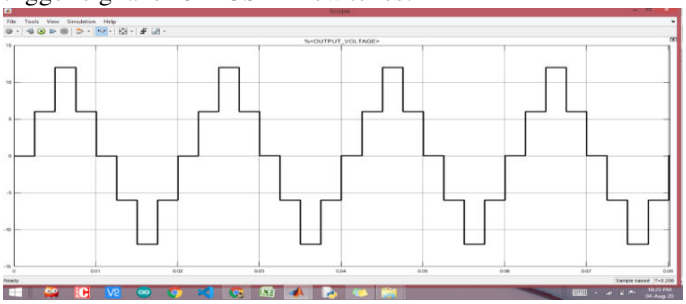


Fig-6: Typical output voltage waveform of a multilevel inverter

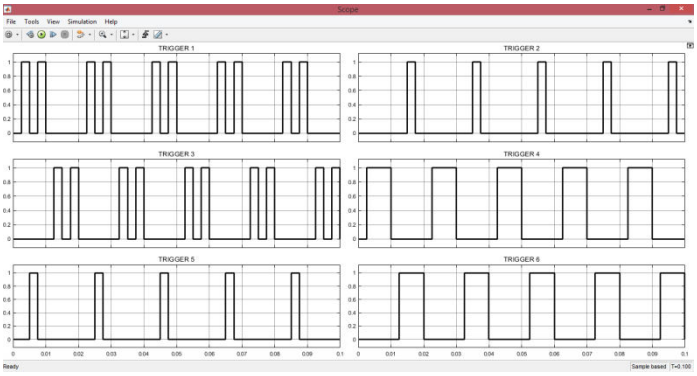
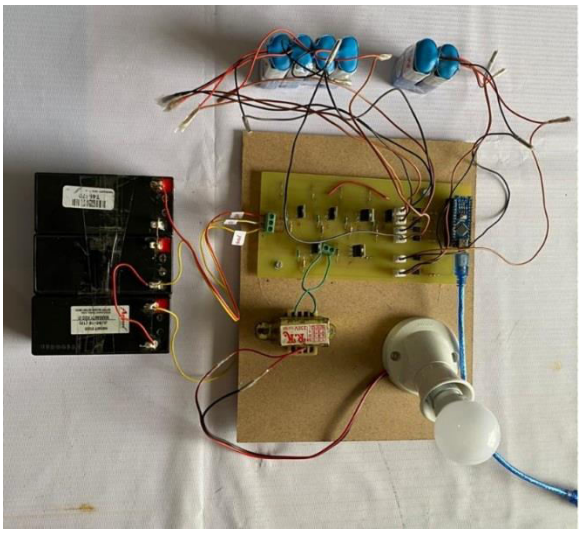
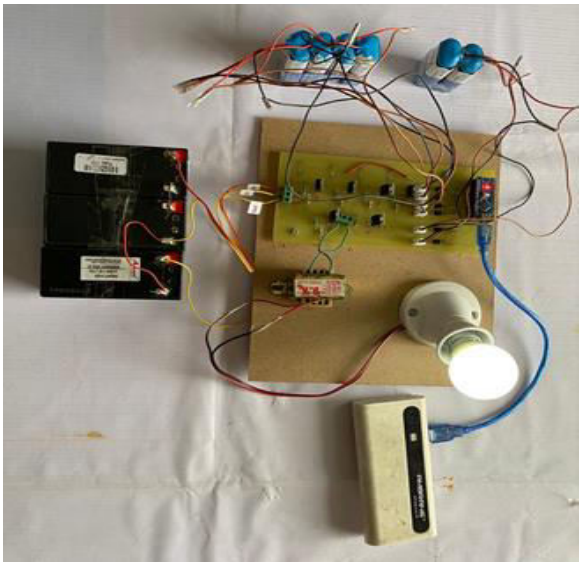


Fig-7: Trigger Output waveform

6. EXPERIMENTAL SET-UP



(a)Initial State without power supply connection



(b) After supplying power to controller circuit

Fig 9: Experimental Set-up of a proposed five level inverter.

7. CONCLUSION

Multilevel Inverters (MLI) are capable of providing limits to various parameters such as electromagnetic interference (EMI), total harmonic distortion (THD), Voltage stress on the switches and dv/dt problems etc. Multilevel inverters are now enhancing their horizons in variety of fields of applications. They are mostly preferred in industries for medium voltage (MV) and high voltage (HV) applications such as FACTS, HVDC, PV systems, EV, UPS and other industrial drive applications. A micro-controller based multilevel inverter topology is proposed in this paper. The software implementation of the five-level multilevel inverter is successfully completed with the help of control circuit in MATLAB Simulink tool. It is observed that the proposed topology is significantly successful in reducing the count of number of switching devices, capacitor voltage balancing, manufacturing cost etc. Simulation results conclude that a high-quality output voltage waveform is generated with lower order of THD. The proposed system design is also verified experimentally and the results are as stated above.

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