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DESIGN AND SIMULATION OF 1 BIT SIGMA DELTA ADC USING CMOS TECHNOLOGY

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Abstract: -This paper presents the design of a 1 bit sigma-delta analog-to-digital converter (ADC) which is realized using CMOS technology. Power consumption is major issue in VLSI design. An efficient low power first order 1 bit sigma Delta ADC will be designed and implemented using a standard n-well CMOS process. ADC is classified into Nyquist rates and over sampling ADC's. Design of 1 bit sigma Delta ADC consists of Op-amp. Op-amp is a key component in sigma delta ADC .Op-amp at Integrator stage and its open loop gain stage are combined together to form a 1 bit sigma delta ADC circuit.1 bit sigma Delta ADC will be implemented using Mentor Graphics tool .

KEYWORDS: ADC, VLSI, CMOS technology, Op-amp, Integrator.

SIMULATION TOOL: Mentor Graphics Tool.

1. INTRODUCTION:

Analog-to-digital converter (ADCs) very important building blocks in modern signal processing and communication systems. For signal processing, the digital domain is preferred over the analog domain due to its advantages such as noise immunity, storage capacity, security etc. In the long run, digital communications are more reliable because of the repetitive nature of the process. Because of this, today almost all modern electronic devices are digital operated, allowing for advanced digital signal processing (DSP). But real-world signals such as signals coming from various transducers are analog in nature. This analog signal should be converted to digital to allow digital signal processing.
Similarly after a signal is inserted into the digital domain, the signal is converted to analog. This is required for a speaker-like transducer. Digital to Analog Converter (DAC). Use of ADC includes DC instruments, process control, thermocouple sensors, modems, digital radio, video signal detection etc. The ADC should be installed at low power and high speed due to many reasons. Firstly the faster arrival of the battery operating system requires less power dissipation to increase battery life, as well as a smaller number of battery cells to reduce the volume and weight of the system. Another reason is the smaller feature sizes offered by today's VLSI technology.

We use analog to digital converter (ADC) because analog signals are difficult to store, difficult to transfer, difficult to process. Digitals signals are easy to store, easy to process and have less errors. The sigma delta conversion technique has been existence from many years, but recent technological advances are now making the devices are usable and their use has increased. Converters have found homes in applications such as consumer and professional audio, communication systems, industrial weight scales, and precision measuring devices.

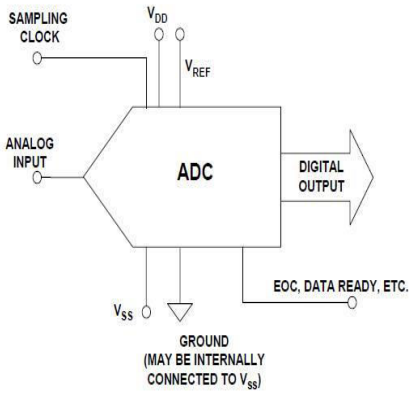

Figure 1. Basic ADC

Sigma-delta (Σ-Δ) ADC is now used in many applications where it costs low cost, low bandwidth, low power, high ADC resolution. An important feature of these converters is that they are the only low cost conversion system that offers both large flexibility and flexibility in converting low bandwidth input signals. They are perfectly suited for slow and medium-speed conversions such as instrumentation, digital voice and audio applications. Sigma delta (Oversampling) is aanalog to digital conversion based on the oversampling method. It uses high frequency and thus eliminates the need of anti-aliasing filters at the input to ADCs like Nyquist rate ADCs. Compared to other ADCs the Sigma-Delta ADC (Σ-Δ ADC) is simpler and easy to realised.

2. Types of ADC:

ADCs can be divided into two categories depending on the rate of sampling. The first category samples the input at the Nyquist rate, or fN = 2F where F is the signal bandwidth and fN is the sampling rate. The second type samples the signal at a rate much higher rate than the signal bandwidth. This type of converter is calledoversampling converter. The oversampling ADC is able to achieve higher resolutions than Nyquist-rate ADC.

Nyquist rate converters are used to generate a series of output values where each value has one to one correspondence with a single input value. However, it should be noted that Nyquist-rate converters are seldom used at the Nyquist rate due to the difficulty in realizing practical anti-aliasing and reconstruction filters. In most cases, Nyquist rate converters work from 1.5 to 10 times the Nyquist rate. Oversampling are those converters which operate faster than the Nyquist power output rate (typically 20 to 512 times) and increase the output rate (SNR) for input noise that is not in the signal range. In A / D converters, the filter is digital, whereas in D / A converters, an analog filter is used.For nonlinear ADCs, the analog sample is sampled and calculated at a frequency of samples higher than the Nyquist average, then the amplification noise from the quantizer will be spread evenly. Higher sample rate will result in lower signal amplitude power in signal bandwidth and consequently higher signal resolution. The delta-sigma ADC is the primary means of eliminating ADCs. By using the response logo on the module, the composing sound was created to reduce the amplitude of the signal in the signal range. Excessive control allows audio input to be performed in a digital domain but with high frequency.

A. Nyquist-Rate ADCs:

- Flash ADCs
- Sub-Ranging ADCs
- Folding ADCs
- Pipelined ADCs
- Successive Approximation(Algorithmic) ADCs
- Integrating (Serial) ADCs

B. Oversampling ADCs:

- Delta-Sigma based ADCs

Over sampling typically employ switched-capacitor circuits and therefore do not need sample and hold circuits. The comparator compares the input signal against its last sample, to see if the new sample is larger than the last one. If it is larger, then the output is increases and if it is smaller, then the output is decreases. Since the Greek letter-Δ (delta) is used to indicate deviations or small incremental changes, the process is known as "delta modulation".

Delta modulation is based on measuring the change in signal from sample to sample rather than the absolute value of the signal in each sample. Sigma stands for summing or addition, which is performed at the input stage on the digital output with the input signal before the delta modulation. Therefore this digital conversion analog of this method is called “Sigma-Delta modulation”.

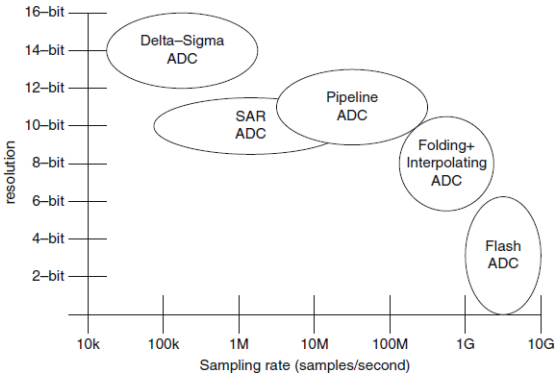

Figure 2. Comparisons of all ADC’s according to resolution (bits) and sampling rate (samples/s)

3. PROPOSED SYSTEM:

The diagram shows a block diagram of the 1 bit sigma delta ADC. It consists of Integrator, Comparator (1 bit ADC), D-latch, 1 bit DAC. In the above circuity, 1 ADC (commonly known as Comparator), drive it through the integrated output, and then feed the compiler with a separate split output output of 1 DAC from the D-latch output.

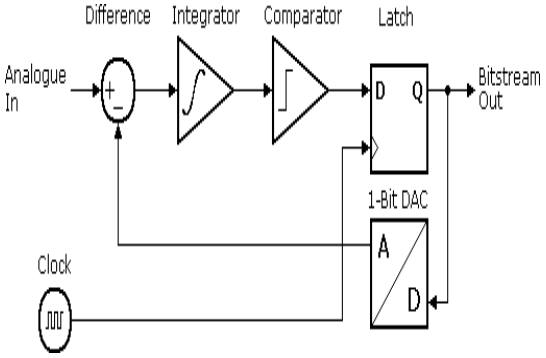

Figure 3. 1 bit sigma delta ADC implementation

4. Circuit diagram:

The integrator is simple Miller integrator using a large resistor and a small capacitor to reduce the layout space. The resistor and capacitor values determine the time

constant.The constant should not be too large. Otherwise, the integrator will enter the saturationstate. The Op-amp is a core part of the sigma delta converter. It provides a large open loop gain to be properly integrated. The output of integration feeds to the input of a comparator referenced to ground to quantize the signal to VDD or VSS. This output is fed to a D flip-flop, which includes the delay required to close the cycle. The results of this are applied to the DAC reference level change which converts this back to the dynamic input signal range. The DAC operates from the output of the Q and Q bars of the flip-flops.

5. Op-amp Design:

The integral operational amplifier of the integrator must have a high gain to achieve a smooth integration and bandwidth large enough to support the high frequency sine wave we will integrate. The op-amp operates at the clock frequency, since the difference are being integrated over the region of time. Therefore, the gain bandwidth product of the op-amp must be greater than one at the clock frequency to efficiently pass the signal. The amplifier used is shown below. The key thing to note to about the amplifier is the frequency compensation network which is used to push the high frequency zero out of the pass bass of the op-amp.
The integrator is designed using a two stage op-amp, the op-amp integrator is an operational amplifier circuit which performs the mathematical operation of integration. It acts like a storage element which produces an output voltage proportional to the integral of its input voltage with respect to time. It is connected with a feedback capacitor which helps in charging of the input voltage to give integrated output.

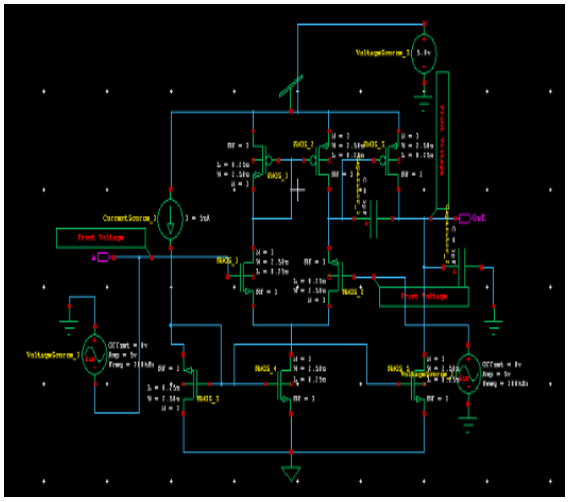

Figure 4. Integrator Design using CMOS

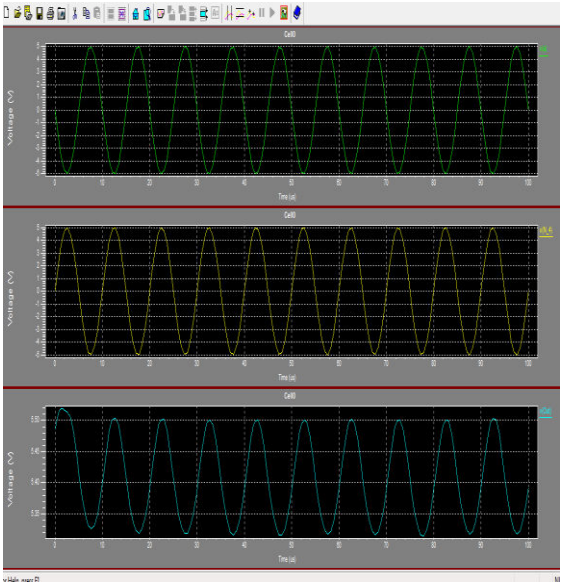

Figure 5. Waveform of Integrator

6. Comparator Design:

A comparator is a circuit that performs the operation of comparing two analog input signals and decoding the difference in to a single digital output signal. The comparator is one of most critical parts of almost all analog to digital (ADC) converters. Depending up on the size and structure they can have a severe impact on the device. The speed and resolution of an ADC is directly affected by the input offset voltage, delay and input signal range.
The design of comparator is similar to that of an op-amp. The only difference is the use of the compensation network consists of resistors and capacitor and extra multipliers on a biasing NMOS device. The comparator does not used the compensation network because sit's only function to switch from rail to rail. When a sinewave is input to the circuit, the comparator switches from positive rail to negative rail.
The comparator is simulated using a sinusoidal input signal to the differential pair in its one terminal and making the other terminal as ground. Here the analog signal input signal is compared against last sample signal to see if it is higher than the reference or not. If it is larger the output is increased or else decreased. The density of '1s' and '0s'and '0s' forming a pulse stream at the output is the digital representation of the input analog signal.

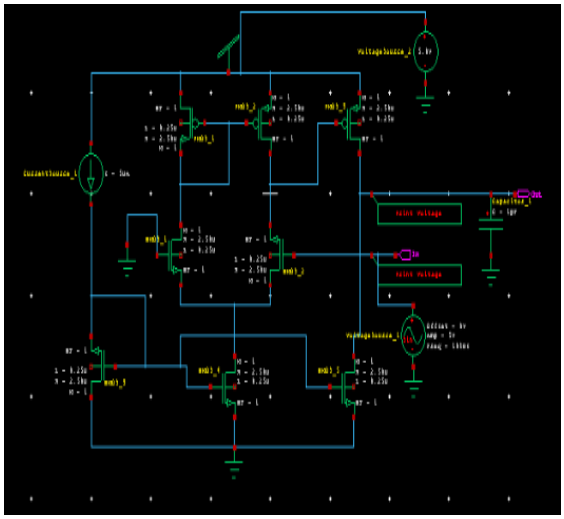

Figure 6. Comparator Design using CMOS

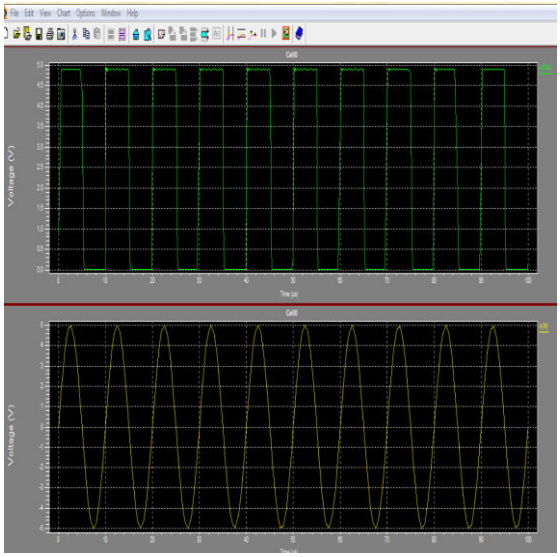

Figure 7. Waveform of the Comparator

7. Flip-Flop Design:

The D flip-flop is compose of two D latches arranged in a master-slave configuration. Each D latch consists of a pair of transmission gates and a pair of inverters. The outputs Q and Q bar are taken off the outputs of the second D latch B and B bar respectively. The clock frequency of D flip-flop decides the sampling rate. In this case D flip-flop operates on 5MHz.

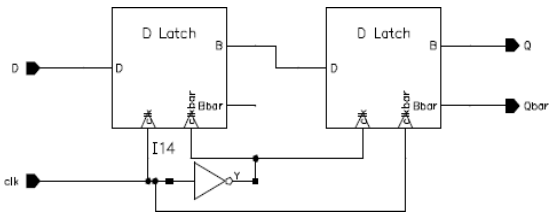

Figure 8. D flip-flop

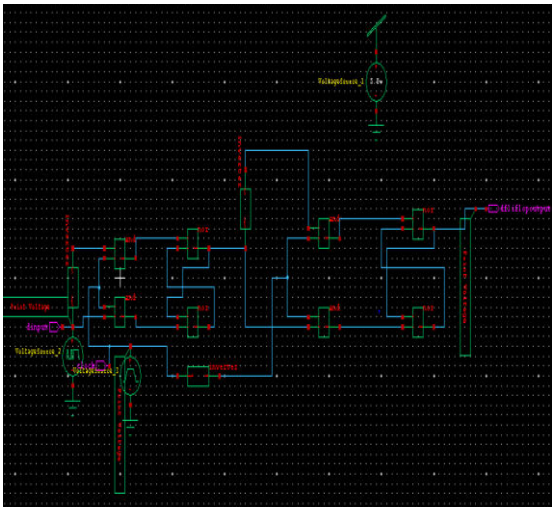

Figure 9. D flip-flop Schematic

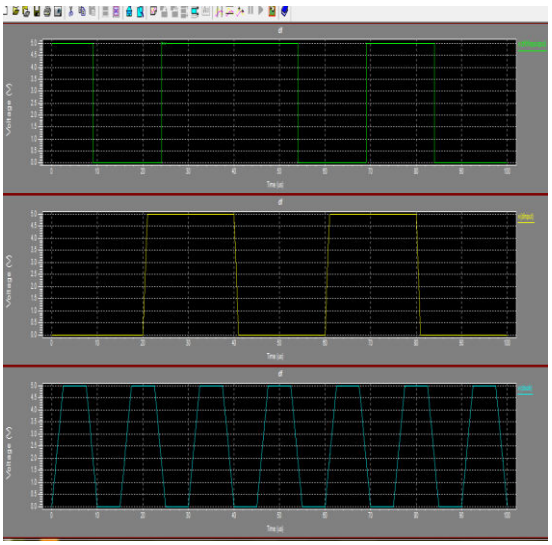

Figure 10. Waveform of the D flip-flop

8. 1 Bit DAC Design:

The DAC consists of a pair of transmission gates and two pairs of resistors. The input to each transmission gate is a voltage divided down from positive and negative 2.5 volts rails that acts as ±Vref signals according to the digital input signal. Through sigma delta modulator operation, the DAC receives a square signal from the flip-flop. In the response mode, the DAC adjusts the sensitivity level so that the response name corresponds to the input level of the input which makes the difference evenly weighted.

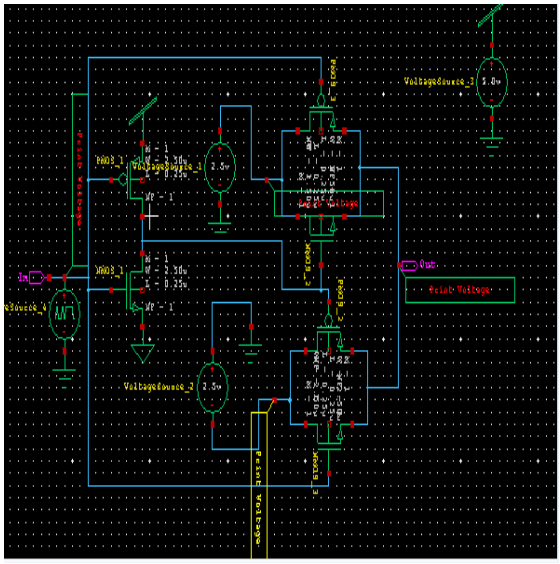

Figure 11. 1 Bit DAC schematic

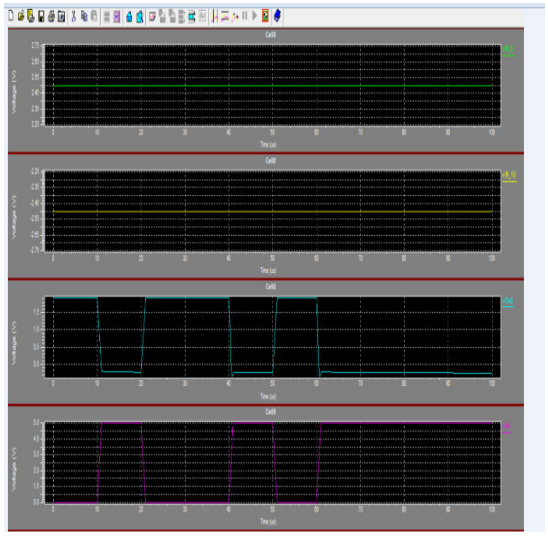

Figure 12. Waveform of 1 Bit DAC

9. Simulation Results of 1 bit Sigma Delta ADC:

The circuit design of 1 bit sigma delta ADC have been developed and implemented by using 0.18um CMOS technology. The whole 1 bit sigma delta ADC system works very well under the following conditions.

Input sine wave frequency up to 10KHz

Clock frequency (D-Latch) 5MHz

The output signal of a converter is a pulse density waveform. Figure shows input and output waveform of 1 bit sigma delta ADC.

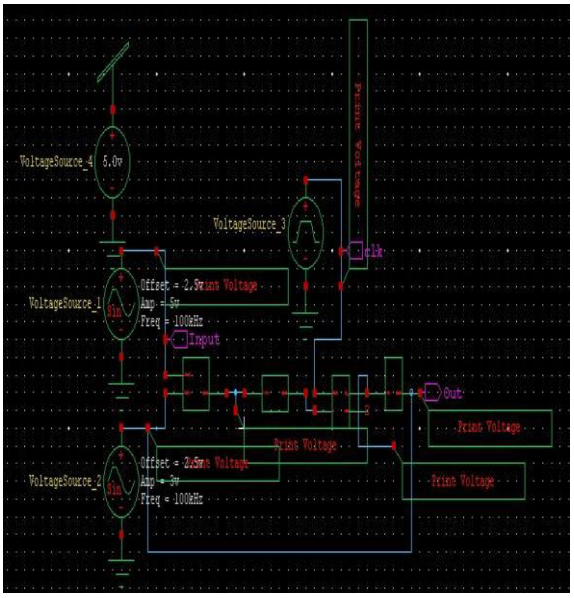

Figure 13. 1 Bit Sigma Delta ADC schematic

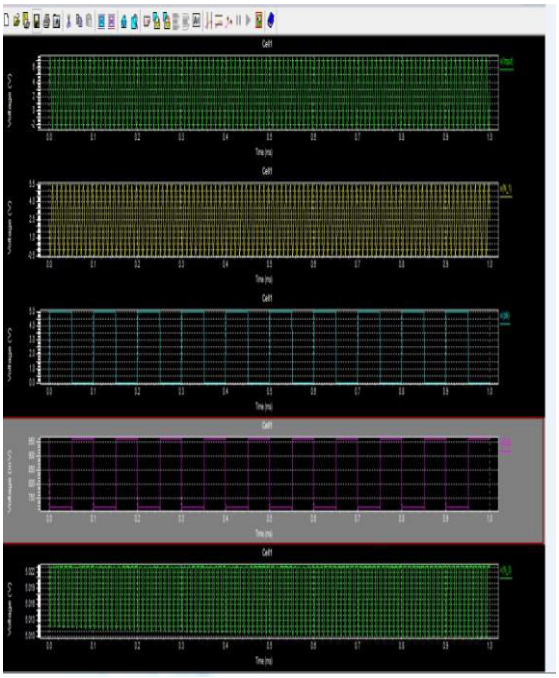

Figure 14. Waveform of 1 Bit Sigma Delta ADC

10. Results:

The designed circuit consists of Integrator, Comparator, D flip-flop, 1 bit DAC. The reference voltage is 1.8V.

This table shows the parameter of ADC in this work

Process used	0.18um
Supply voltage	1.8V

Clock frequency	5 MHz
Power consumption	1.59nw

Table 1. Parameter of ADC

11. Conclusion:

In present work, An 1 Bit Sigma Delta ADC (analog to digital converter) has been designed and simulated in a standard 0.18um CMOS technology in Mentor graphics tool to obtain accurate results. Considering all the output parameters in the limit we have designed the 1 bit sigma delta ADC which consumes less power.

Comparison of SAR ADC and 1 Bit Sigma Delta ADC

TYPE OF ADC / PARAMETER	SAR ADC	1 BIT SIGMA DELTA ADC
PROCESS USED	0.25um	0.18um
SUPPLY VOLTAGE	2.5V	1.8V
POWER CONSUMPTION	69.594uw	1.59nw

Table 2. Comparison of ADCs

12. References:

[1] “R. Jacob Baker, Harry W. Li and David E. Boyce, CMOS Circuit Design, Structural Planning,

and Simulation. New York, NY: Wiley-IEEE Press, 1997”chapter 29, pp-790-854

[2] Max W. Hauser, "Principles of A / D Conversion," Journal Audio EngineeringSocietyVol.39No.1 / 2, January / February 1991, p. 3-26.

[3] P. E. Allen and D. R. Holberg, Design of the CMOS Analog Circuit, 2nd edition, Oxford University Press, 2002.pp.270-280,453-454

[4] “Sigma-Delta Modulator” by Jeremy Ferris, Alfred Blais, University of Maine. www.eece.maine.edu/vlsi/Fall_00/SDM_547_Final.pdf

[5] Walt Kester, Analog-Digital Conversion, Analog Devices, 2004, ISBN 0-916550-27-3

[6] "ADC Architectures" http://www.springer.com/978-90-481- 8651-8

[7] Ngspice Tool Tool 21 by Paolo Nenzi, Holger Vogt Ngspice homepage http://ngspice.sourceforge.net/

[8] The design and simulation of the Active Access Register for A / D Converters using 0.18um CMOS Technology Kalmeshwar N. Hosur, Girish V. Attimarad.