International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 05 Issue: 04 | April - 2021 ISSN: 2582-3930

Design and Simulation of Low Data Rate Burst Transceiver for SATCOM

Anantha Padmanabha[1], Dr N N S S R K Prasad[2], Vinod L Kannur[3]

[1]*CEMILAC, DRDO, Bangalore*
[2]*Aeronautical Development Agency, Bangalore*
[3]*Alpha Design Technologies Pvt Limited, Bangalore*

Abstract -The Airborne radio communication system via satellite is referred to the term 'SATCOM'. All military aircraft including fighters are likely to be equipped with software Defined Radio (SDR) as onboard communication system with SATCOM as one of the channels. It supports both voice & data in UHF band. MIL-STD-188-181A, "interoperability standard for satellite communication" establishes the mandatory requirements for satcom system design. In satcom, digital data are transmitted and received in short bursts known as burst mode and data rate is usually as low as 2400 bps & 4800 bps. This burst transceiver design has additional complexities as compared to conventional modem design. In Burst modem, the carrier lock has to happen every time the burst data appears. The synchronization block will get very limited time to achieve lock (acquisition) per burst. Especially short bursts impose necessarily short acquisition periods. This paper describes the design & simulation of whole transceiver that includes, transmitter, channel & the complete receiver chain that includes coarse carrier recovery, fine carrier recovery, timing recovery, phase ambiguity resolution & demodulator blocks. In the proposed low data rate burst transceiver design, BPSK, QPSK, and offset QPSK modulation schemes are employed The BER for each of the modulation schemes are compared & results are presented

Key Words: SDR, Burst, BPSK/QPSK/OQPSK, CFO, Burst Receiver, BER, E_b/N_0.

1. INTRODUCTION

In satellite communication, digital data are transmitted and received in short bursts known as burst mode. The burst transmission employs the data packetized for a specific length which is encoded, scrambled and applied with error correction techniques to overcome the errors at the receiver. For receivers to detect the frame and decode data correctly synchronization is an important technique, Unique Word is inserted at the start of each packet so that the receiver gets synchronized by correlation technique.

The Ultra High Frequency (UHF) satellites used for military communications have hard–limiting transponders. These hard-limiting features preclude the use of any amplitude modulation scheme by forcing the modulating signals to have a constant envelope. Therefore, modulation should be either frequency or phase modulation. Accordingly in the proposed burst low data rate transceiver design BPSK, QPSK, and offset QPSK modulation schemes are employed

The data packets are serialized and modulated with Binary Phase Shift Keying (BPSK) modulation, Quadrature Phase Shift Keying (QPSK) and offset Quadrature Phase Shift Keying (OQPSK) at three different simulation stages. The modulated baseband signal is up converted to UHF carrier frequency and transmitted over the medium during the implementation. This paper is restricted to design and simulation only.

The receiver section carries out the coarse recovery, fine carrier recovery, timing recovery and phase ambiguity recovery prior to demodulation of the received signal. The Feed Forward (FF) carrier offset recovery and symbol recovery algorithms are used to get the data bits from the baseband symbols. The bits are correlated to find the Unique Word and the packet is formed by removing the phase ambiguity. The packet is decoded by Forward Error Correction (FEC) decoder to detect and correct any errors induced over the channel. The decoded data packet is descrambled and decoded to get the original packet

2. BASIC ARCHITECTURE OF TRANCEIVER DESIGN

The Fig.1 below shows the Simulink blocks of low data rate BPSK modem with Burst mode. Transmitter, Channel and Receiver are major sections. The architecture remains same for BPSK, QPSK and OQPSK. Contents of each section of the transceiver are discussed in the subsequent paragraphs.

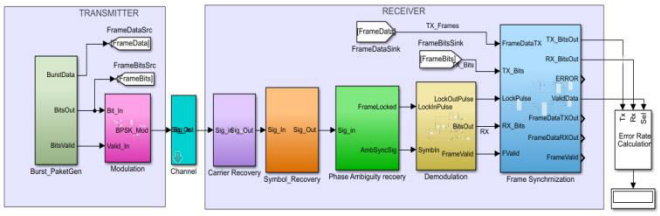

Fig-1: Simulink block diagram of low data rate burst mode BPSK transceiver.

2.1 TRANSMITTER SECTION

Transmitter section consists of burst packet generator & BPSK, QPSK, OQPSK modulator. The transmitter section has the following blocks. Following table 1 shows the specifications of the modem.

Table 1 Burst MODEM Specification

Sl.No	MODEM Parameter	Value
1	Bit rate	2400 bits/sec
2	Interpolation	8
3	Sample rate	19200 Ksps
4	Noise (SNR)	0 to 12dBm
5	Frequency Offset	+/- 4 KHz

2.1.1. Burst Packet Generator: This block generates burst packets. The Figure.2 depicts the burst packet structure. The Figure.3 shows the burst and the inter burst gap duration for the transceiver waveform. The bit rate of the burst packet is 2400 bits/sec. The payload data is stored in a buffer which is appended with the Flag field and preamble (CR, BTR, UW) fields. The specification of each field is shown in table-2.Total Packet is converted to serial before modulating in the next module.

Table-2: Burst Packet format

Sl No	Parameter	Value
01	Data rate	2400 bits/sec
02	Carrier Recovery(CR) Bit Time Recovery (BTR)	30 Bytes.
03	Unique Word (UW) Length	02 Bytes.
04	Flag Length	02 Bytes.
05	Pay Load Length	124 Bytes.
06	Burst Packet Length	0.5267 sec.
07	Inter Burst Gap	0.533 sec.

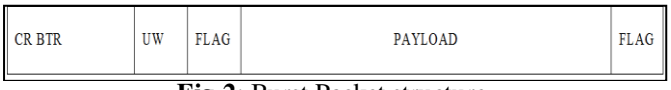

Fig-2: Burst Packet structure

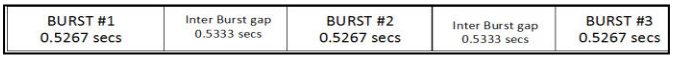

Fig-3: Burst Packet with inter burst durations.

PREAMBLE (CR, BTR, UW):

CR, BTR: Carrier recovery (CR) bits is the sequence of bits in each burst packet. Burst acquisition time at the receiver is decided by the CR bits length, which is the most critical part of the receiver. The receiver must recover the carrier signal in the presence of frequency offset within the CR bits duration. The CR field contains a sequence of bits (all 1's or 0's). Bit Timing Recovery (BTR) is the sequence in the preamble. The timing recovery (symbol recovery) of the recovered symbols should be attained within this duration at the receiver.

UW: Unique word is a sequence of bits that follows the carrier and Bit timing recovery sequence (CR, BTR) of bits in the preamble. The unique word bit sequence in the burst packet provides a timing reference on the occurrence of the burst start and also provides a timing marker to allow the receiver to extract their part of the traffic burst. The timing marker allows the identification of the start and finish of a message in the burst and helps to correct decoding. The unique word should have a high probability of detection. The phase ambiguity is also corrected by using UW pattern.

2.1.2. Modulator: The packets received are modulated using one of the modulation schemes i.e BPSK, QPSK, OQPSK in this module. The serial bits are modulated and In-phase & Quadrature symbols are generated. These symbols are having a step transition which generates infinite bandwidth. So as to avoid this, we will make the transition smooth by inserting more samples per symbol and filtering using Square Root Raised Cosine (SRRC) Filter before transmitting to channel. The Modulator block is shown below, which includes the BPSK/QPSK/OQPSK modulator and SRRC Filter.

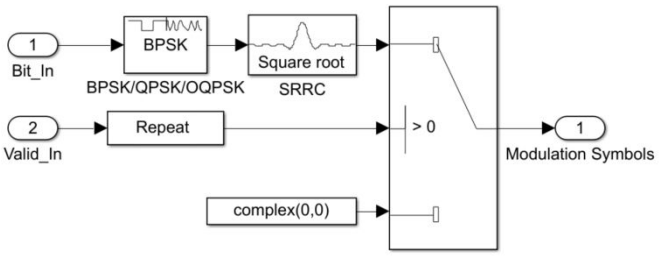

Fig -4: Modulator with Interpolation and Filtering.

BPSK Modulation: In BPSK, two phases are possible for the carrier. One phase represents logic1 and the other phase represents logic 0. As the input digital signal changes state (i.e., from logic high to low or from logic low to high), the phase of the output carrier shifts between two angles that are separated by 180.

QPSK Modulation: The Symbol Mapping subsystem uses the QPSK Modulator Lookup table in order to map the two bit input value [0,1,2,3] onto the appropriate complex valued symbol [1+1i, -1+1i, 1-1i, -1-1i] respectively. Mapping (Grey) the symbols in this manner allows for a 2 bit value to be used to represent each symbol.A QPSK modulator is a binary (base 2) signal, to produce four different input combinations: 00, 01, 10, and 11. Therefore, with QPSK, the binary input data are combined into groups of two bits, called dibits. Each dibit code generates one of the four possible output phases (+45°, +135°, -45°, and -135°).

OQPSK Modulation: Offset-QPSK (OQPSK) is widely employed in satellite communication and it is also one of the requirements of MIL-STD-188-181B.In this modulation scheme, I and Q channels are misaligned by one another by half a symbol time interval Ts/2=Tb, so that abrupt phase change of 180° is eliminated. Hence, phase trajectories passing through the origin of the constellation diagram is avoided. This makes the OQPSK signal less sensitive to non-linear amplifier impairments.

The following table summarizes digital modulations developed. With M-ary digital modulation, even more symbols are used (so there is more bits/symbol).Table-3 shows the parameters of the schemes developed.

Table-3: PSK Modulation scheme parameters

Modulation	# Symbols (*M*)	# Bits/symbol ($N=\log_2 M$)	Bandwidth (*BW*)
BPSK	2	1	$2R_{sym}= 2R_b/N=2R_b$
QPSK	4	2	$2R_{sym}= 2R_b/N= R_b$
OQPSK	4	2	$2R_{sym}= 2R_b/N= R_b$

Interpolation and Pulse Shaping:

The Pulse Shaping component uses an FIR Interpolation filter, featuring an up sampling factor of Eight, and a Square Root Raised Cosine (SRRC) impulse response shown in Figure-5. To avoid bandwidth spreading over large span the signals are passed through RRC filter. The output signal will have finite bandwidth after the filtering.

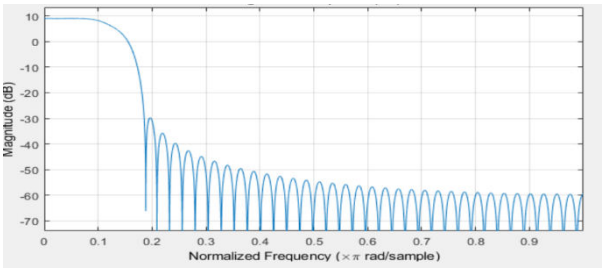

Figure-5: Transmitter SRRC Filter response.

Table-3: Transmitter SRRC Filter parameters

Sl.No	Filter Parameters	Type/Value
1	Modulation type	BPSK/QPSK/OQPSK
2	Interpolation rate	8
3	Filter used	FIR based SRRC
4	Roll off Factor	0.35
5	Filter Span	10 Symbols

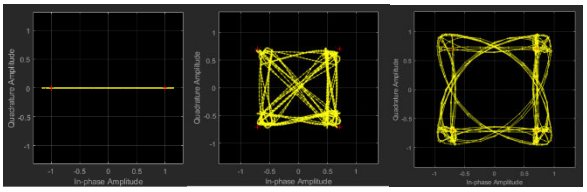

Figure-6: Constellation for BPSK, QPSK, OQPSK

2.1.3. Channel: In the current design, the channel considered is AWGN with large frequency offsets. The Transmitter section sends the modulated signals over the channel, which is a wired/wireless medium. In this scenario we have introduced Phase and Frequency offset to the modulated signal in the channel. The Noise induction is varied and results are plotted for Bit Error Rate (BER) measurement. The maximum Frequency offset introduced is +/- 4KHz.

2.2. RECEIVER SECTION

The receiver module would perform Burst detection from the channel, then carrier recovery, symbol recovery, phase ambiguity recovery, demodulation, frame synchronization and BER measurement. Each of the blocks is explained in the subsequent section.

2.2.1. Burst Detection: The received baseband signal is checked for Burst detection, which is implemented here as a simple energy threshold mechanism, where in, the input signal energy is is calculated. When it rises above a certain threshold, which is determined statically or dynamically, samples are captured and tagged as a burst. The detection works for the various levels of noise. We can compare the technique to Receiver Signal Strength Indicator algorithm which also indicates the signal strength.

$$InputSignalPower = \frac{[absolute(RxSignal)^2]}{2}$$

2.2.2. Matched Filter: Matched Filter (MF) produces an output in such a way that, it maximizes the Signal-to-Noise Ratio (SNR) in the presence of noise. The MF decimates the incoming samples by 4, which makes the sample rate after the matched filter at 4.8 kbps. In the proposed design, we have split the task of pulse shaping equally between the transmitter and the receiver. Accordingly, the SRRC filter is used at both the transmitter and the receiver. This way, the product of the two filter responses will result in an overall Raised-Cosine response with zero ISI.

2.2.3. Carrier Recovery: Carrier frequency offset occurs when the local oscillator of the receiver does not synchronize with the carrier signal of the transmitter. All receivers exhibit a frequency offset compared to the transmitted frequency. In case of low data rate applications, the frequency offset is a critical parameter which needs to be found and compensated by the receiver. The magnitude of the frequency offset may vary for each transmitter and receivers. In some scenario the frequency offset of the received signal may go above the capacity of the receiver carrier recovery limits. In such cases we need to employ additional techniques to compensate the offset present in the signal. The carrier recovery is divided into coarse and fine carrier recovery stages.

Coarse carrier recovery: Fast Fourier Transform (FFT) base Carrier Frequency Offset (CFO) estimation is carried out to find the frequency offset. The signal is transformed to frequency domain to find frequency. To estimate the frequency offset, FFT is calculated and index of the maximum amplitude across the frequency band is found and its index is used to find the peak frequency present in the input frame within the acquisition duration. The equation to find the frequency offset using the FFT based estimation is,

$$\text{FreqOffset} = \text{Index of Max Amplitude} * \frac{Rx\ Sampling\ rate}{\text{FFT Length}}$$

Index of Max Amplitude is the index of FFT output where the maximum amplitude peak has appeared.

FFT Length is the FFT order at which the FFT is processed.

Rx Sampling Time is the sampling rate of the input samples fed to FFT block.

The estimated frequency offset value is converted to phase increment parameter for the configurable Direct Digital Synthesizer (DDS).The phase increment value is used to generate the complex sinusoids and the receiver signal is multiplied. The phase increment value is calculated by the following equation.

$$PhaseIncrement = \frac{(RequiredFreq) * 2^{phasewidth}}{FrequencyInput}$$

Phase width is value of DDS accumulator bits. Frequency input is at which DDS is clocked. Required frequency is fed by estimation parameter.

Fine Carrier recovery: The purpose of Fine Carrier recovery module is to compensate for the Phase offset and Frequency offset which remains even after the coarse carrier recovery. The carrier recovery is PLL based algorithm which consists of a PLL, PED, NCO and a multiplier. The Carrier recovery implements a phase-locked loop (PLL) to track the residual

frequency offset and the phase offset in the input signal. A maximum likelihood Phase Error Detector (PED) generates the phase error. The tunable proportional-plus-integral Loop Filter, filters the error signal and then feeds it to DDS block. The DDS generates the compensation frequency which nullifies the offset when we multiply with the input signal.

2.2.4. Symbol Recovery: The aim of symbol recovery is to recover the optimal sampling moments for the data symbol detection. The powerful feed forward (FF) estimators for symbol timing recovery has been chosen for efficient acquisition since it is a burst modem. The Timing recovery subsystem implements a PLL to correct the timing error in the received signal. The zero crossing Timing Error Detector (TED) has been used to detect the timing errors. On average, the Timing Recovery subsystem generates one output sample for every two input samples.

2.2.5. Phase Ambiguity recovery: This block corrects any phase ambiguity present in the signals. The BPSK received signal has 180° phase ambiguity, whereas QPSK and OQPSK introduce 90° phase ambiguity. To correct the ambiguity, the UW is inserted for every packet. The preamble is tested for the phase changes and test results are compared with the ideal preamble phase. With the difference in the ideal and received preamble phases the phase shift is known. The conjugate value of phase shifted value is multiplied with the incoming frame by that the ambiguity is compensated.

2.2.6. Demodulation: The symbols received after the phase recovery is used for symbol to bits conversion which is done using demodulator. In this paper, we have tested three modulation schemes BPSK, QPSK and OQPSK at the transmitter. In the receiver block, the respective demodulator is used for demodulation. The incoming Real and Imaginary channels are fed to this demodulator, where the magnitudes of the signals are compared with the Lookup table values. For BPSK [1 -1] are mapped to binary [0 1]. In QPSK and OQPSK Lookup table values are [1 + 1i, -1 + 1i, 1 - 1i, -1 - 1i], If the quantized input matches the table values then [0,1,2,3] binary outputs are generated respectively.

2.2.7. Frame Synchronization: The frame synchronization module will detect the unique word in the incoming data traffic by correlation. Once the correlation results of preamble are above the expected threshold value, then the data is considered as required data. The required data is then supported with a valid signal, by which packets are identified and the unwanted data is removed from processing. The required data is sent to rate transition management unit.

3. SIMULATION RESULTS AND DISCUSSIONS

Various Simulink models were developed using MATLAB /SIMULINK R2018b for the characterization of complete transceiver. Burst packets were generated at the transmitter and modulated with BPSK/QPSK and offset QPSK with matched square root raised cosine filters used both at the transmitter & receiver. The channel is added with AWGN in addition to large frequency offsets. The receiver section starts with coarse carrier recovery wherein coarse frequency compensator is introduced to compensate for coarse frequency offsets followed by fine carrier recovery. Frequency offsets up to 4000 Hz has been verified. The performance of each modulation schemes is verified through measurement of BER and the same has been compared with the theoretical BER. The results are comparable with satisfactory results. At the end, all the three modulation schemes are compared through their respective BER calculations & the combined plot is appended.

Simulation result 1

Figure-7 shows the Burst packet generation at the transmitter. Waveform at row-1, shows the packet in byte format, row-2 shows the burst valid signal, row-3 is the burst packet in bit format and row-4 shows the burst valid signal for the burst at bit format.

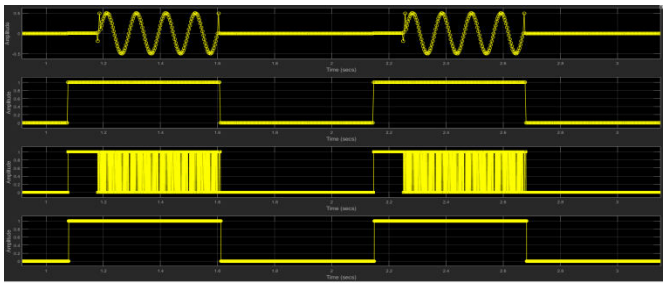

Fig -7: Burst packet generation at transmitter

Simulation result 2

Figure-8 shows the Burst packet at the BPSK modulator block at the transmitter, waveform at row-1 shows the valid signal for the modulated burst, row-2 shows the BPSK modulated symbols for the burst data, row-3 and row-4 are the burst signal after interpolation and filtering by SRRC filter.

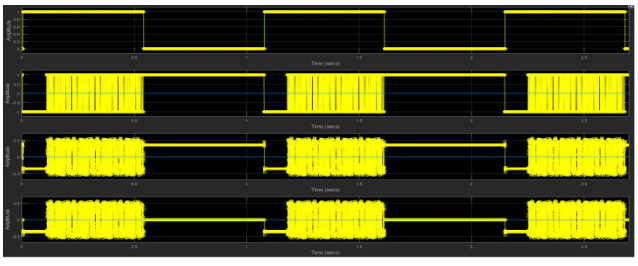

Fig- 8: Burst packet at BPSK modulator

Simulation result 3

Figure-9 below: Row-1 shows the transmitted signal after modulation and interpolation. Row-2 shows the signals after channel with phase, frequency offset induced in the signal.Column-2 shows Constellation after the phase, frequency impairments.

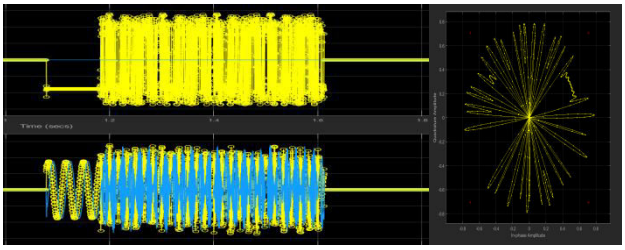

Fig -9: Burst packet at channel block

Simulation result 4

Figure-10 below: Column1- signals at row-1 shows the received signal after channel, row-2 shows the signals after MF block, row-3 shows the signals after Carrier recovery block and row-4 shows signals after Timing recovery block.

Column2 - signals at row-1 shows the signal after PA recovery, row-2 shows the signal frame lock once packet is detected at receiver, row-3 shows the signals after BPSK demodulation and row-4 shows valid signal for the burst demodulated signal at receiver.

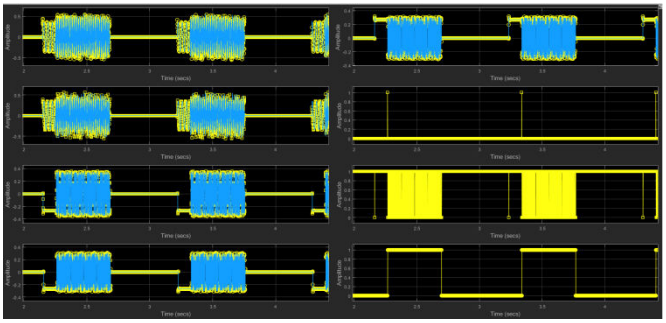

Fig -10: Burst signal at Receiver block

Simulation result 5:

Figure-11 shows the signal comparison and finding errors at the receiver block. The waveforms are similar for all modulation schemes.

Column1: signals at row-1: shows the valid signal for the received burst signal, row-2 shows the bits at transmitter, row-3 shows the bits at the receiver, and row-4 shows error between the transmitted bits and received bits.

Column2: signals at row-1: shows the valid signal for the received burst signal, row-2 shows the byte data at transmitter, row-3 shows the byte data at the receiver, and row-4 shows error between the transmitted byte data and received byte data.

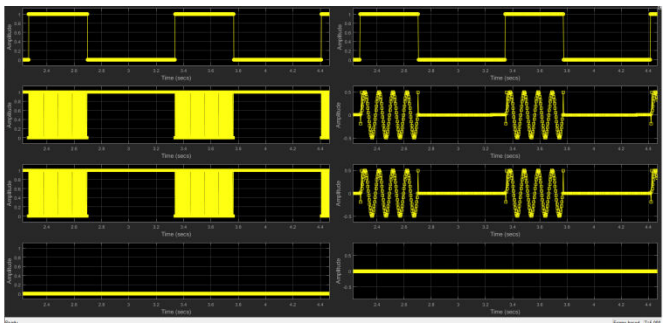

Fig- 11: Error detection bit & byte format.

4. BER MEASUREMENT

The BER curve is plotted for BPSK/QPSK and OQPSK results and compared against theoretical values. It has been found that simulation design of Burst modem performance is very close to theoretical values in presence of noise and frequency offset of +/-4K Hz.

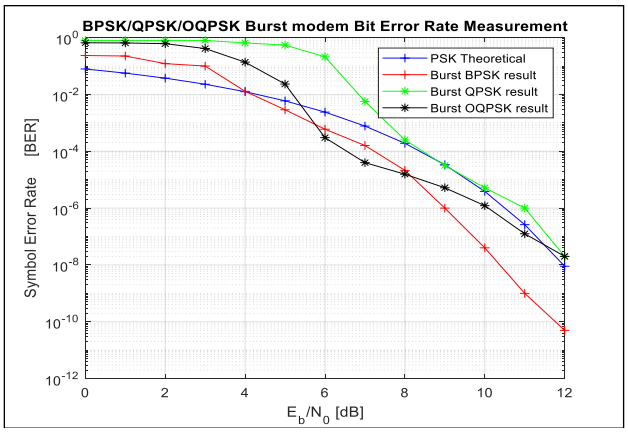

Figure -12: BER comparison: BPSK/QPSK/OQPSK

5. CONCLUSIONS

This paper describes, the model-based design & simulation of low data rate burst transceiver proposed for the SATCOM application. The performance metrics indicated by BER curves for the various modulation schemes simulated indicate that, the simulated output is close to the theoretical values. The system has successfully captured the burst with large frequency offsets of up to +/-4 kHz. In continuation with these efforts, with HDL code development, implementation will be taken up on FPGA.

ACKNOWLEDGEMENT

The authors acknowledge the support and guidance extended by Chief Executive (Airworthiness), CEMILAC, DRDO &Shri Krishna Kumar, Sc-F Regional Director (APS) for their valuable guidance & support in writing this paper.

Authors also acknowledge the guidance & the support extended by VTU, Belgaum & their doctoral team for their continual review.

REFERENCES

1. Digital Satellite communication: Giovanni E Corazza, University of Bologna, Italy, Springer Publication.
2. Signal processing in Digital communication: George J.Miao, Artech House publication.
3. Modeling of Digital communication systems using Simulink: Arthur A. Giordano, Allen H. Levesque. Wiley, Publication.
4. Introduction to Digital Communication: KRZYSTOF WESOLOWSKI, Poznan University of Technology, Poland. Wiley, Publication.
5. Modern digital communication signals and systems: Sung-moon Michael yang, Springer publications.
6. MIL-STD-188-181A: 31 Mar 1997: Interoperability standard for single-access 5-KHz and 25- KHz UHF satellite communications channels, Department of Defence.

Author Biography:

Shri Anantha Padmanabha, Scientist-F is currently working in CEMILAC, DRDO and looking after the Airworthiness certification of Avionics, communication & EW systems for various airborne platforms. He received his M Tech degree in Electronics Design & Technology from Tezpur, Central University, Assam and currently pursuing PhD from VTU, Belgaum. He is a recipient of "Scientist of the laboratory Award" in 2010 and Technology group award in 2013 & 2017