

DESIGN OF LOW POWER R2R DAC FOR HIGH SPEED COMMUNICATIONS

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Abstract: The DAC is a device which converts a digital signal to an equivalent analog signal such as a voltage, current, or electric charge. Natural phenomena are converted to digital signals using A/D converters which are then converted back to analog signals using D/A converters. DAC is used for high-speed applications. DAC includes an input circuit that produces a number of interchangeable signals to respond to a digital input signal and ladder network. The resulting DAC output voltage is proportional with digital value applied to resolution. The main components are op-amp, R2R ladder and binary switch. There are various types of D/A converters. To overcome huge range of resistors in the other types R2R ladder DAC is introduced. The CMOS schematics will be designed and simulated using Mentor Graphics tool.

Keywords: DAC, R-2R ladder, CMOS, OP-AMP, Switches.

I. INTRODUCTION TO DAC

Wireless communication has been a driving force in the development of analog electronics for the past decades. High-speed digital to analog converter (DACs) are in high demand today. The signal we have seen and stored is in analog form. In order to process the signal effectively the signal is converted to a digital form. Thus the interaction between analog and digital signals are known as Data converter. In RF systems the analog-digital interface is pushed to towards the antenna, as a complex signal processing can be handled more efficiently in the digital domain.

Where do we need DACs?

A Computer is a binary machine that operates in the analog world so that it can produce meaningful output by the device using DAC. In order to play the back sound like a speaker we need analog signals because as we know the speaker position is vibrating based on the depth of the analog signal to produce sound. So here, we're going to make DAC convert a digital audio file into an analog signal to play on the speaker.

DAC operation

A binary system is a temporary system, which means a local value system, each of which

represents the presence or absence of two specific energies in the total energy values. In other words the whole digital process of the analog conversion process can be thought of as a function of amplification - the binary value is viewed at a certain voltage level, with 0V being the minimum and maximum volume being the highest voltage input. Digital to analog Converter commonly referred to as, D/A or D2A is a tool that converts binary values (0s and 1s) into a set of continuous analog voltages. There are many ways in which it is done with its own advantages and disadvantages.

TYPES OF DACs

A) BINARY WEIGHTED NETWORK

Binary-weighted DAC is one of the fastest conversion methods. It contains any current sources or resistors for each bit. These items are connected to the summing area that gives the result. It suffers from poor accuracy because of the high precision required for each voltage and current. Due to features such as high accuracy, it is expensive so this type of converting is usually limited to 8-bit resolution or less.

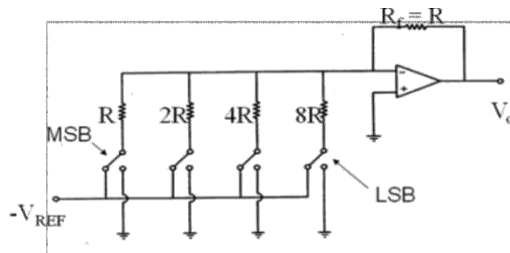


Fig 1.Binary Weighted DAC

B) R2R LADDER NETWORK:

This type of DACs contains a resistor value structure that can be closely matched. The topology is binary with weight and offers a high resolution compared to its binary weight counterpart. The most popular D / A converter structure uses the R-2R ladders. These ladders are useful for monitoring binary cycles with a small number of elements and with a resistance rate of only 2, except for the number of bits, N

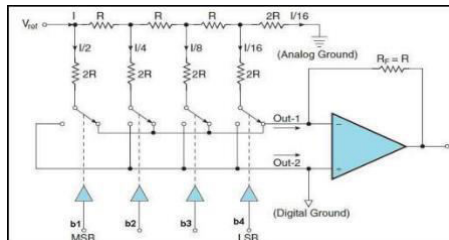


Fig.2.R2R ladder DAC

The output of DAC is given through

$$V_{OUT} = -V_{REF} \sum_{i=0}^n b_i \frac{1}{2^{i+1}}$$

C) RESISTOR STRING NETWORKS

This type of DACs is new and the switch network is connected to a decoder-like tree. The main limitation of this DAC is the delay on the switched network. The figure below shows the Resistor DAC thread.

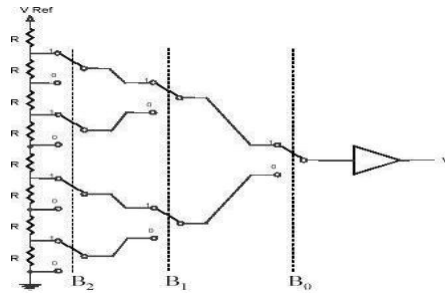


Fig 3.Resistor String Network

1.2 OBJECTIVE

The main purpose of this project is to design an R2R Ladder DAC to reduce the energy consumption and handling of elements that occur in a standard DAC.

1.3 PROBLEM SPECIFICATION

Improper control of the elements occurs in the DAC-weighted Binary and is also suffering from poor accuracy due to the high precision required for each voltage or current that is too expensive.

II.RELATED WORK

In this work a 6bit DAC is designed. The block diagram of 6 bit DAC is shown in fig.4

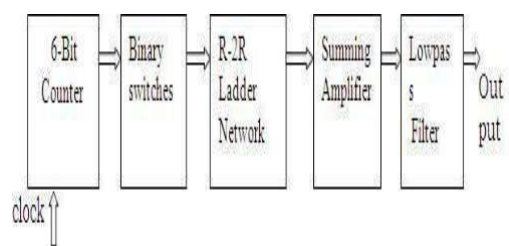


Fig 4.Block Diagram of DAC

The component used to build the circuit consists of a binary switch, a R2R resistor network, and a Summing amplifier, a low pass filter.

2.1 COUNTER

The counter contains six sections with a Cascaded D-flip-flop. One flip-flop is connected to a clock and the other to a previous flip flop effect. The reset is connected to all Flip Flops. When the LSB gradually becomes less transformative the information becomes paralyzed with all flip-flops. The first flip-flop

release serves as the input of the second flip-flop and up to six.

It generate up to 64 parts due to 6-bit. Current releases are included as binary R-2R binary input.

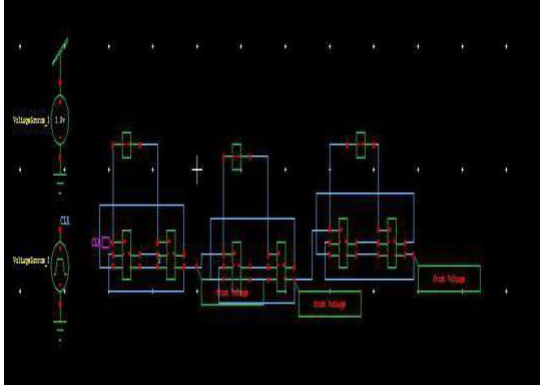


Fig.5. Schematic of Counter

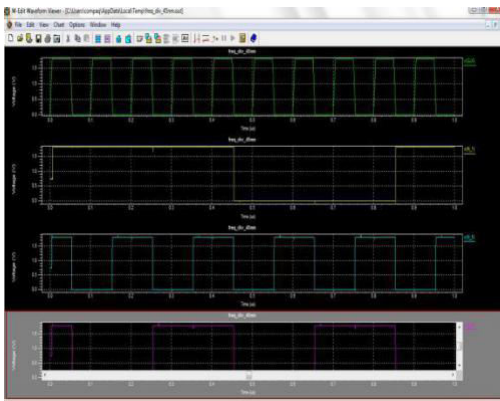


Fig.6. Simulation of 6 bit Counter

2.2 BINARY SWITCHES

The digital input controls the switch and connects the input to the standard V voltage or to the OPAMP virtual ground.

2.3 R-2R LADDER NETWORK

The R-2R ladder is simply a cleverly designed resistance set that gives you the unique ability to convert binary signals into an analogue output volume. It operates on a superposition basis when switching to binary options input adds additional voltage to the output. The steps are useful for detecting binary streams with a small number of elements at a resistance level of only 2, except for the number of bits, N. Therefore, the R-2R is generally smaller in size and offers better accuracy compared to other methods. R-2R ladder setup using two

different, standard 2 resistors: N-bit DAC requires 2N resistors.

It uses Kirchhoff's current law which states that the number of wheels entering a node must equal the number of waves leaving the node. At a stage, at each location, the current is split into two. By changing the currents in each node the total flow now has a binary weight.

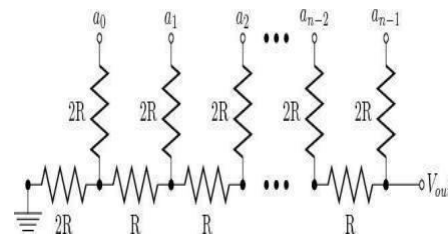


Fig.7 R2R Ladder Network

2.4 SUMMING AMPLIFIER

In this work OPAMP is used as Summing Amplifier. The main function of summing amplifier is to sum up all the individual current flowing through the resistor or voltages in the resisting regions. The circuit provides a good range of standard mode and good output.

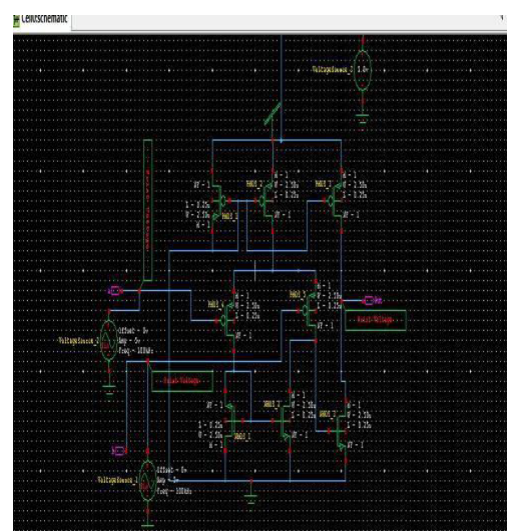


Fig.8. Schematic of Summing Amplifier

The input differential amplifier stage is implemented by a pair of pmos transistors with their sources tied together. The pair is biased by current mirrors which acts as active load. There

are two current mirrors pmos and nmos current mirrors. The pmos current mirror serves as a constant current source and nmos which sinks the current.

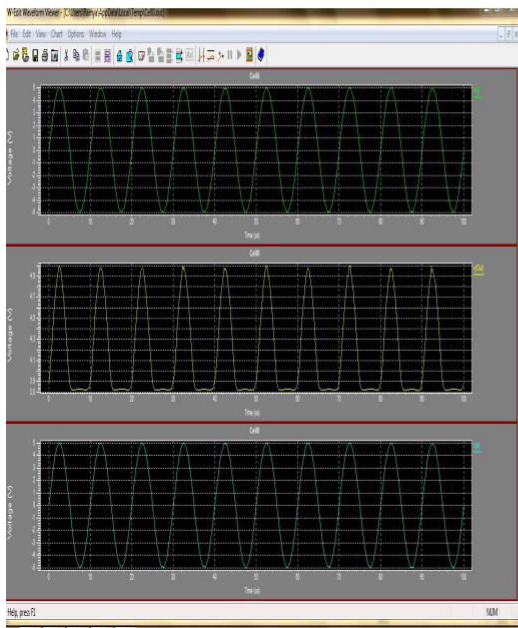


Fig.9.Simulation of Summing Amplifier

2.5 LOW PASS FILTER

The main function of low pass filter is to obtain a smooth curve for the step output of the DAC. The basic operation of LPF is the output of DAC requires a low pass analog filter called reconstruction filter, which is used to construct a smooth analog signal from digital input as in the case of DAC or other sampled data output device. The stair case output wave formed at the DAC output is smoothened by the Low pass filter.



Fig.10.Schematic of LPF

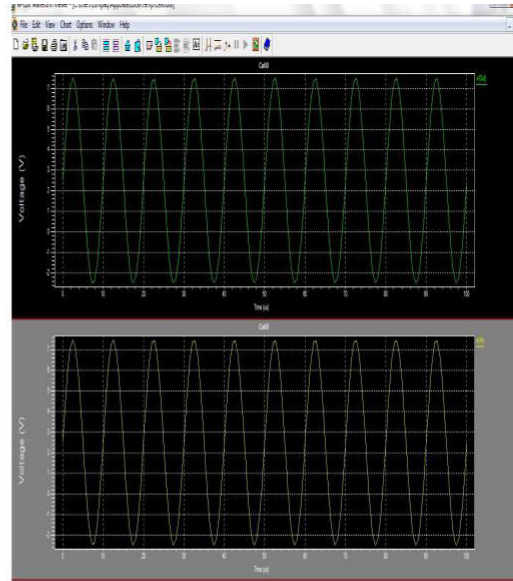


Fig.11.Simulation of LPF

3.Simulation Result of R2R LADDER DAC

The fig.12 shows the schematic of R2R ladder DAC. By integrating all the previous blocks that is the 6-bit counter, summing amplifier and the low pass filter in which all these are connected with resistors of the values R and 2R we obtain the overall schematic of the R2R ladder DAC.

The network converts a parallel symbol into analog voltage. Each input adds its own weighted contribution to the analog voltage.

The main work of DAC is to obtain an analog voltage. From the above circuit this can be done when a certain number of sequence is given by the counter and then it is converted into analog voltage by R2R ladder network in which the multiple voltages are added by the summing amplifier and finally produces a distortion less output after connecting it to the low pass filter.



Fig.12.Schematic of R2R ladder DAC

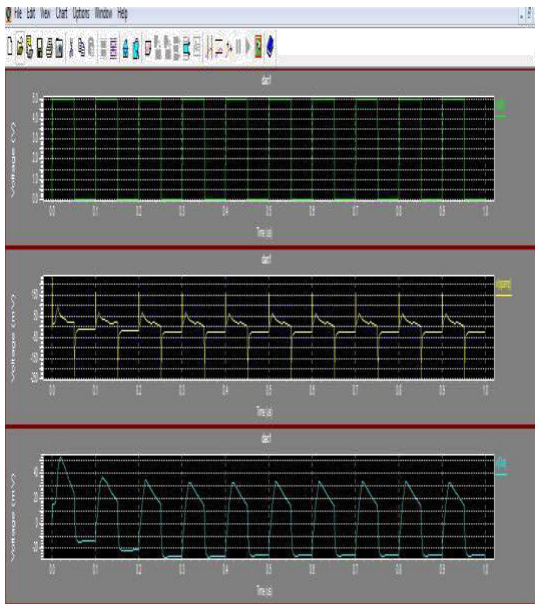


Fig.13.Simulation of R2R ladder DAC

4. RESULTS AND DISCUSSION

The designed circuit consists of counter, binary switches,summing amplifier,low pass filter and the resistors.The reference voltage considered is 1.8V.The approach of both binary weighted and R2R will be similar.The drawback of binary weighted is the circuit requires large range of resistors with high precision which is expensive whereas in the R2R ladder DAC it has only two resistor values R and 2R.It does not require any high precision resistors.

The below table shows the parameters of Dac in this work

Process used	0.18 μ m
Bit Resolution	6-bit
Supply voltage	1.8V
Power dissipation	1.09mW

Table 1.Parameters of DAC

5.CONCLUSIONS

The present work discusses the design of R2R ladder DAC which is used for high speed communications.Operations performed on this DAC are simulated using 0.18um CMOS technology in Mentor Graphics tool to obtain

the accurate results.So Considering all the output parameters within the limits we have designed a R-2R ladder DAC which consumes low power and reduces the distortions in the circuit.

6.Comparison of Binary weighted DAC and R2R ladder DAC.

DAC type	BINARY WEIGHTED DAC	R2R LADDER DAC
Parameter		
PROCESS USED	0.25 μ m	0.18 μ m
SUPPLY VOLTAGE	3.5V	1.8V
POWER DISSIPATION	455mW	1.08mW

Table2.Comparison of DACs

7.REFERENCES

- [1]Samiran Halder, Hans Gustat,"A-30GS / s-4-BitBinary Weighted DAC in SiGe BiCMOS Technology" pp.1-4244-1018-5 / 07.
- [2] .Palmer, P. and M.S.J. Steyeart, 2010. A 10- bit 1.6- GS / s 27-mw current D / A converter with 550-MHz 54-dB SFDR bandwidth at 130nm CMOS. IEEE T. Circ. Syst., 57 (11): 2870-2879.
- [3] .Song Yijun and Li Wenyuan, "A 6-bit 4 GS / s pseudo-thermometer separated by a CMOS DAC". Journal of Semiconductors, Vol. 35, No. 6, June 2014.
- [4].No A.B.A.Taib,Md.Mamun,"Loe power 3-bitDigital to Analog Converter in 0.18 μ m CMOS Process"ISSN:2040-7459.
- [5] .Laizhuan Lin, Zhiquan Li "Design of 7-bit 16-MS samp / s Low Power Supply Digital Power-to-Analog Converter.3rd International Convention on Multimedia Technology (ICMT 2013).
- [6].Xu Wu,Steyaert M.A 90nm CMOS %-bit 2GS/s DAC for UWB transceivers.IEEE ICUWB, 2010:20

- [7] .Doveugele J, Steyaert M S J. A 10-bit 250-MS / s binary-current density of DAC. IEEE J Solid-State Circuits, 2006, 41: 320
- [8] Bhaumik Vaidya, Devani Anupam, Prashanth Dadhania, Nehal parmar Design and 4DAC Decoder Simulations using Design Designer IJSRD ISSN(online): 2321-0613.
- [9] Jevegeny Perelman and Ran Ginosar Low Power D/A converter IEEE TRANSACTIONS In TECHNOLOGY.
- [10] Liu Huigang; Geng Weidong; Liu Yanyan November Design for Dual Ladder Resistor D / A Converter.