DESIGN OF MCM BLOCK OF FIR FILTER WITH MINIMISED AREA

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In this paper, an algorithm is proposed to design a linear phase FIR filter with less number of shifters and adders. The proposed algorithm is a tree based algorithm, where a specific path is chosen to compute the given coefficient set. When the coefficients are computed along the path suggested by the proposed algorithm, the number of shifters and adders required for computation of those coefficients are reduced to an appreciable quantity. The algorithm works well with higher order FIR filters and achieves considerable amount of reduction in the chip area when applied to those filters. Examples for the proposed algorithm shows that it reduces the number of shifters and adders required for performing the computation. The proposed algorithm can be simply extended for the design of FIR filter with less area consumption.

Keywords: Adders, Shifters, Multiple Constant Multiplication, Rootnode, definite path.

1.Introduction:

Linear phase finite impulse response (FIR) filters arewidely used in digital signal applications such as speechcoding, image processing, multi-rate systems, etc. Although thestability and linear phase is guaranteed, the complexity andpower consumption of the linear phase FIR filter are usuallymuch higher than that of the infinite impulse response (IIR)filter which meets the same magnitude response specifications.Therefore, many efforts have been made to the design oflow complexity linear phase filters.
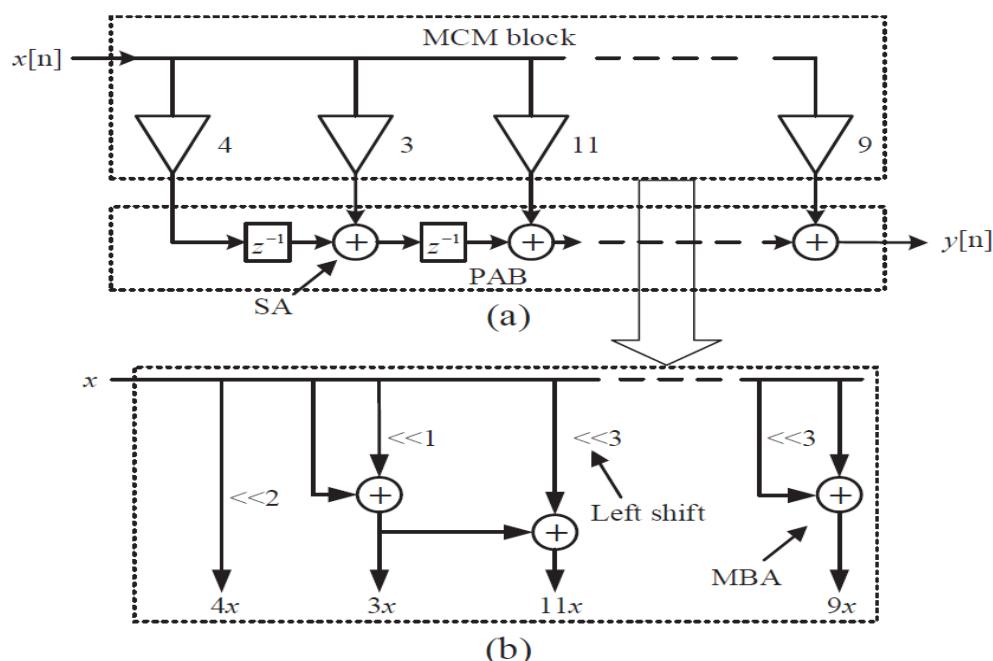

Figure 1.1(a)Transposed direct form of FIR filter (b) Shift and add implementation of MCM block.

A conventional filter structure, called transposed direct form,is shown in Fig. 1.1(a), in which the input signal is first multipliedby the constant filter coefficients and then goes into the delayelements. This operation is often referred to as multiple constantsmultiplication (MCM) problem. The adders in the MCM block are referred to as multiplier block adders. These adders

can be further classified into structural adders (SA) and multiplier block adders (MBA). The MBA's are used to compute the products and these products are then accumulated using the SA's in the product accumulation blocks (PAB).

The constant multiplierscan be realized using multiplier-less techniques where the generalmultipliers are replaced by a network of shifts and adders, asindicated in Fig. 1.1(b). The design of FIR filters using a multiplier-less technique is of two different categories. The first step is to obtain a continuouscoefficient set by linear programming optimization and quantize this continuous coefficient set within a given wordlength to obtain a discrete coefficient set. After that, a certain MCM algorithm is applied to the discrete coefficient set to synthesize the adder-and-shift network.But having a discrete coefficient set makes the hardware realisation less optimal, due to increase in complexity of the design. Thus instead of designing discrete coefficients, many researchers have gone back to the filter design process to incorporate the MCM algorithms into the discrete coefficient set optimization procedure.

In this paper, we propose a linear phase FIR filter design algorithm aiming to find a coefficient set which can be synthesized into an adder-and-shift network with the lowest number of shifters and average adder depth (AAD) of SAs. The proposed method is based on tree search in which we traverse along a specific path in order to realise the coefficients with least number of shifters and adders.

The decrease in the number of shifters and adders will eventually lead to reduction in the chip area. Since the adder cost of SAs generally is determined by the filter order which is fixed, the lower AAD will also lead to the lower power consumption of SAs.

2.Proposed algorithm for the MCM block implementation

In this section, we will discuss about the algorithm used to find the definite path consisting of intermediate nodes which are nothing but the quantized coefficients for computing theeach coefficientfrom the given set of discrete fixed coefficient set of N-order FIR filter.

Optimised path search procedure

For the design of multiple constant multiplication block of FIR filter, root node is generated from the given set of fixed discrete coefficients under some conditions. This leads to the production of child nodes from which another root node is generated and this is repeated until all the coefficients are computed in the optimized path requiring minimum number of shifters and adders. The detailed procedure for the proposed algorithm is given below:

1) First, sort the discrete coefficients of the N-order FIR filter which are already to quantized to discrete coefficient set within the required wordlength from the continuous coefficient set in descending order.

2) Next, from the sorted coefficient list, the coefficients that are powers of 2 are not considered for further computation and they are removed from coefficient list since they can be implemented only using left shifter without any need for adders.

3) To find the discrete root node, check for bit position with the maximum number of 1's from the Maximum Significant Bit (MSB) to the bit position before LSB in the list of binary representation of the discrete coefficients. If two or more bit positions has the same count of logic 1 and is the maximum count, then select the position which is near to the MSB.

4) Consider the smallest coefficient among the coefficients with the selected bit position having the maximum number of logic 1.

5) In that smallest coefficient, consider the bits from the selected bit position up to the LSB of that coefficient. This forms the root node.

6) Subtract the root node value from all the other coefficients that are greater than or equal to the root value. The result obtained out of subtraction forms the child nodes and append this value to the pathlist of coefficients greater than equal to root node where pathlist is the list of optimum paths for each and every coefficients of the N-order FIR filter.

7) Once again, the root node is computed, using the above procedure, for the set of generated child nodes. The root nodes that are generated at each level are stored in a list because if the same root node is generated after some steps already implemented root node can be reused which further reduce the number of shifters and adders.

8) If the child node is a 'power of two' number, then it can be directly obtained by means of shifters and thus they are not included in the further calculation process and they are added to the pathlist of that particular coefficient.

9) Also if any of the child node computed equals to any already generated root node value then child node is not considered for the further calculation because already implemented root node can be reused.

10) If two child nodes are left, then take the smaller child node as root node and go to step 6.

11) The above steps are repeated until we are left with a single child node and this child node is added to the pathlist of the particular coefficient.
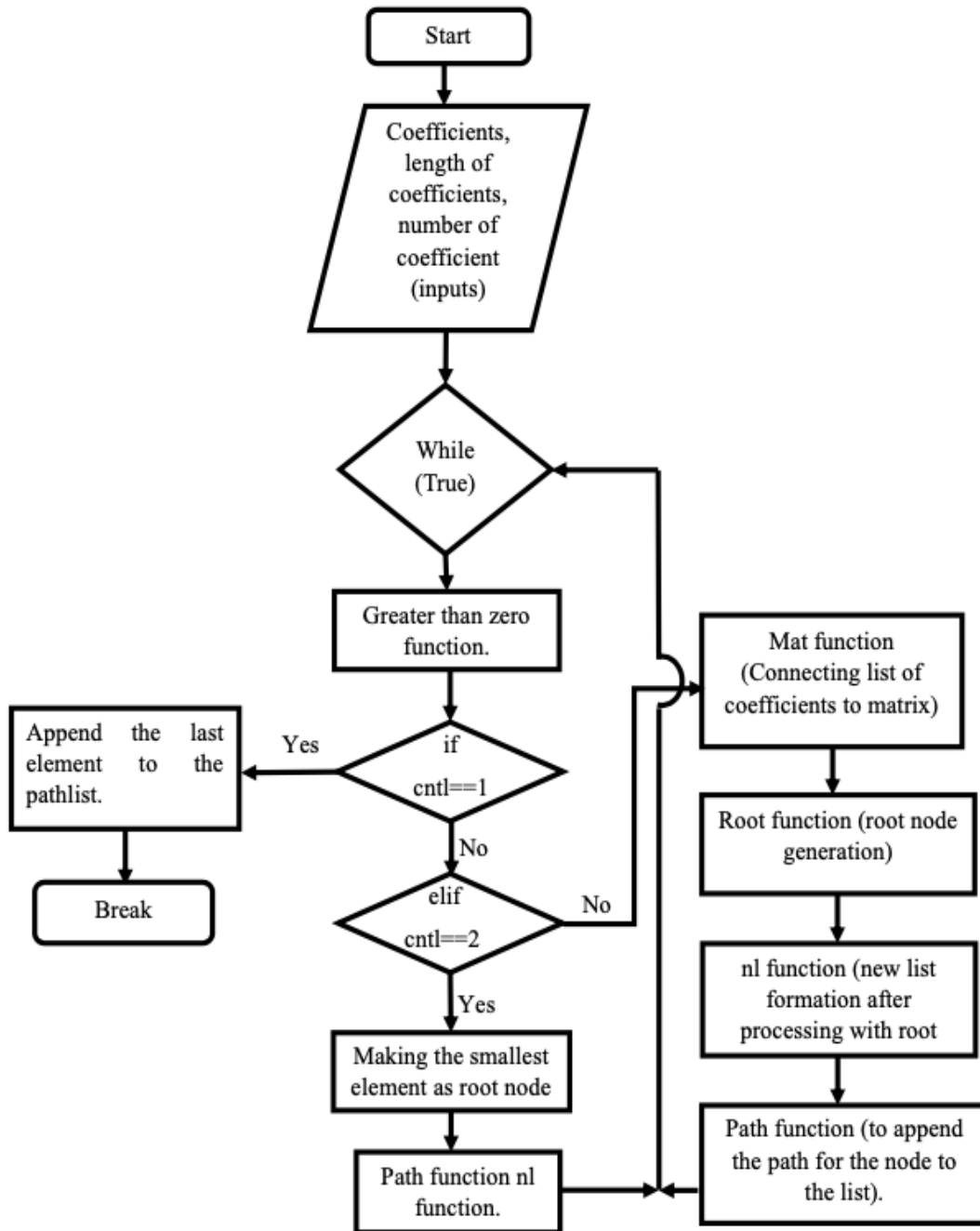
Figure 2.1 Flowchart for the proposed algorithm for MCM block design

In the given flowchart '**cntl**' refers to the number of zeros present in the newly formed list '**nl**' after each computation process of finding the root node and child nodes which are power of 2.

3. Analysis of the proposed algorithm

In this section, we discuss about the advantages of the proposed algorithm for the MCM block implementation by analysing and comparing the schematic representation of the MCM block without implementing the proposed algorithm that is the conventional model with schematic representation of the MCM block after implementing the proposed algorithm for the example given below.

$$H(z) = 4 + 9z^{-1} + 11z^{-2} + 16z^{-3} + 25z^{-4} + 39z^{-5} + 43z^{-6} + 56z^{-7} \qquad 3.1$$

In conventional model, each and every discrete coefficient of the FIR filter are implemented using the shifters and adders network individually. There is no connection between the adder and shifter network of any two coefficients, so no adder or shifter can be used commonly between any two coefficient shifter and adder implementation.

While in the proposed model of MCM block implementation, shifters and adders are shared among many coefficient implementation. This is made possible by applying the proposed algorithm to find the root node which is realised using adder and shifter network and itsoutput value are shared among the eligible coefficients' hardware implementation.

Figure given below gives us the clear idea about the difference between the conventional model and proposed model of the Multiple Constant Multiplication (MCM) block design.
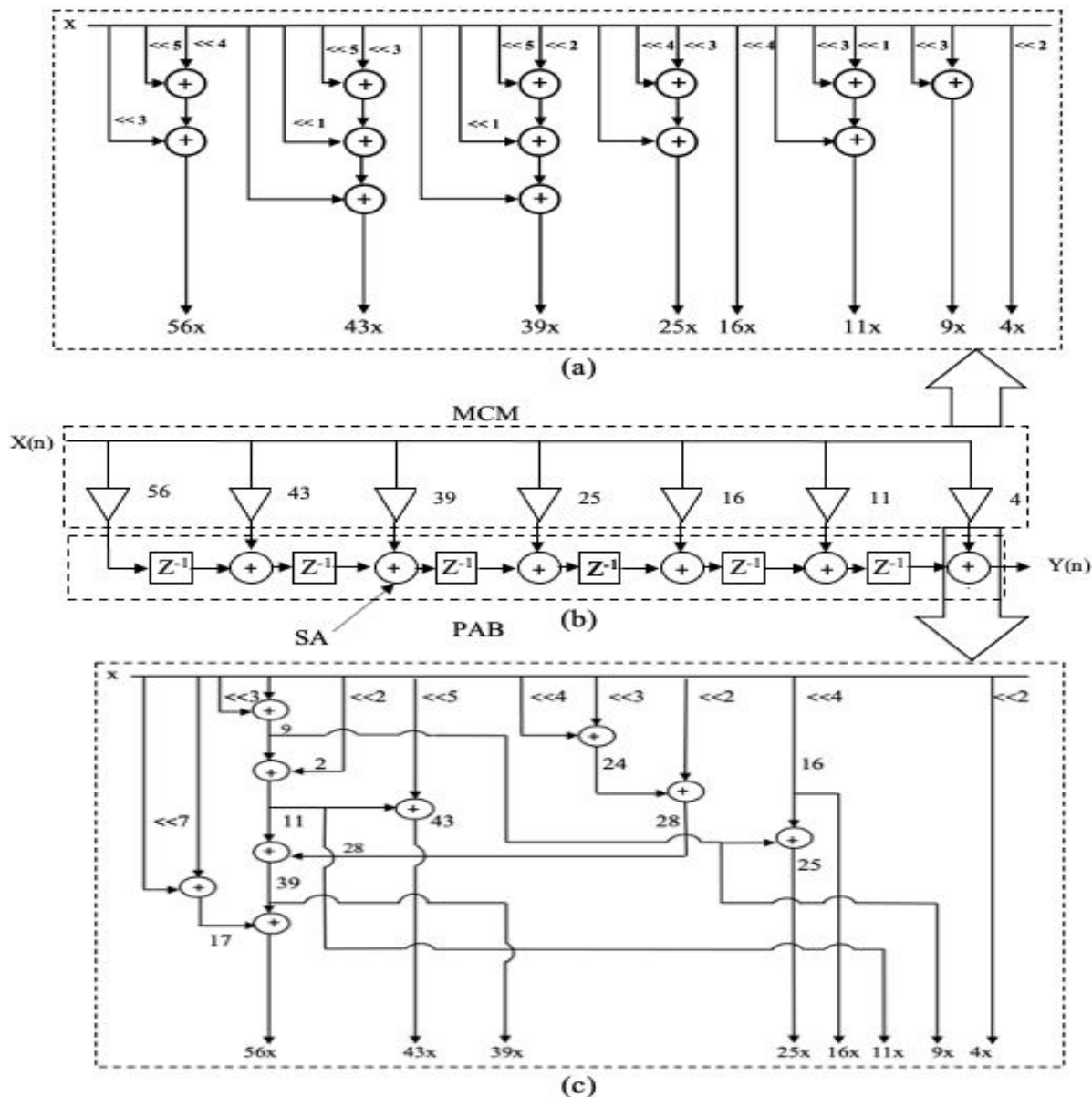

Figure 3.1 (a) Implementation of MCM block without using the proposed algorithm (conventional method) (b) Transposed direct form FIR filter structure (c) Implementation of MCM block using the proposed algorithm

Here, the number of adders and shifters used in proposed model is very much less than the total number of adders and shifters used in conventional model. This reduction in the number of hardware components in the transposed direct form realization of N-order FIR filter results in the reduction of chip area consumption. For example, if we consider the same example that is mentioned in equation 3.1, the number of adders in the proposed model is 9 while in conventional model it is 13, therefore when we realize the adder using 16-bit carry lookahead adder in hardware implementation, an area of $864\ \mu m^2$ is reduced even without considering the reduction of area due to number of shifters.

Table 3.1 Comparison of Number of Shifters

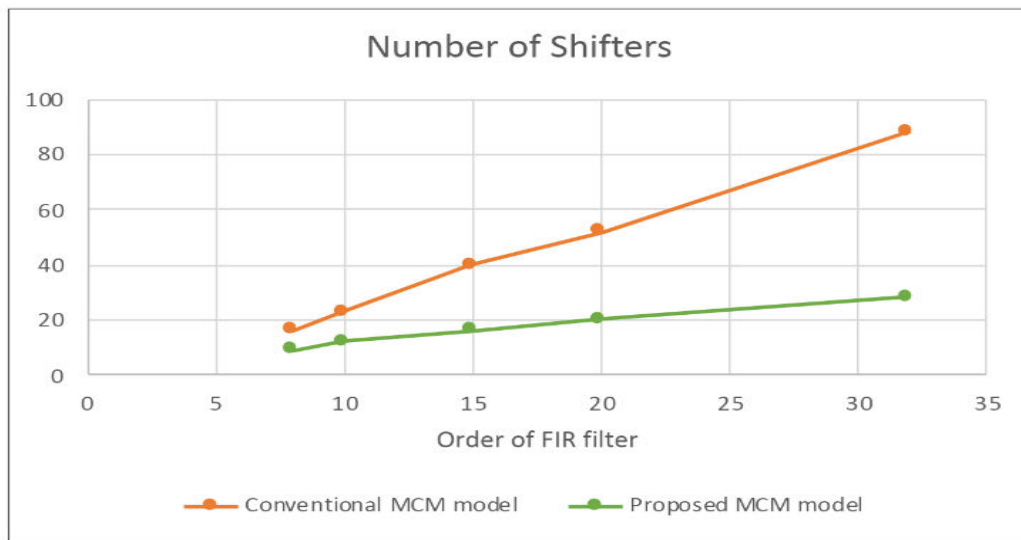| Order of filter (N)	Conventional MCM model	Proposed MCM model
8	16	9
10	23	12
15	40	16
20	52	20
32	88	28

Figure 3.2 Comparison graph between number of shifters in conventional and proposed model of MCM block

Table 3.2 Comparison of Number of Adders

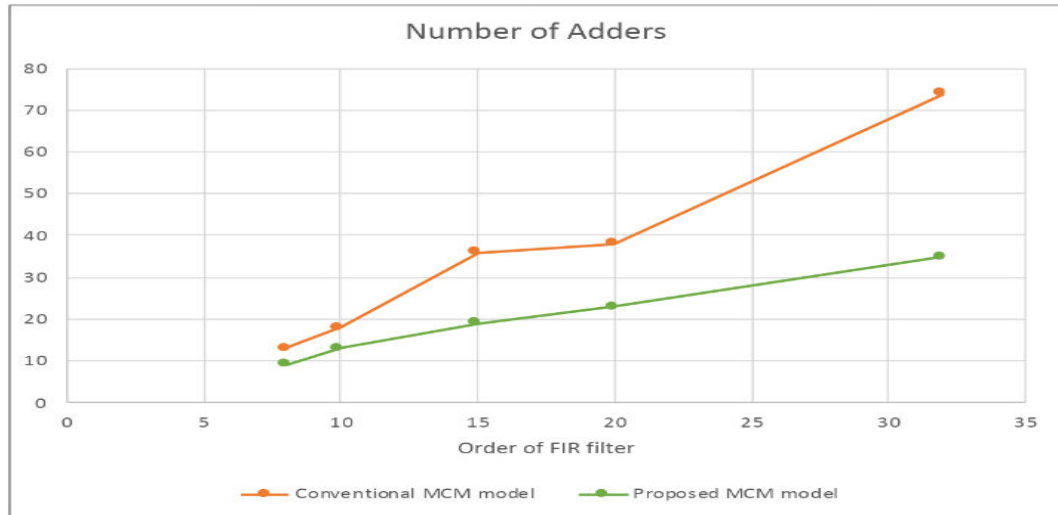| Order of filter (N)	Conventional MCM model	Proposed MCM model
8	13	9
10	18	13
15	36	19
20	38	23
32	74	35

Figure 3.3 Comparison graph between number of adders in conventional and proposed model of MCM block

Though we share the adders and shifters between two or more coefficient realisation it does not affect the filtration process that is, it produce the same filtered output signal as that of the conventional model MCM block realisation. This is proved by processing the same input signal in both conventional MCM model and proposed MCM model of FIR filter using the Simulink software. Simulink software enables one for the rapid construction of virtual prototypes to explore design concepts at any level of detail by providing the customizable set of block libraries with graphical block diagramming tool. Simulation output of the FIR filter consisting of proposed MCM block along with the input signal is given below :
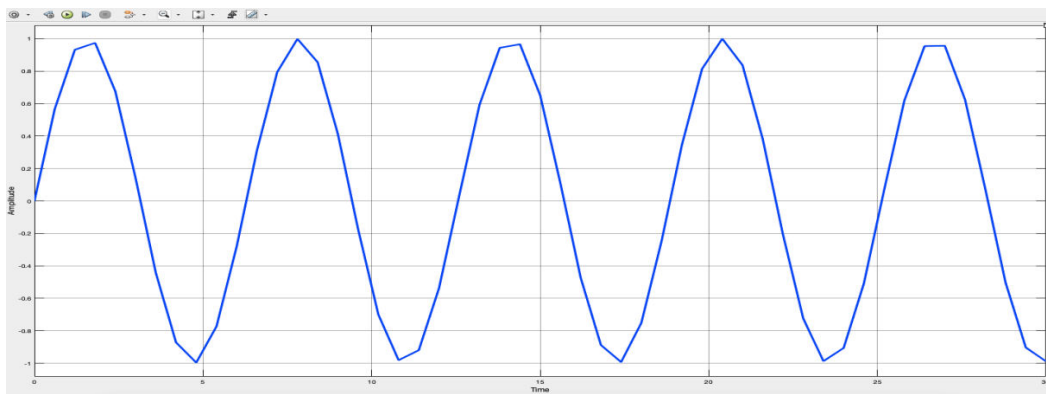
(a)
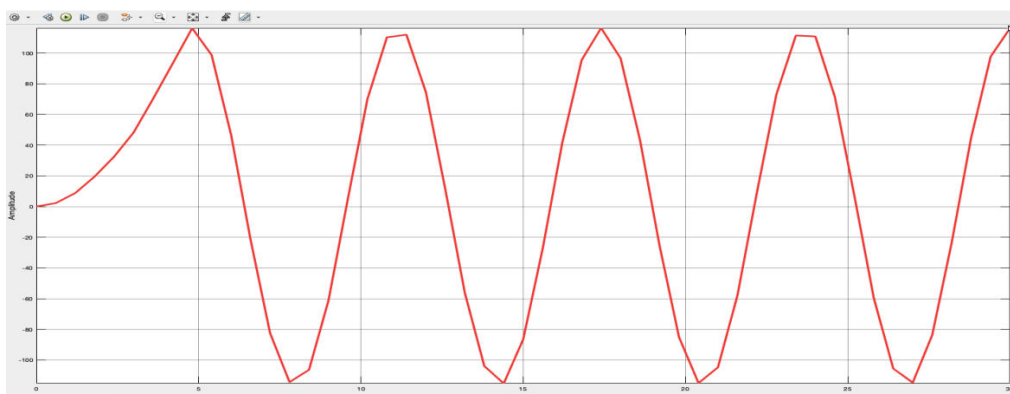
(b)

Figure 3.4 (a) Input signal to the FIR filter (b) Filtered output signal from FIR filter

Therefore, the overall performance of the proposed model of MCM block in FIR filter is far superior than conventional model especially in terms of chip area consumption without any compensation in the filtering process.

4. Conclusion

In this paper, a FIR design method with less number of adders is proposed. A tree based algorithm is found to find the minimum number of adders required to compute the coefficients of the FIR filter. In this tree based algorithm we traverse along a specific path for computing the filter coefficients. Various conditionals are employed in order to determine the specific path that is to be traversed. The algorithm focuses on finding the path involving minimum number of adders, in a shorter span of time when compared to the other conventional methods. This is achieved by considering only a single path along the tree. Thus the time required for identifying the path with minimal number of adders is less when compared to the existing methods. Design examples shows that the proposed algorithm effectively reduces the chip area by minimizing the number of adders and shifters required for the computing the filter coefficients. Thus it is evident that the proposed algorithm can generate designs with less chip area than the existing systems.

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