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Low Power High Speed Magnitude Comparator Design

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***Abstract*- The modern portable devices demand ultra-low power consumption due to the limited battery size. The binary magnitude comparator is the important block in many digital systems. This paper explores the existing magnitude comparator design techniques and proposes a new binary comparator that provides significant reduction in the power and area. In order to evaluate the effectiveness of the proposed technique over the existing, all the existing comparators are implemented in Verilog, synthesized and simulated with Xilinx tool chain and design metrics such as area, power and delay are evaluated. The simulation results on FPGA show that the proposed comparator provides more than 2.6% reduction in power over the best-known comparator.**

***Keywords:* Comparator, High speed integrated circuits, VLSI, Low-power design, FPGA.**

I. INTRODUCTION

The modern very large scale integration (VLSI) technology allows us to build an Integrated circuit (IC) that can have thousands of transistors into single chip. More and more functionality are being implemented into the same chip with each new technology. This integration of huge functionality is imposing several challenges to the VLSI designer as increasing functionality increasing failure probability. Further as area, power and delay are main area of concern; it is very difficult to achieve optimal value of these parameters at the same time. High power consumption due to several operations on these devices worsens the performance of the device and lifetime of the battery.

In addition to the basic arithmetic operations, comparison of two numbers is the prime operation performed in the most processing units for performing functionalities such as instruction decoding, flag generation etc [1]. In order to perform comparison efficiently, there is the demand of high performance low power comparator. The performance of the comparator significantly affects the overall performance of these processing units [2]. Significant efforts have been given to improve area, power and delay parameters of the comparator at different level of abstraction [3-6]. The existing architectures of the magnitude comparator are not power and performance efficient [3], thus, demanding novel comparator architecture that provides highly energy efficient comparison of two numbers. This paper presents an energy efficient comparator for different signal processing application.

The rest of the paper is organized as follows: Section II presents the work done to achieve low power high performance comparator and further critically analyses each of the design techniques. Section III details proposed low power comparator architecture whereas its effectiveness using via simulation is given in Section IV. Finally Section IV concludes the paper.

II. LOW POWER COMPARATORS

The section explores different comparator architectures in details.

Traditional Comparator Architecture

The block diagram of the magnitude comparator as shown in Figure 1 has two inputs and three outputs [3]. The comparator compares two inputs A and B and provides output as either EQ (A=B), G (A>B) or S (A<B) given by the following equations.

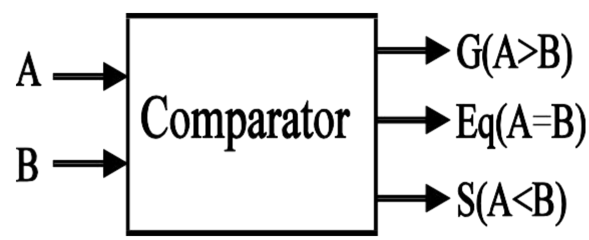


Figure 1: Block diagram of magnitude comparator

The circuit for comparing two n-bit numbers, has 2^n inputs and 2^{2^n} entries in the truth table, for example in 1-bit comparator has 4-rows in the truth table, whereas 2-bit comparator has 16 rows in the truth table.

2- bit Comparator Architecture

The circuit compares two 2-bit binary numbers A and B, and gives three outputs. Let input A and B have bits $A_1A_0$and B_1B respectively. The logical expression for the 2-bit comparators output G, S and Eq are given by the equations 1-3 below.

$$Eq = (A_1 \odot B_1).(A_0 \odot B_0)$$
$$G = A_1\overline{B_1} + (A_1 \odot B_1)A_0\overline{B_0}$$
$$S = \overline{A_1}B_1 + (A_1 \odot B_1)\overline{A_0}B_0$$

The logical diagram for the greater (G), smaller (S) and equal (Eq) are shown in Figure 2.

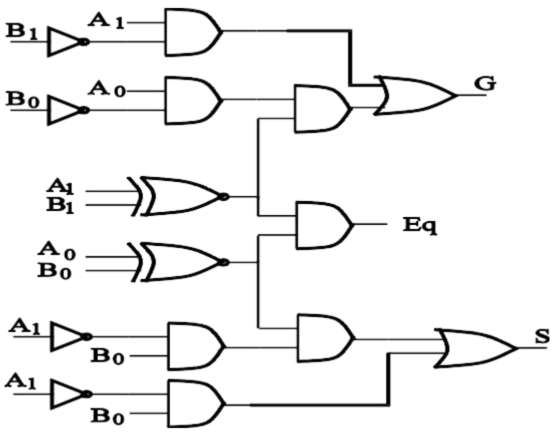


Figure 2: Logical diagram of 2-bit comparator

It is observed that as the input bit-width increases the complexity of the designs increases significantly. Therefore direct implementation of the higher bit-width comparator is costly in terms of area, power and delay as increasing complexity increases the power and delay. Hence, 4-bit comparator is used to design higher bit-width comparator.

Extensive bit-width Comparator

The direct implementation of large bit-width comparator is very complex and costly [7-10]. Therefore, we can implement extensive bit-width comparator using small bit-width comparator. Figure 3 shows 16-bit comparator design using five 4-bit comparators [11].

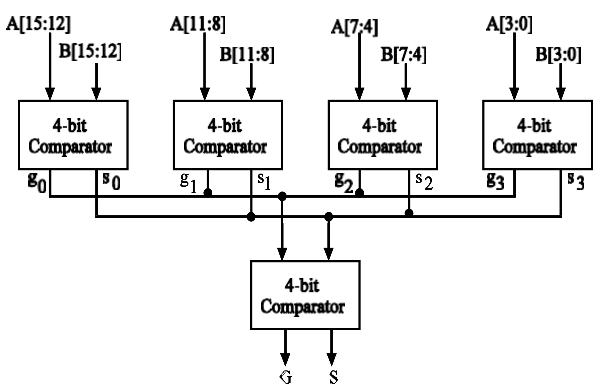


Figure 3: 16-bit comparator using five 4-bit magnitude comparators

In the first stage, four comparators compares group of four bits of 16-bit number whose outputs are given to the final comparator in the second stage.

Priority Based Comparator (PBC) Architecture

Priority based comparator [13] has three stages to compute output as is shown in Figure 4. First stage identify 1's in each input that may cause the number may be greater over the other number. The second step Identify most significant in each number. The third step identifies which number have 1's at more significant position over the other.

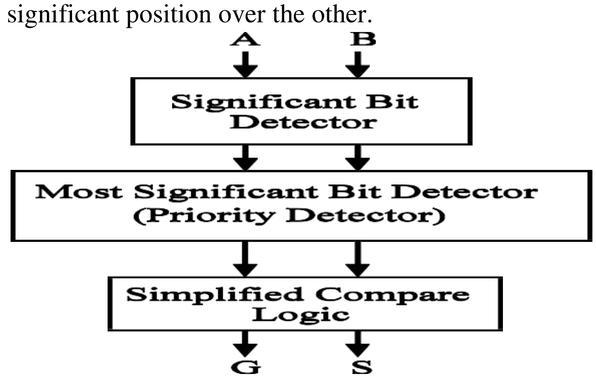


Figure 4: Block diagram of PBC

All the three stages are combined to achieve priority based comparator as shown in Figure. 5

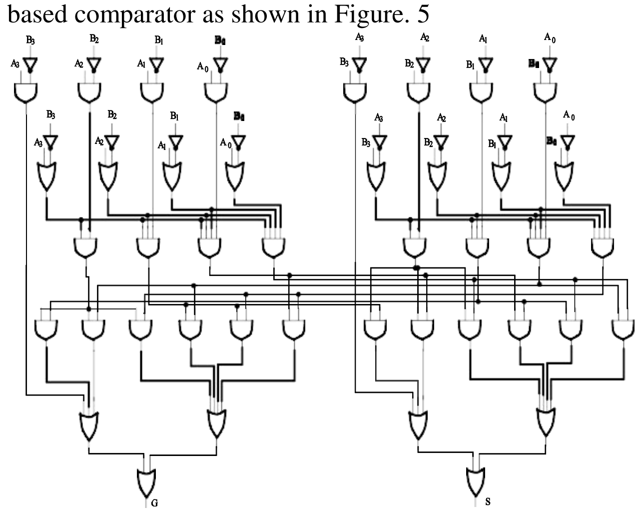


Figure 5: Logical diagram of PBC

Look-ahead Comparator Architecture

The look-ahead comparator (LAC) [13] is based on the concept of look-ahead adder where carry-in is calculated in advance to eliminate carry dependency. In the LAC, a look-ahead logic computes the bits which decides the which number is greater/smaller. The block diagram of the look-ahead block accepts two four bit numbers and generates 4-bit cmp output. Only one bit of the cmp out will be high if the number is greater or smaller else are zero it reflect that numbers

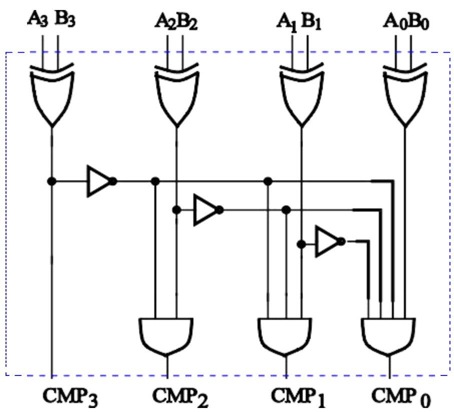


Figure 6: Logic diagram of look-ahead logic

The logical diagram of the look-ahead logic [14] as shown in Figure 6 requires four XOR gate to find 1‘s which corresponds to the _0‘ in the other number and then provides ultimate compare output based on the value of the XNOR out. If the most significant XOR is at logic _1‘ it reflect that this bit will cause output will be greater or smaller, if this bit is on logic _0‘, other significant XOR will be searched. In this way it evaluates the compare signal. The architecture of the look-ahead comparator as shown in Figure 7 employs look-ahead logic with some additional logic.

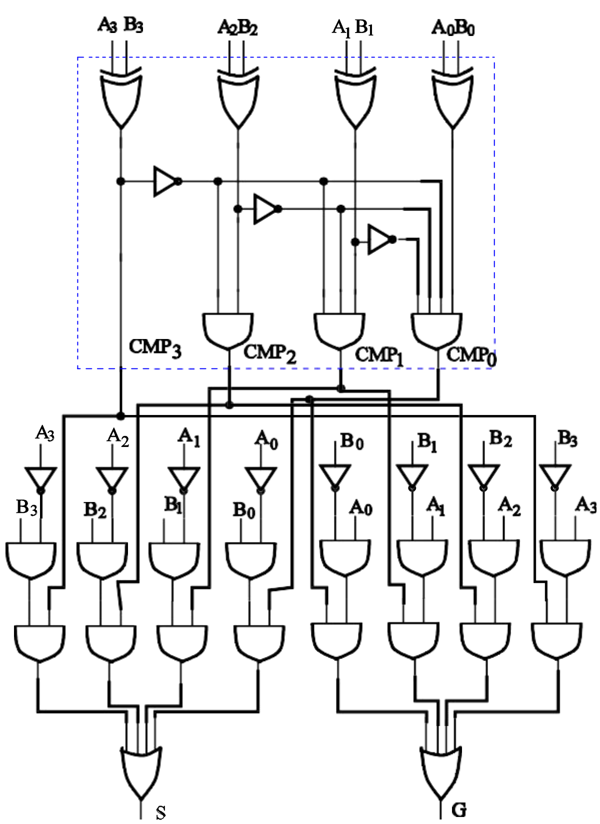


Figure 7: Block diagram of LAC

Subtractor Based Comparator

This comparator utilizes the subtractor to compare two numbers [15-17]. The block diagram of the subtractor based comparator (SBC) is shown in Figure 8.

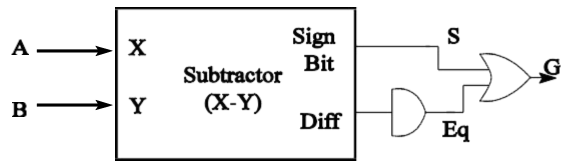


Figure 8: Block diagram of SBC

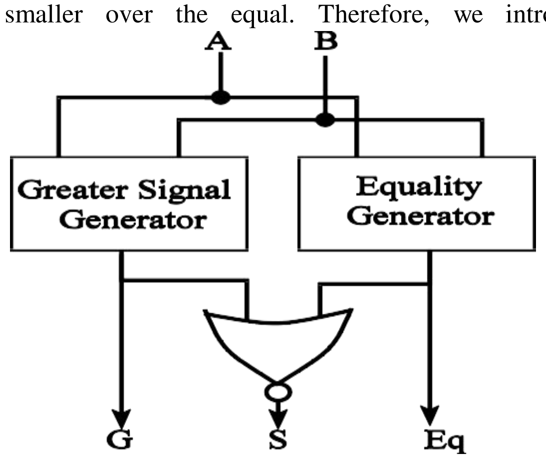
When the number A is smaller than number B, result of the subtractor will be negative which can be easily detected by the sign bit. If sign bit is _1‘ it reflect negative difference which in turn shows that number A is smaller than B. On the other hand, when the two numbers are equal it will provide zero output, in this case all bits of the difference will be zero that can be detected by simple OR gate. If all bits of the OR gate are zero then output will be logic _0‘ else it will be logic _1‘. The equal and the small signal is further used to generate greater signal.

III. PROPOSED LOW POWER HIGH PERFORMANCE COMPARATORS

The architecture of the proposed comparator is shown in Figure 9. The proposed comparator implement the logic for greater and equal signal. The equal signal is used further used to generate small signal.

Figure 9: Proposed comparator Architecture

It is observed in the literature that complexity in terms of area, power and delay are more for greater and smaller over the equal. Therefore, we introduce



comparator as shown in Figure 3.1 which computes greater and equal in place of greater and smaller. The greater and equal signals are further used to generate the small signal.

In order to compare the complexity of the proposed

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design over the existing we implemented the whole design with the 2-input NAND gate as 2-input NAND gate is universal gate which is standard benchmark. The equal logic requires 23 NAND gates while the greater and smaller logic requires 33 2-input NAND gates. Since in the traditional and existing architectures, logic for G and S are implemented simultaneously, it requires 66 two input NAND gates. On the other hand proposed scheme requires only 57 NAND gates only as it implements only greater and equal logic.

As the proposed approach requires less area over the traditional, it will consume less power and will have less delay. The simulation results in the next section show efficacy of the proposed over existing comparator architectures.

IV. SIMULATION ENVIORNMENT AND RESULTS DISCUSSION

All the comparator designs are implemented in Verilog. The Xilinx ISE 14.5 is used to synthesize the proposed and existing comparator architectures. Test bench for all the designs are created and simulated to verify the functionality of each designs. Further, design metrics such as area, power and delay are extracted and compared. Following subsections provides the simulation results and their analysis for the proposed comparator over the existing comparators.

Simulation results of 4-bit comparators:

All the comparator designs are coded in Verilog and implemented on Xilinx Vertex XC7VX330T. The implementation complexity in terms of area, maximum combinational delay and power consumed is evaluated. The design metrics are shown in the Table 1.

Table 1: Metrics of the 4-bit comparators

Technique Comparator	Area (#LUTs)	Delay (nS)	Power (mW)
Traditional	3	1.455	30
Priority Based	4	1.444	31
Look-ahead	4	1.522	36
Subtractor based	5	1.51	35
Proposed	4	1.455	30

It can be observed from the simulation results that proposed comparator requires 4.4% and 3.6% reduced power over Look-ahead and Subtractor based comparator respectively. Further, it can also be observed that proposed comparator requires 3.2%, 16.6% and 14.2% reduced power over Priority based, Look-ahead and Subtractor based comparator respectively. These 4-bit comparators are used to design 16-bit comparators.

Results of 16-bit comparators:

The design complexity of the different 16-bit comparators are shown in the Table 2. All the designs are synthesis with the same FPGA device to have apple-to-apple comparison.

Table 2: Metrics of various 16-bit comparators

Technique Comparator	Area (#LUTs)	Delay (nS)	Power (mW)
Traditional	20	2.556	151
Priority Based	20	2.466	153
Look-ahead	29	3.025	158
Subtractor based	18	2.922	163
Proposed	20	2.644	147

The area requirement of the proposed comparator is very small over the existing comparator archiectures as shown in Figure 11. The area is measured in terms of number of (Look Up Tables) LUTs which reflects the required combination logic to implement the desired logic. It can be observed from the Figure 10 that proposed comparator requires 10% reduced area over the Subtractor based comparator.

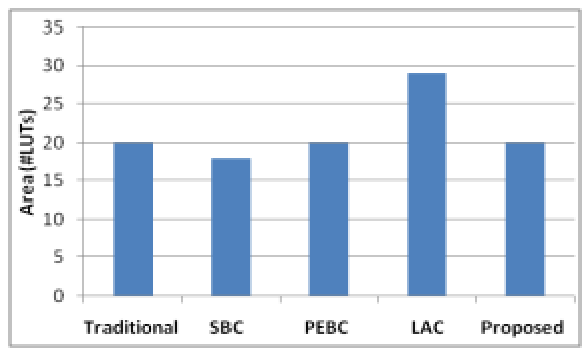

Figure 10: Area of various 16-bit comparators

It can be observed from the Figure 12, proposed 16-bit comparator exhibits smaller delay over the look-ahead. The proposed comparator requires 12.6% and 9.5% less delay over LAC and subtractor based comparator respectively.

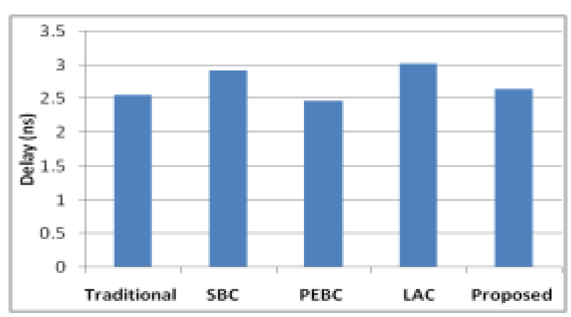

Figure 12: Delay of various 16-bit comparator

It can be observed from the Figure 13 that proposed comparator exhibits smaller power over the existing. The proposed comparator shows 2.6%, 3.92%, 6.9%, and 9.3% reduced power over the traditional, priority based, look-ahead and subtractor based comparator, respectively.

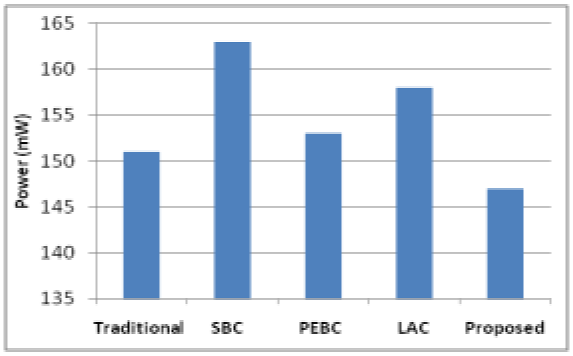

Figure 13: Power of 4-bit comparators

All these results shows efficacy of the proposed comparator over the existing architectures.

V. CONCLUSION

This paper explored the existing comparator architectures and presented a new comparator that shows significant improved performance over the existing comparator architectures. The proposed and existing comparator are implemented in Verilog and processed with Xilinx ISE tool chain. Further the designs are synthesized and post synthesis results are extracted. The extracted metrics are compared. The simulation results show nearly 2.6% power reduction over the existing architecture. Thus, the proposed comparator can be effectively utilized different signal processing applications such as image/video processing.

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