International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 05 Issue: 08 | Aug - 2021 ISSN: 2582-3930

RESEARCH WORK ON POWER QUALITY IMPROVEMENT USING CASCADED MULTILEVEL INVERTER

Mr. Vinod B. Kolhatwar
Dept.of electrical engineering
Vidarbha Institute of Technology, Nagpur

Prof.Souras Ghotekar
Dept.of electrical engineering
Vidarbha Institute of Technology, Nagpur

Dr.Sanjay S.Uttarwar
Dept.of electrical engineering
Vidarbha Institute of Technology, Nagpur

Abstract

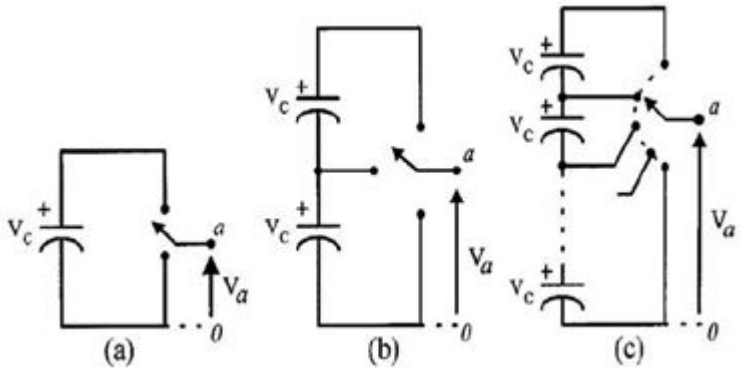
Recently, cascaded inverters have been tested for their superior value over voltage source and connector applications. The output of this converter is connected by a cross-sectional filter to create a sinusoidal flow with low harmonics as well as to meet the required network network requirements. The project is designing a new cross-sectional topology for a network connection system that connects a five-phase cable. The optical filter incorporates additional resistance-capacitance and similar capacitors of the inductive-capacitance-inductive capacitor as well as additional resistance to it to reduce energy loss. It can reduce the harmonic frequency fluctuations better than traditional filters and drop the same value applied, reducing power and resistance. Introduce quantitative filters and methods to determine filtered filters. In addition, a new system using Boundary Propagation (PSO) is recommended to ensure that the humidity is reduced and to ensure that the maximum humidity is reduced. In addition, the PSO algorithm for this function is used to raise the attenuation corresponding to the ambient frequency change based on the agreed values and filtering capacitance. A comparison discussion of a transient filter and the recommended filters is obtained from a test conducted on a 110V, 1 kW connected inverter. The volume conversion algorithm is implemented for a multi-variable converter using the SPARTAN 6-XC6SLX25 Processor Processor Processor (FPGA). Studies show that the recommended filters not only provide a reduction in power but can also provide a reduction in noise compatibility with higher frequency, better output output, as well as a lower Harmonic Distortion (THD) potential power level is better for some translators. -netite network - connected network

1. INTRODUCTION

The transformer provides the appropriate mechanism for medium and high power systems to produce an output voltage that allows the harmonic content of the voltage and current waves to be reduced. It refers to a series of connections in multilevel transformers, called "levels", to provide the output voltage at the desired "levels". The increase in phase speed causes a decrease in harmonic damage. Three topologies are selected, such as phase capacitor (FC), zero point (NPC) and multilevel cascade inverter (CMLI) for different applications, depending on the system and the conversion system. Of the three topologies, CMLI is the best choice for renewable energy integration due to benefits such as voltage drop issues, elimination of the DC-DC converter, changes without small frequency changes, interference and diodes.

CMLI photovoltaic (PV) solar power supplies come in a variety of forms, but are designed for processing in low-light and low-temperature conditions. The Sound Amplifier System (PWM) is recommended for CML level 5 and CMLI level 7 for photovoltaic systems that require rotation, auxiliary circuits and multiple signals to generate the pulse. The current CMLI Level 5 of a single PV system is combined with a PV system that requires adjustment of the LC filter to reduce losses and resistance at high power levels. The three maximum power control panels (MPPs) of the five-phase amplifier use an output switch between the inverter and the grid. Although the shrinkage decreases as the level increases, CMLI requires a number of semiconductor switches that must be reduced to reduce losses, costs, complexity and gaps. Series connection of multilevel inverters introduced in restricts its use in high power applications because of the necessity of changing the voltage polarity in every half cycle and also the switches with different ratings are required. A detailed look-up table is required for the method proposed in [7] which consists of series connection of a high-voltage NPC and a low-voltage on ventional inverter. A 5-level inverter with four DC sources comprising two numbers of 2-level and 3-level inverters is proposed in. The drawback of this method is that in conventional inverters upto 9 level can be generated with

the same number of power supplies. Bidirectional switches with voltage and current blocking capability for the reduction of switches is proposed in where each bidirectional switch requires a separate gate drive circuit which increases the power loss.



(a)Two levels, (b) Three levels and (c) n levels

Fig. 1 One phase leg of an inverter

2. PROPOSED WORK

The multilevel inverter using cascaded-inverter with separate dc sources (SDCSs) synthesize a favorable voltage from several independent sources of dc voltages, which may be achieved from batteries, solar cells and fuel cells. This structure recently has become very widespread in ac power supply and adjustable speed drive applications.

1) Study and analysis of various topologies of multilevel inverter.
2) To Study control strategy of cascaded multi-level inverter
3) To simulate "multilevel inverter switching and control algorithm" in MATLAB environment.
4) Design and development of Multilevel inverter for the proposed system.
5) Design and development of cascaded multilevel inverter for various operating condition.

Solar photovoltaic (PV) fed CMLI is dealt in various literatures, but it intends for low voltage and low levelconfigurations. Pulse-width modulation (PWM) technique for a 5-level CMLI. In this paper, a twenty five-level Cascade H-bridge inverter based T-STATCOMconfiguration has been presented. The adoption of Cascade H-bridge inverter for T-STATCOM applications causes to decrease the device voltage and the outputharmonics by increasing the number of output voltage levels. This paper presents a T-STATCOM with a PIC controller based twenty five-level CHB multilevel inverter forthe voltage sag, voltage swell and reactive power mitigation of the nonlinear load[1]Solar photovoltaic (PV) fed CMLI is dealt in various literatures, but it intends for lowvoltage and low level A 5-level current Cascaded MLI for grid connected PV system which fed by singlephase is addressed. But the redesigning of LC filter is needed for this which furtherreduces the resistive and inductive losses forgetting higher power levels.Modified multilevel connections (MMCs) to achieve 15 levels and 27 levels,respectively. The three stage CMLI power circuit used to achieve 15 levels by binarymode using digital switching technique comprises of counters and logic functions.The same power circuit is used to achieve 27 levels by trinary mode using embeddedcontroller. In certain literature, voltage balancing, ultra capacitors, PWM switchingand transformers are required which will be the cause for the increase in cost andmanufacturing

problems thereby not desirable for motor drive application. In conventional approach, PWM techniques are used by the comparison of reference and carrier signals to provide the required gating signals for the inverter switches. The number of output voltage levels obtained from this approach is given in the following equation

$$m = 2N_s + 1$$

3. MODIFIED MULTILEVEL CONNECTIONS

THE above two approaches, the modification is realized in control circuit of CMLI to achieve 15 and 27 levels with three inverter stages. In this approach, the modification is made in both control circuit and predominately in power circuit to obtain 15 levels with only seven switches. Fig. 3.shows the circuit diagram of MMC approach where the input scaling is not mandatory.

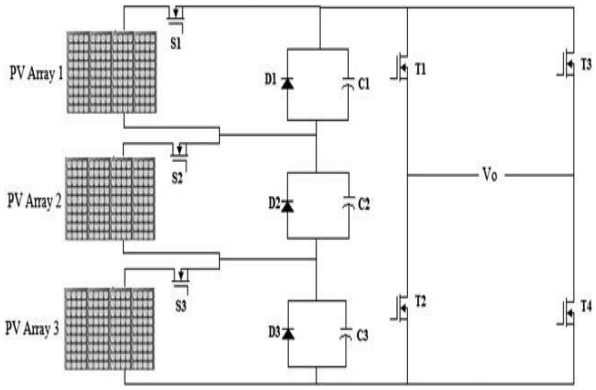
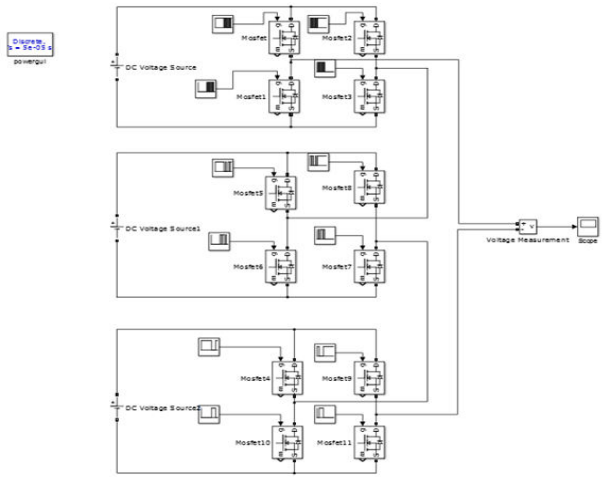


Figure .3Single stage 15-level inverter power circuit

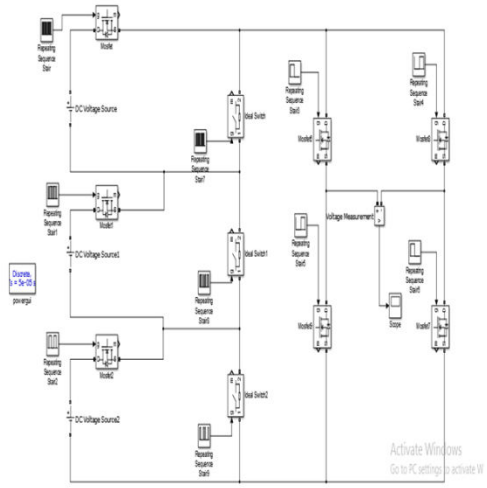
4. RESULTS ANALYSIS

Simulation and Results

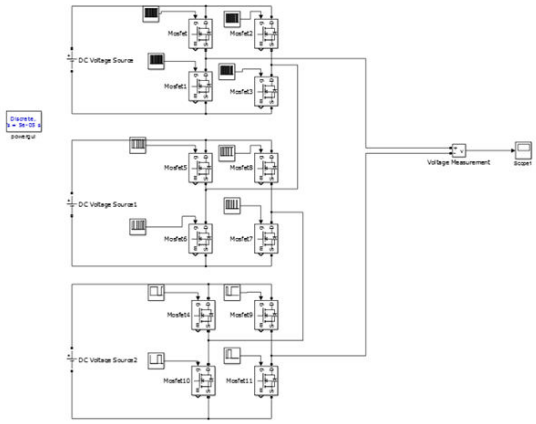
1.Simulink model of Cascaded MLI In binary mode.



2.Simulink model of Cascaded MLI in MMC mode

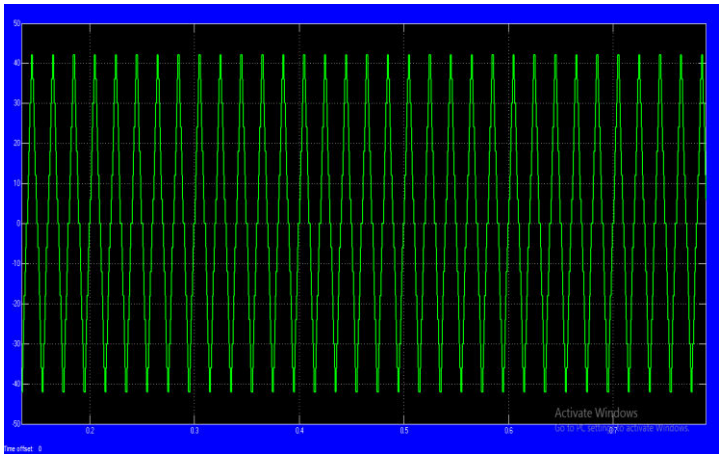


3.Simulink model of Cascaded MLI in trinary mode.

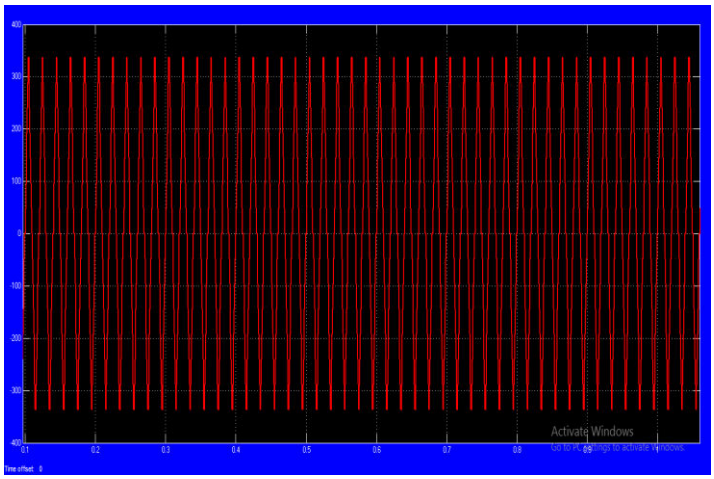


Simulation Results-

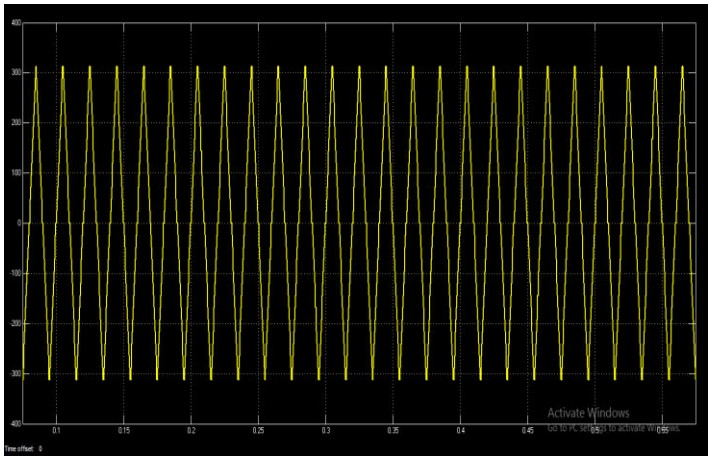
1.Binary mode MLI output voltage.



2.MMC mode MLI output voltage.



3.Trinary mode MLI output voltage.



5. CONCLUSION

In this project, improving the power supply for solar energy in CMLI and reducing the number of semiconductor keys are investigated. The 15-level output must be achieved with only 12 keys in binary mode and 7 keys in MMC mode. In addition, the 27-level output is available in 12 keys via trinary mode. The mathematics of the model for the implemented solar PV is directly related to the phase inverter. Analytical analysis of the study was carried out for the different categories and comparisons were made. A photovoltaic powered 3 kWp CMLI is implemented for all three details of the topology and generated harmonics. Based on the observations, the design method offers many advantages including reduced THD, low cost, simple design, small computational size and lack of transformers, dynamic converters, detailed tables and cleaning departments. Furthermore, these methods are more suitable for standalone / networked PV systems to improve energy efficiency.

6. REFERENCE

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