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REVIEW WORK ON POWER QUALITY IMPROVEMENT USING CASCADED MULTILEVEL INVERTER

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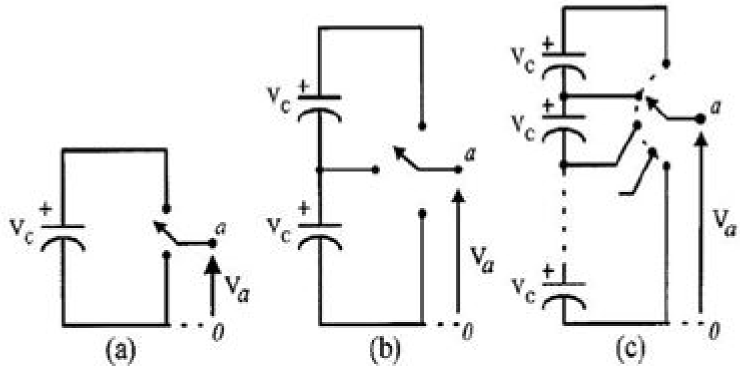
Abstract

Recently, cascaded inverters have been tested for their superior value over voltage source and connector applications. The output of this converter is connected by a cross-sectional filter to create a sinusoidal flow with low harmonics as well as to meet the required network network requirements. The project is designing a new cross-sectional topology for a network connection system that connects a five-phase cable. The optical filter incorporates additional resistance-capacitance and similar capacitors of the inductive-capacitance-inductive capacitor as well as additional resistance to it to reduce energy loss. It can reduce the harmonic frequency fluctuations better than traditional filters and drop the same value applied, reducing power and resistance. Introduce quantitative filters and methods to determine filtered filters. In addition, a new system using Boundary Propagation (PSO) is recommended to ensure that the humidity is reduced and to ensure that the maximum humidity is reduced. In addition, the PSO algorithm for this function is used to raise the attenuation corresponding to the ambient frequency change based on the agreed values and filtering capacitance. A comparison discussion of a transient filter and the recommended filters is obtained from a test conducted on a 110V, 1 kW connected inverter. The volume conversion algorithm is implemented for a multi-variable converter using the SPARTAN 6-XC6SLX25 Processor Processor Processor (FPGA). Studies show that the recommended filters not only provide a reduction in power but can also provide a reduction in noise compatibility with higher frequency, better output output, as well as a lower Harmonic Distortion (THD) potential power level is better for some translators. -netite network - connected network

1. INTRODUCTION

The transformer provides the appropriate mechanism for medium and high power systems to produce an output voltage that allows the harmonic content of the voltage and current waves to be reduced. It refers to a series of connections in multilevel transformers, called "levels", to provide the output voltage at the desired "levels". The increase in phase speed causes a decrease in harmonic damage. Three topologies are selected, such as phase capacitor (FC), zero point (NPC) and multilevel cascade inverter (CMLI) for different applications, depending on the system and the conversion system. Of the three topologies, CMLI is the best choice for renewable energy integration due to benefits such as voltage drop issues, elimination of the DC-DC converter, changes without small frequency changes, interference and diodes.

CMLI photovoltaic (PV) solar power supplies come in a variety of forms, but are designed for processing in low-light and low-temperature conditions. The Sound Amplifier System (PWM) is recommended for CML level 5 and CMLI level 7 for photovoltaic systems that require rotation, auxiliary circuits and multiple signals to generate the pulse. The current CMLI Level 5 of a single PV system is combined with a PV system that requires adjustment of the LC filter to reduce losses and resistance at high power levels. The three maximum power control panels (MPPs) of the five-phase amplifier use an output switch between the inverter and the grid. Although the shrinkage decreases as the level increases, CMLI requires a number of semiconductor switches that must be reduced to reduce losses, costs, complexity and gaps. Series connection of multilevel inverters introduced in restricts its use in high power applications because of the necessity of changing the voltage polarity in every half cycle and also the switches with different ratings are required. A detailed look-up table is required for the method proposed in [7] which consists of series connection of a high-voltage NPC and a low-voltage on ventional inverter. A 5-level inverter with four DC sources comprising two numbers of 2-level and 3-level inverters is proposed in. The drawback of this method is that in conventional inverters upto 9 level can be generated with the same number of power supplies. Bidirectional switches with voltage and current blocking capability for the reduction of switches is proposed in where each bidirectional switch requires a separate gate drive circuit which increases the power loss.



(a)Two levels, (b) Three levels and (c) n levels

Fig. 1 One phase leg of an inverter

2. Topologies Of Multilevel Inverters

Traditional multi-pulse and VSC magnetic fields have become popular systems and have been incorporated into 18 and 48 phase rotations for battery energy storage and STATic CONDenser (STATCON) applications, individually (Walker 1990). These transformers are usually connected to the voltage level by changing the rotational speed of the transformer and complex zigzag connections (Lai and Peng 1996). Magnetic link path problems are difficult, cumbersome, and expensive. Therefore, the capacitor coupling system is preferred over the magnetic coupling system. There are three different transformers depending on the connection of the voltage capacitor, listed as follows:• Diode-clamped multilevel converter

- Flying-capacitor multilevel converter
- Cascaded converters with separated DC sources

3. Flying-Capacitor Multilevel Converter

The Multilevel Capacitor Inverter (CCMLI) or Multilevel Capacitor Inverter (FCMLI) appeared in the 1990s. This figure shows the status of FCMC 5 (Flying Capacitor Multilevel Converter) or CCMC (Capacitor Clamping Multilevel Converter) topology. The current voltage in the FCMC is the same as the DCMC. In this topology, the connection holes of the semiconductor device connected in sequence are blocked by other capacitors. A series of locked capacitors are required to exist, their numbers being selected on each leg so that all capacitors store the same power. That way, no more capacitors are needed. Voltage projects are related to instructions. There is no three -circuit connection between the capacitors Ca, Cb and Cc and the DC communication core for those systems, according to the DCMC topology..

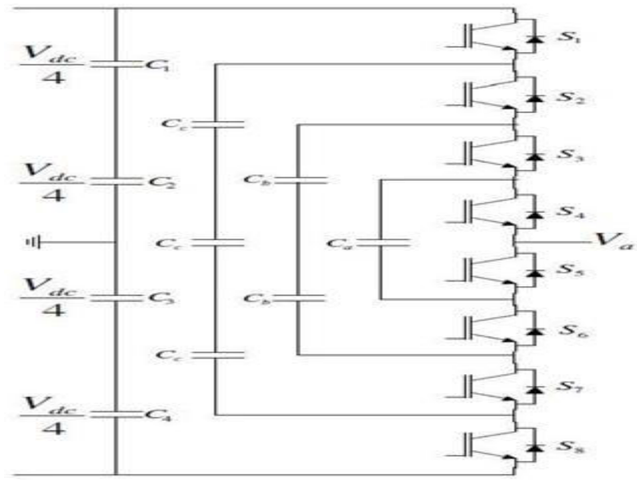


Fig..2 Power circuit of one phase leg of a 5-level FCMC

4. LITERATURE REVIEW

- **A. Rockhill, Graduate Student Member, IEEE, Marco Liserre, Senior Member, IEEE, Remus Teodorescu, Senior Member, IEEE, and Pedro Rodriguez, Member,** IEEE This paper describes the design procedure and performance of an LCL grid filter for a medium-voltage neutralpoint clamped converter to be adopted for a multimegawatt (multi-MW) wind turbine. The unique filter design challenges in this application are driven by a combination of the medium-voltage converter, a limited allowable switching frequency, component physical size and weight concerns, and the stringent limits for allowable injected current harmonics. Traditional design procedures of grid filters for lower power and higher switching frequency converters are not valid for a multi-MW filter connecting a medium-voltage converter switching at low frequency to the electric grid.

- **Jih-Sheng Lai, Senior Member, IEEE, and Fang Zheng Peng, Member, IEEE Multilevel Converters-A New Breed of Power Converters Multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications**. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of dc capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. There are several ways of implementing voltage balance in multilevel converters. Without considering the traditional magnetic coupled converters, this paper presents three recently developed multilevel voltage source converters

- **Rahim, N.A., Selvaraj, J.,2010 „Multistring five-level inverter with novel PWM control scheme for PV application", IEEE Trans. Ind. Electron., , 57, (6), pp. 2111–2123. Multistring Five-Level Inverter With Novel PWM Control Scheme for PV Application** This paper presents a single-phase multistring five-level photovoltaic (PV) inverter topology for grid-connected PV systems with a novel pulsewidth-modulated (PWM) control scheme. Three PV strings are cascaded together in parallel configuration and connected to a five-level inverter to produce output voltage in five levels: zero, +1/2V dc, V dc, -1/2V dc, and -V dc. Two reference signals that were identical to each other with an offset that was equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switches. DSP TMS320F2812 is used to implement this PWM switching scheme together with a digital proportional-integral current control algorithm. The inverter offers much less total harmonic distortion and can operate at near-unity power factor. The validity of the proposed inverter is verified through simulation and implemented in a prototype. The experimental results are compared with a conventional single-phase multi string three-level grid-connected PWM inverter.

5. Proposed Work

The multilevel inverter using cascaded-inverter with separate dc sources (SDCSs) synthesize a favorable voltage from several independent sources of dc voltages, which may be achieved from batteries, solar cells and fuel cells. This structure recently has become very widespread in ac power supply and adjustable speed drive applications.

1) Study and analysis of various topologies of multilevel inverter.
2) To Study control strategy of cascaded multi-level inverter
3) To simulate "multilevel inverter switching and control algorithm" in MATLAB environment.
4) Design and development of Multilevel inverter for the proposed system.
5) Design and development of cascaded multilevel inverter for various operating condition.

6. Modified Multilevel Connections

The above two approaches, the modification is realized in control circuit of CMLI to achieve 15 and 27 levels with three inverter stages. In this approach, the modification is made in both control circuit and predominately in power circuit to obtain 15 levels with only seven switches. Fig. 3.shows the circuit diagram of MMC approach where the input scaling is not mandatory.

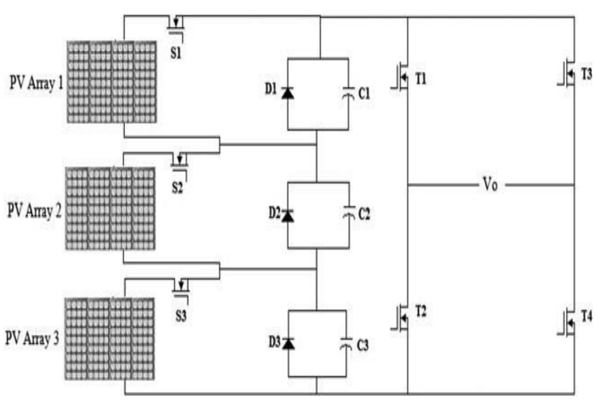


Figure .3Single stage 15-level inverter power circuit

7. Conclusion

In this project, improving the power supply for solar energy in CMLI and reducing the number of semiconductor keys are investigated. The 15-level output must be achieved with only 12 keys in binary mode and 7 keys in MMC mode. In addition, the 27-level output is available in 12 keys via trinary mode. The mathematics of the model for the implemented solar PV is directly related to the phase inverter. Analytical analysis of the study was carried out for the different categories and comparisons were made. A photovoltaic powered 3 kWp CMLI is implemented for all three details of the topology and generated harmonics. Based on the observations, the design method offers many advantages including reduced THD, low cost, simple design, small computational size and lack of transformers, dynamic converters, detailed tables and cleaning departments. Furthermore, these methods are more suitable for standalone / networked PV systems to improve energy efficiency.

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