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2-Bit Comparator design using Quantum Dot Cellular Automata (QCA)

Dr.V. Adinarayana, N. Sravanthi, B. S. S. Sahithi, K. N. Nikhilesh, M. Satish Kiran Kumar

1Associate Professor, 2Student, 3Student, 4Student, 5Student
1Department of Electronics and Communication Engineering, Gayatri Vidya Parishad College for Degree and PG Courses, Visakhapatnam-45

Abstract

Comparator is a hardware electronic device and made up of standard AND, OR and NOT logic gates. This device takes n number of inputs in binary form and determines whether one input is greater than, less than or equal to other input. CMOS Comparators has a major drawback of size and power consumption leading to the failure of Moore's law To overcome this disadvantage, Quantum-Dot Cellular Automata, an emerging Nanotechnology has been implemented. QCA provides faster speed with low power dissipation at nano-scale extent. This project focuses on the design of Quantum dot Cellular Automata (QCA)- based 2–bit comparator with less power consumption in lesser area.

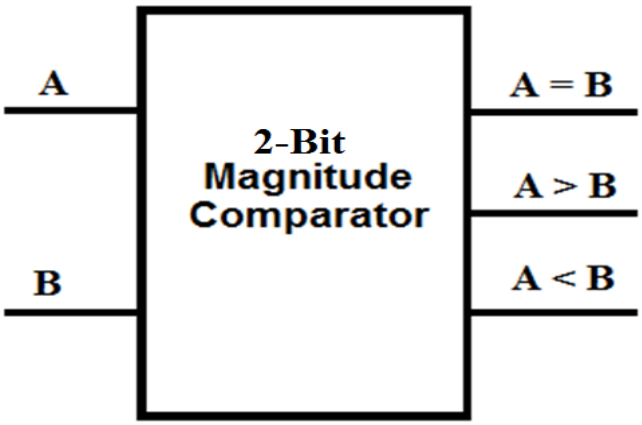
1. Introduction

A few advanced microchips that have been popularized in the 21-st century incorporate decimal number juggling equipment units. This is a reaction to procuring requests for sophisticated calculations which are necessary for cost-saving and mechanical applications. As the preparing requests approach galactic measurements, the PC business is considering the possible development towards new rising advancements to defeat CMOS limitations for execution speed and wide power scattering on limiting the incorporated circuits

The present crucial breaking points in CMOS circuit's calculations and development of quantum mechanical impacts in exponentially as of recently added quantum circuits to another dimensional tending of the electronic group.As a consequence, quantum calculation and data remain an appealing territory of research over the most recent few decades This shows that superior information of quantum mechanics is required.

Quantum dot cellular automata are the processing with cell automata confined with varieties of quantum dots.A QCA cell is a Nano shell device ready to encode data by two electron shape. Current advancement of quantum computing continues from numerous viewpoints; quantum circuit's combination is the massive test in the quantum information handling and the improvement of the quantum PC engineering.

BLOCK DIAGRAM of 2-bit Magnitude comparator



2.1 Background: How QCA charge transfer?

A QCA cell can be seen as an arrangement of four charge vessels or "specks", set in the corners of a square. The cell is pick up accuse of two free electrons which are able to burrow between dots. QCA are exhibited coulomb coupled quantum dot cells. Electrons situated in every cell have characteristic states with characteristic relate charge scattering. The condition of every cell is checked by its significant interaction with adjoining cells [26]. Bury cell barriers entirely repress charge exchange between the cells. The limit condition of last cells which go about as an information and yield cells which rely upon numerous electron frameworks in the composed circuit. Edge cells are controlled by the communication of electrostatic charge.

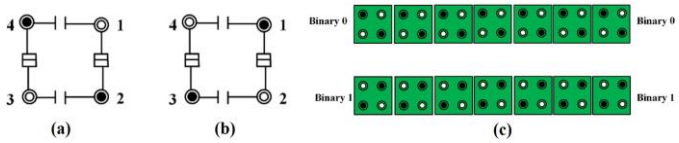
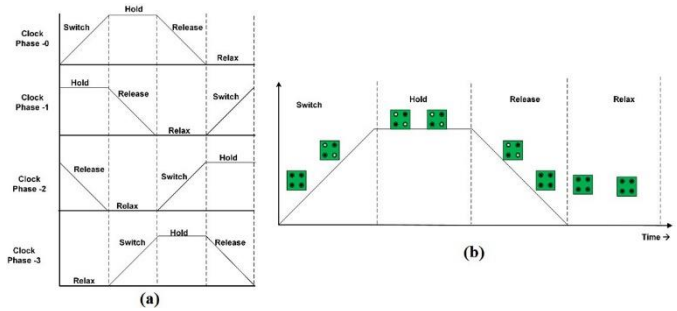


FIG. 1. (a) (b) QCA cell negative polarization denoted as logic "0"; (b) QCA cell with positivepolarization denoted as "1"; (c) QCA wire showing charge transfer

2.2 Clocking

The timing of QCA, follow the semi adiabatic timing system. This system consists of four stages: switch,hold, release (discharge) and relax (unwind). At first, when the potential energy of the electron is low and the electron isn't equipped for burrowing between quantum dots, it has a definite extremity. With the start of the switch stage, the potential vitality of electrons begins to rise and toward the finish of this stage the electron achieves its most extreme potential vitality. Amid the hold stage the electron keeps up its greatest potential energy and turnsout to be totally delocalized losing its polarity. In the discharge stage the potential energy of the electron beginsto decrease and the cell moves incrementally towards a definite polarity. Amid the last stage i.e. the unwind stage the electron keeps up least energy and is excessively powerless, making it impossible to burrow between the dots. Along these lines, the cell achieves a definite extremity.

FIG. 2. (a) QCA cell with clocking;



(b) Propagating of QCA cell in clock zones

The principle contrast between CMOS configuration circuits and QCA configuration circuits is that in the CMOS, the clock flag controls the circuit yield and states, whereas in QCA, the clock is valuable to exchange the charge information from one cell to next contiguous associated cell. On each clock cycle every cell discharge or evacuates its state and each cell in QCA including info and yield cells are clock controlled [13]

2.2 Wire crossing technique

For efficient design of QCA circuit in a smaller footprint, one area of primary consideration is wire crossing. Wire crossing is vital in QCA based plan and numerous strategies have been proposed to outline an efficient wire crossing, for example, coplanar based and the multilayer based methods, recently. Meanwhile the wire crossing strategies utilizing the control of clock stage have also been proposed [14]. Keeping in mind the end goal to outline the wire crossing using the said procedures, extra undertakings ought to be requested, for example, interpretationor rotation of QCA cells control of clock stage, expansion of bigger and soon. Like this their methods requireextra time or spatial intricacy.

1 Coplanar based wire crossing procedure was proposed by Tougaw and Lent is shown in Fig. 3(a) basic geometry of the coplanar based wire crossing system [18, 19]. In this illustration the vertical wire and even wires are transmitting the values of 1 and 0 separately. To actualize this wire crossing the cell of horizontal wire are rotatedby 45 ˚. On the off chance that the length of the vertical wire after a crossing point cell is adequate a transmitting value is not influenced by the other wire [14].]. Likewise, the horizontal wire should consist of an odd number cells, since the property of the rotated cells has an inverter chain that the polarization substitutes heading between neighboring cells. Cells rotated by 45 ˚ initiate the extra space between cells. It inherently diminishes the energy partition between the ground state and the primary energized state which debases the execution of such a device as far as highest working temperature, protection from entropy, and least exchanging time [15].

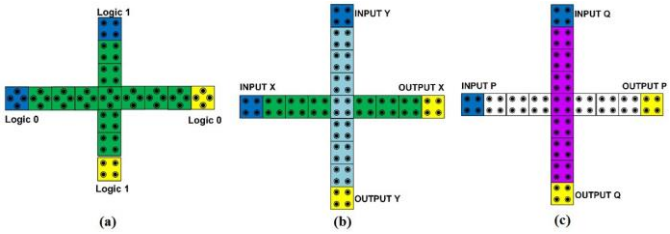


FIG. 3. (a) Co Planar wire crossing; (b) wire crossing using clock 0 and clock 2; (c) wire crossing using clock 1 and clock 3

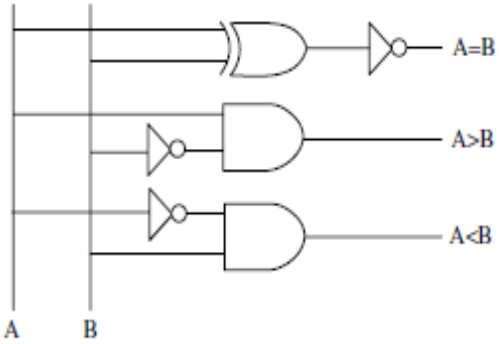
LOGIC DIAGRAM OF 1-BIT COMPARATOR AND TRUTH TABLE

A	B	A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

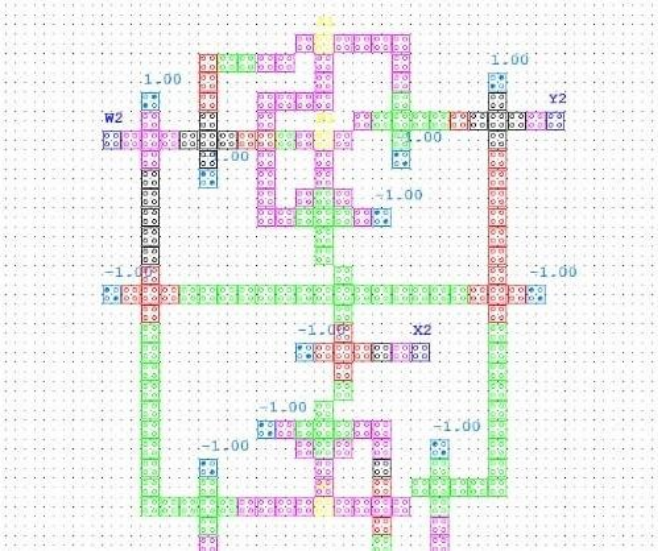
2.3 Simulation results and discussion

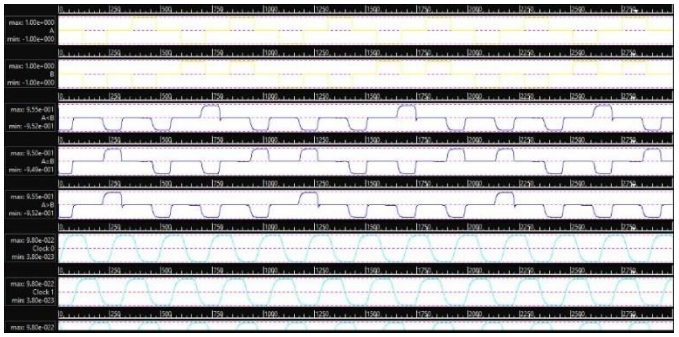
The essential function of a comparator is to regard the magnitude of two binary data to determine their relationship. The EX-NOR gate can be utilized as a fundamental comparator in light of the fact that its output is a 1. On the off chance that the two information bits are equivalent and a 0 if the information bits are not equivalent. we demonstrated 1 bit and 2-bit comparator composed utilizing QCA Design programming with wire crossing uses an inverse clock (180 phase shift) system and actualized with most recent EX-OR entryway. Fig. 5(a, b) demonstrates the 1 bit and 2-bit comparator and planned with fewest number of logic gates. The logic concerns the yield of two bits (A, B) less than (W1, W2), equal (X1, X2), or greater than (Y 1, Y 2) of 1 bit and 2-bit comparator spoke to with logic condition appeared underneath after streamlined with the K-map. The logic for a 1-bit comparator outputs is as follows:

W1 = A 0B

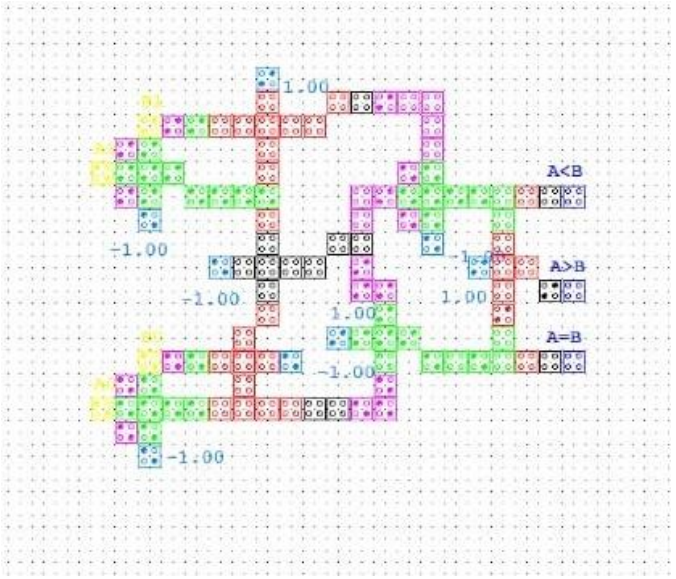


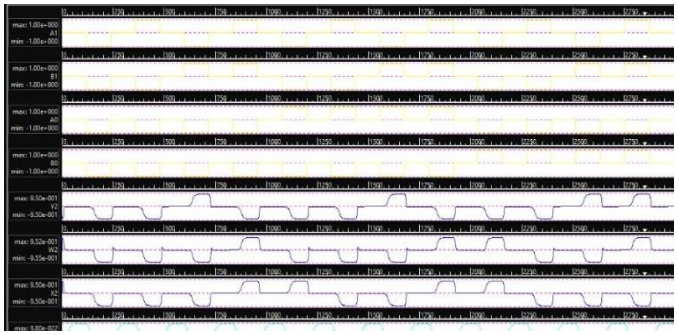
Existing 2-Bit Comparator Design and Result





Proposed 2-Bit Comparator Design and Result





5. Conclusions

The more significant part of QCA combinational circuits with coplanar or multilayer wire crossing it have many-sided outline quality is more. In this paper we proposed a smaller comparator with clock 180-degree wire crossing technique. We composed this QCA design in the QCADesign test system. The proposed 1-bit comparator layout cell count less than 36.84 % of most recent outline and area occupation are less than 2.91 % with delay utilizes just 1/2 clock, whereas the 2-bit comparator possesses range 0.38 µm 2, cell count 203 with clock delay of 1 1/2. Generally, QCA circuits have incredibly noteworthy wiring delays for a quick plan in QCA, many-sided quality imperatives are exceptionally basic issues and the outline needs to utilize compositional systems to support the speed considering these limitations. The QCA innovations once

realized will probably require a change in the outline rules. These outlines utilized the given particular plan rules, however as in a CMOS plan they can be scaled in a similar manner. This provides a chance to contrast the abnormal state outline engineering and in QCA circuits.

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