64-BIT ALU DESIGN USING VEDIC MATHEMATICS

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***Abstract*—This paper presents the design details and implementation of FPGA results of 64-bit ALU based on Vedas such as Urdhva Tiryakbhyam and Nikhilam. After performing the Veda calculation, the equation reached the result in 4.014 seconds. Xilinx Spartan FPGA products complete the ALU module written in Verilog HDL. Play After checking the balance process in detail, the Xilinx ISE 12.3 program is used to get the results. The results show that: More work can be done using Vedas. Application of Arithmetic 85**

***Index Terms*—Vedic mathematics, FPGA, Vedic Multiplier, MAC, and ALU (Airthematic Logic Unit) Design**

I. INTRODUCTION

One of the arithmetic operations is to multiply one number by another. Operations such as multiplication are essential functions used in many DSPs today applications such as convolution, FFT, filters, and ALU (arithmetic logic unit) microprocessors. Repeatedly the preferred operation is multiplication, so it needs to be developed multiplier, which reduces latency and uses power efficiently. Arithmetic calculations are used in many tasks. from simple everyday tasks such as calculations or counting, to complex scientific and business calculations. so fast and efficient calculations are required. devices of computers. Takes less time than array multiplication. A parallel computation method for partial multiplication. Delay Generates the time required for the signal to pass Multiply the array gates [1]. Use of Booth multipliers Large Booth arrays for designing multiplier and exponentiation calculations at the simple speed required for continuous... Ancient formula (eˆ²½) It provides a way to find the product of N x N, N bits respectively. Consider the multiplicand, the smaller part (N/2 = n, Let's say. This part is again divided into smaller parts. We use numbers (n/2 each) until we reach the size of 2x2. So this Simplifies the task of tree structure. ALU can perform various logical operations including: Not, AND, OR, NAND, NOR, XOR and XNOR Efficient adders in the arithmetic logic unit can help. Build high-performance systems with low power consumption. Also, the basic equipment for addition and subtraction is Multiplication is closely related and often includes: Use addition for the operation. Various adder families Have been proposed in the past to balance power, area and Speed is aˆaˆpotentially available in the ALU. Implementation of dynamic adders is important for the following reasons. Importance of ALU performance. Dynamic logic families are Known to be efficient in terms of transistor count, They use additional logic and It uses it to implement the same adder block. Logical subtractor blocks are specifically designed for these operations. The logic block uses the selected lines to drive the multiplexer (MUX) and determines the specific logical operation to be performed. For the shifter and comparator blocks, additional logic is used to evaluate the inputs and create a 1-bit comparator that provides three output states under different circumstances. Additionally, a 2:1 MUX is created that is used as a cell in the cylindrical shear for rotation and shear operations. When considering the design of low-power ALUs and 4:1 multiplexers, it is important to note that the latency can increase significantly, resulting in reduced speed, increased silicon area, and increased power consumption due to complex routing and larger interconnects. The choice between parallel or serial multipliers depends on the nature of the application, as each type has its advantages and disadvantages in terms of speed, area, and power consumption.

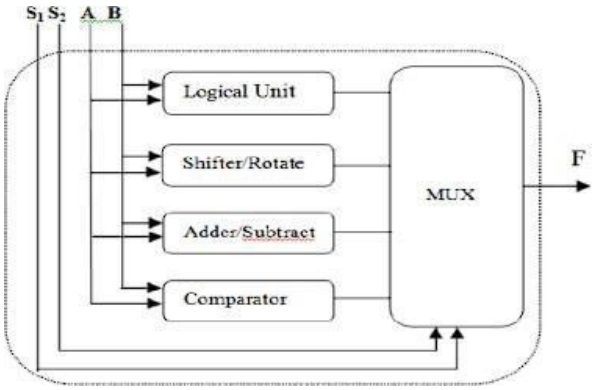

Fig. 1. internal Architecture Of ALU

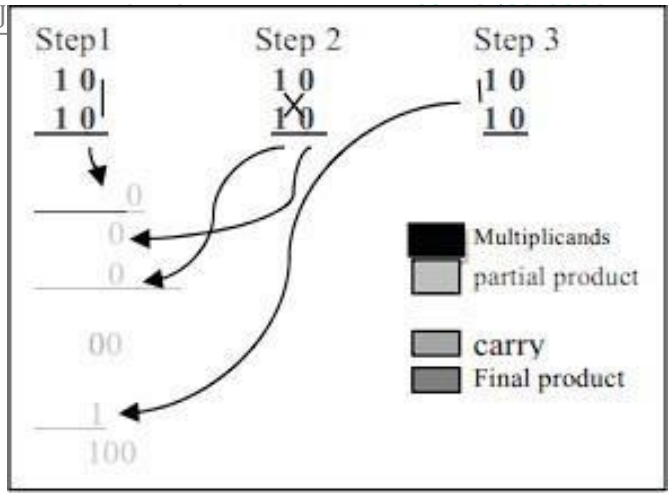

Fig. 2. 2X2 Bit Multiplication Using Vedic Sutra

II. DESIGN

The arithmetic module is divided into smaller modules, such as a multiplier, a MAC block, and an arithmetic module. These three modules are implemented using Verilog.

A. MULTIPLIER USING VEDIC SUTRAS

A 2x2 bit multiplier is obtained using ”vertical crossover”. The algorithm” is based on Urdhva Tiryakbhyam Sutra. Base 2x2 bit multiplier is first designed using Verilog code, 4x4 block is developed using 2x2 block, then 8x8 bit is developed. 4-bit multiplier block’s multiplier and finally 16x16-bit multiplication is obtained using finite 16-bit. Multiplier[3,4,5].

B. MULTIPLIER OF 2x2 BIT

The multiplier contains a 2-bit multiplicand and a multiplier, both of which produce a 4-bit product. For different inputs Combinations of 2-bit values .Produce different results. (0000, 0001, 0010, 0011, 0100, 0110, 1001). The multiplication takes place as shown in the figure. 1. Here The multiplicand ”x” and the multiplier ”y” are equal to (10). Using Urdhva Tiryakbhyam Sutra, the resulting product is: (0100). Step 1: Multiply the least significant digit of each multiplicand vertically. Step 2: Cross-multiply high bits Step 3: Vertically multiply the sum with the high order By the common carry obtained in Step 2.Fig-2

C. MULTIPLIER OF4X4 BIT

Four 2x2 multiplication blocks are used in the development. Bit multiplier of size 4x4. (n=4) bit multiplier Generates an 8-bit multiplication result. Smaller parts of both Inputs a and b, which are 4/2 = 2, are multiplied using: The 2x2 multiplication blocks already developed. Therefore, The 4-bit results are added using an addition tree as follows: Rice. 2. The Wallace tree addition method reduces the addition level from 3 to 2 instead of sequential addition. The least significant 2 bits of q0 are passed as output, and the most significant bit of q0 is fed into the addition tree. Bits, The additional inputs to the tree are detailed in Figure 3. A multiplier, a 64x64-bit multiplier is

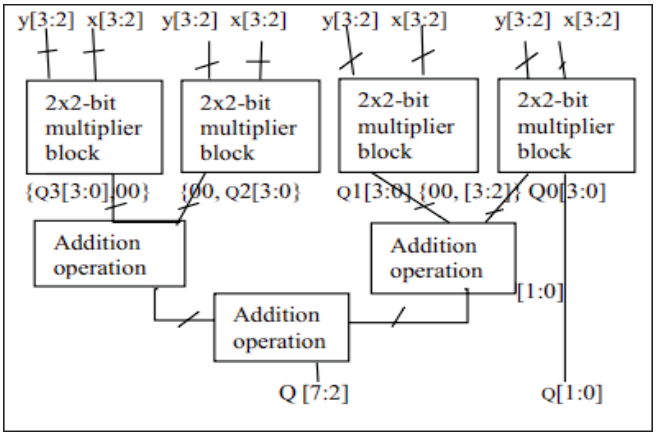

Fig. 3. 4x4 Bit Multiplication Using Vedic Sutras

implemented using: The same method as a 4x4-bit multiplier. 8x8 bit multiplier, 16x16 bit multiplier, 32x32 bit

D. MAC UNIT

The 64-bit MAC block uses a 64x64 Vedic multiplier. Data transfer path. Since the Vedic 64x64 multiplier is faster than others, the multiplier such as the Booth multiplier, the MAC block is faster. In the MAC block, the inputs A and B are 64 bits wide and the output is as follows: It is stored in a 128-bit register to provide the input data. The 64-bit result is then transferred to another adder. Register [6]

E. AIRTHEMATIC MODULE

The arithmetic module uses four components: Adder, Subtractor, Multiplier, and MAC blocks. As a result, the arithmetic block can perform fixed-point addition, Subtraction, multiplication, and accumulation and multiplication 64-bit data [7]. The arithmetic block is built using the usual Adder and

S0	S1	Modules
0	0	Adder
0	1	Subtractor
1	0	Multiplier
1	1	Multiply Accumulate Unit

Fig. 4. Tabel control line for Airthematic Module

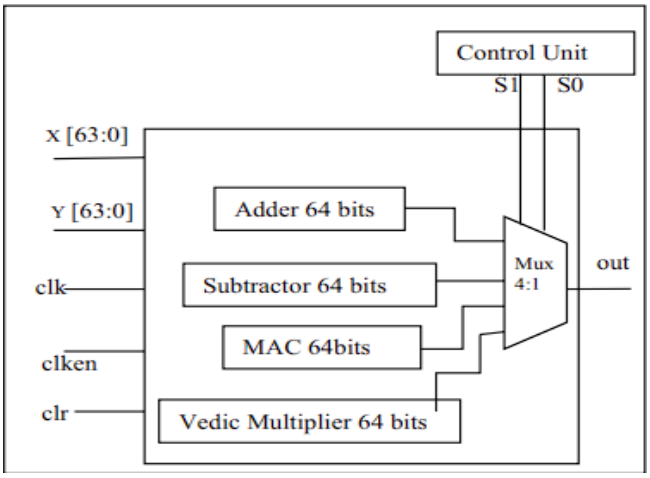

Fig. 5. Block Diagram OF 64-Bit ALU Design

Subtractor, Multiplier, and MAC blocks Vedic Mathematics scriptures. Two control lines Used for various operations as shown in Table fig-4.

III. IMPLEMENTATION

Multiplication is an arithmetic operation involving two numbers. Numbers. Multiplication is one of the most frequently required operations that are now essential in many DSPs for these applications, such as convolution, FFT, filters, and microprocessor ALUs (arithmetic-logic units). Multiplication is often the chosen process; therefore the multiplier should be designed with minimal latency and optimal power consumption. Arithmetic calculations are useful for a wide range of tasks, from simple everyday tasks to complex scientific problems and economic calculations. For this reason, computers require efficient and fast computational units. To get the work Two binary values, a binary multiplier can be used. Digital electronic devices as electrical circuits, such as computers. A binary multiplier is used to: Copy the standard multiplication procedure. The multiplicand The value of each bit multiplied The multiplier, starting with the smallest Considerable. A 2-bit binary multiplier can be implemented using two half-adder (HA) modules. The computer can A variety of mathematical operations that apply digital multipliers. Many of these methods involve calculating subsets. Product and then adding all the parts obtained after. Product. Binary multiplier 2x2.

A. ADDER

It can be created using standard AND and Ex-OR gates. A simple binary adder circuit that can add two 1-bit binary values, A and B. When we add these two numbers, we get two output values, the SUM of the addition and the CARRY bit. or carryout (COUT). Binary adders are commonly used in calculation and arithmetic circuits. Let's look at the basics. Below we add two decimal (base 10) integers. 123 A (add) 789 B (add) 912 SUM In math class, we learned how to add a whole column of numbers. Starting from the right, each number is given a weighted value based on its position in the column. If the sum is greater than or equal to 10, a carry is generated when all the columns are combined. Add the numbers and do basic school arithmetic. This carry is then added. The result of adding the next column to the left Soon. The concept of adding binary numbers is similar to this. Adding decimals, but in this case, a carry is generated. This is only possible if the result of the column is greater than or equal.

B. BINARY ADDER

When adding binary numbers, the rules are similar to addition. In decimal, the only difference is that The largest number. If the sum of two binary numbers is more than 2 (1 1), a carry is generated. This carry bit becomes 'CARRY' and is added to the next column, and soon. Be careful of the carry bit when adding.

C. HALF-ADDER

A half-adder is a logic circuit that adds two binary numbers. It produces binary numbers in the form of sums and divisions. The truth table of a half adder shows that the AND gate produces a carry (Cout) and the XOR gate produces a SUM (S). Boolean half adder representation: However, the main disadvantage of a half adder circuit is that: In the previous diagram, if you add multiple "transfers" data bits. This limitation becomes apparent when you try to add two 8-bit data bytes because there is no carryover from the previous addition.

D. FULL-ADDER

A full adder is a logic circuit that adds three binary numbers. It generates a carry that is passed. The following addition sequence is similar to a half adder. Next, transfer The more significant digit is called carry, and internal carry is the potential carry of a less significant digit. A full adder can be thought of as two half adders connected. In various ways, the first half adder transfers the carry to the next. Second adder. Since a full adder circuit has two half adders, They are inherently connected and the truth table for completeness The adder includes an additional column that records the amount. Input and C IN input.

E. N-BIT PARALLEL ADDER

To create a serial carry adder, you would connect: Cascading 1-bit full adders to add two n-bit values. A portable adder is simply a cascade of 1-bit full adders, each of which is an

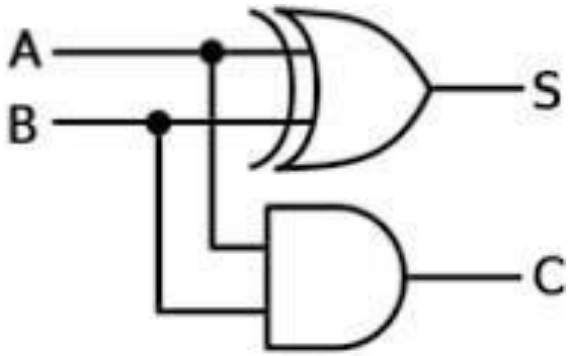

Fig. 6. Half-Adder

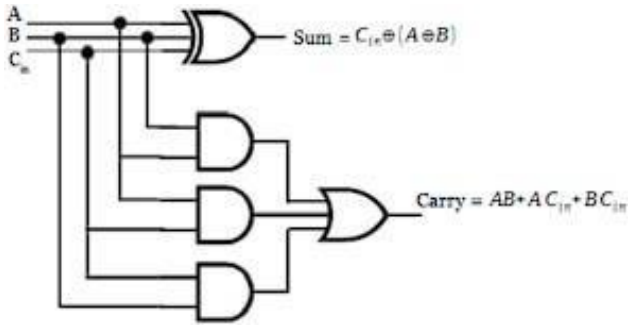

Fig. 7. Full-Adder logical Diagrm

extended binary addition: One weighted column. This is called a serial carry adder. Carryover causes the signal to shift from right to left (LSB to MSB) creating a 'ripple effect' through the binary adders. For example, if you wanted to 'add' two 4-bit values, you could use: Using the output of the first full adder as the input.

IV. VEDIC MULTIPLIER

Vedic multiplication is performed using Vedic mathematics. Multiplication and requires fewer hardware components. It Uses Urdhva Tiryakbhyam sutra. Vertically and horizontally. Block diagram of 32-bit Vedic The multiplier is shown in Figure 6. The two input bits are separated into two halves, and the calculation is Vertical and cross multiplication is performed using inputs A[31:0] and B[31:0]. The intermediate stage addition design uses two adders. As shown in Figur. The product of these two adders Then it i used as input to another RCA. If the sizes do not match, If they are the same, the bits are combined. This is a picture 32-bit Veda multiplier

V. SUBTRACTOR

Subtraction is a simple arithmetic operation performed on a digital computer. It involves subtracting one number from another to find the difference. Numbers are in meters. 6. Vedic many grains. 7. minus meter. 8. Partial Subtractor Dial another number to subtract. H. Half Subtractor A half subtractor is a combination of several factors. A loop that subtracts two 1-bit

Multiplication method	Delay
Booth	37ns
Array	43ns
Karatsuba	46.11ns
Vedic karatsuba	27.81ns
Vedic Urdhva Tiryakbhyam	4.014ns

Fig. 8. Block Diagram Of Vedic Multiplier

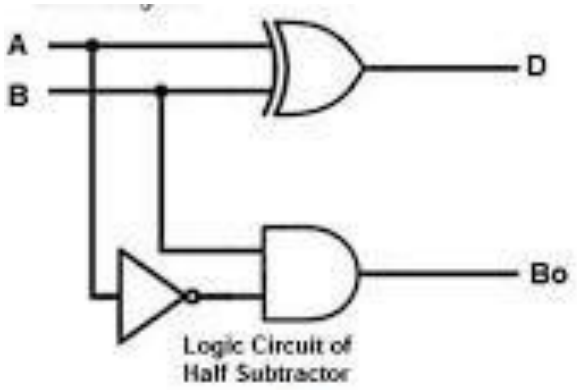

Fig. 9. Half-Subtractor block diagram

binary numbers. number. It has two inputs and two outputs. The two inputs correspond to two 1-bit binary numbers, and the two values correspond to the difference bit and the borrow bit (the difference between the numbers and the half plus obtained). You can see the difference from the facts. The output of half subtraction is the same as the output of XOR (same as the output of half addition). So partial subtraction is also done by XOR gate using AND gate. It works by using one inverted input and one output. The logic circuit of the half-adder is as follows. Next picture. This circuit is similar to a half-adder. The only difference is that the decremented input A is added before feeding the AND gate to complete the credit. In multi-digit subtraction, subtraction of two numbers must be done by subtracting the previous number. Therefore, the subtractor must have three inputs, which is impossible. as a partial subtractor. Due to this limitation, semi-subtractors have few applications and are not widely used in practice.

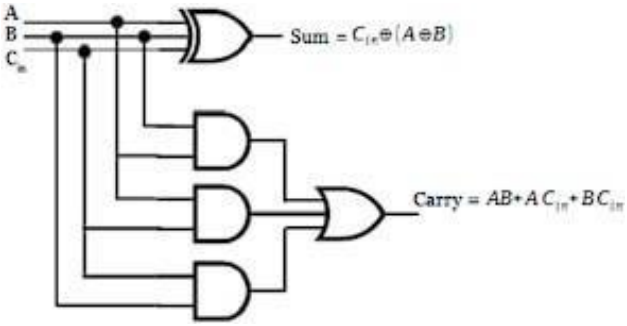

Fig. 10. Full-subtractor

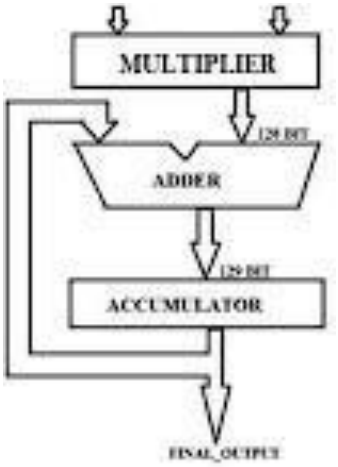

Fig. 11. Block Diagram Of MAC

A. MAC

The MAC unit is a key component in many Digital Signal Processing (DSP) applications that require equalization and integration. It is used to drive high-speed digital DSP systems that include internal devices, filters, convolution, and other operations. Nonlinear functions commonly used in DSP technology include the discrete wavelet transform (DWT) and the discrete cosine transform (DCT). fast. Equalization and summing techniques are specific to digital filters. The simple use of the MAC unit allows for fast filtering and other specialized DSP functions.

VI. SOFTWARE REQUIREMENTS

Verilog behavioral descriptions can be used to create logic-circuit architectures directly using Verilog synthesis tools. These tools help to convert Verilog into physical hardware. With Verilog, we can design, simulate, and synthesize a wide range of hardware, from basic combinational circuits to entire microprocessors on a single chip. Verilog HDL is a standard language for describing hardware, offering many useful features for hardware design. It is a user-friendly and easy- to-learn hardware description language with a syntax similar to the C programming language. Designers familiar with C programming will find it easy to understand Verilog HDL. Additionally, Verilog HDL allows for combining multiple layers of abstraction within a single model, giving designers the flexibility to specify various levels of detail in their designs

VII. RESULTS

A. RTL-schematic

The transfer level list (RTL) diagram is the most important part of the design. It is used to ensure that the project planning is done according to the best architecture that has not yet been developed. Hardware Description Language (HDL) is used to convert the description or details of the design into functional

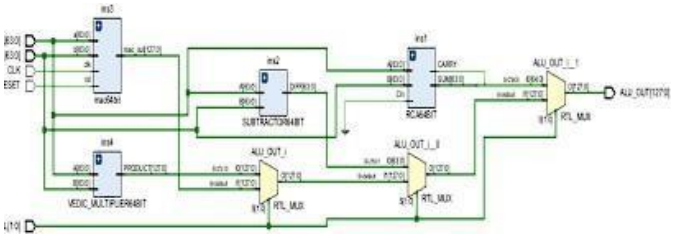

Fig. 12. RTL-schematic Diagram

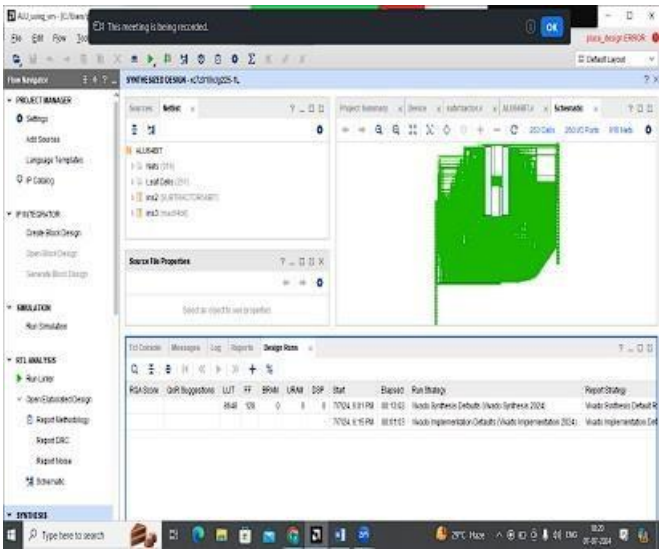

Fig. 13. RTL-Technology Schematic

details using Verilog coding language. Central connections are also listed in the RTL diagram to develop the description. The RTL diagram of the project plan is shown in the figure below.

B. TECHNOLOGY-SCHEMATIC

The architecture is schematically defined in LUT format and LUT is used as a parameter by VLSI to evaluate the architecture design. The memory allocation of the code is represented in LUTs of FPGA which are treated as square units. Technical schematics represent the architecture in LUT format where LUT is treated as a metric to measure the architecture design in VLSI. LUTs are treated as square units and the memory allocation of the code is represented in LUT in FPGA.

C. SIMULATION

Simulation is the final check of how the system works, while the schematic is the check of individual blocks and connections. To open the simulation window, you can switch from

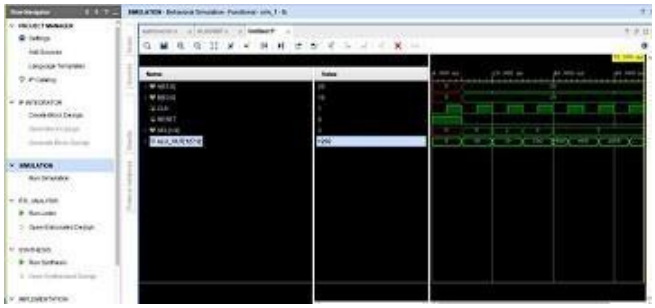

Fig. 14. RTL simulation

Multiplication method	Delay
Booth	37ns
Array	43ns
Karatsuba	46.11ns
Vedic karatsuba	27.81ns
Vedic Urdhva Tiryakbhyam	4.014ns

Fig. 15. Table for Delay Comparisons for Different Methods of Multiplication

the device's main screen to the simulation. The simulation window shows the output in a nice waveform, let's use more basic systems

VIII. CONCLUSION

The design of 64-bit Vedic multiplier, 64-bit multiply-accumulate unit and 64-bit arithmetic module was implemented by Spartan Components. The computation time of the Vedic multiplier is 4.014ns. The computation delays for the MAC unit and arithmetic unit are 10.9ns and 10.248ns respectively, which clearly shows the performance increase. Urdhva Tiryakbhyam Sutra is an effective equation algorithm. Urdhva Tiryakbhyam and Nikhilam sutras help in reducing the time delay, energy, and material in the study. A slow comparison of different multiplication methods is shown in the table.fig-15

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