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8-bit 250 MSPS Two-Step Flash ADC ASIC Design

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Abstract - Low power consumption and a high data rate are requirements for modern wireless communication devices. Analog-to-digital converters are the essential parts of the portable device that serve as an interface between the analog and digital domains. Low-power approaches for high-speed applications are becoming more and more important as the market for portable devices grows. Small feature-size processes can help cut down on power consumption. However, process variances and other factors impact the device's performance as power consumption decreases. The three main needs for portable devices are low power consumption, medium resolution, and high speed. The design of an 8-bit 250 MSPS ADC is the project's objective. This ADC ASIC is a mixed signal. This ADC ASIC is mixed signal. This design uses a subranging type 2-step flash ADC architecture. The 4-bit flash type ADC is designed in two stages. Sample and hold block, comparator block, op-amp, bias circuit, and TGB encoder make up the ADC design. A versatile operational amplifier (op-amp) is developed that can be employed in three distinct ADC modules: S/H amplifier, Subtractor, and Residual amplifier. Upon thorough examination of various op-amp topologies in relation to the provided specifications, the Two Stage Folded Cascade topology was chosen. The Cadence Virtuoso 6.1.5 spiced simulator was utilized for the design, implementation, and analysis of the ADC in 180nm technology.

***Key Words*:** optics, photonics, light, lasers, templates, journals

1.INTRODUCTION

Most signals found in the real world are analog, such as voltage and current. To enable a computer to process, transmit, or store information, this signal must be transformed into digital form. Analog to Digital Converter is used to accomplish this conversion [1]. One of the key elements of a communication system and signal processing system is the analog to digital converter. Anytime analog signals are needed again, a digital to analog converter is needed.

When designing an electronic system that processes analog data using digital logic, the analog to digital converter is a crucial component [2–5]. These devices are getting smaller every day, despite their increasing functionality

ADC can be classified in terms of speed and accuracy as:

1. Low-to-medium speed and high accuracy
(i) Integrating Oversampling ADC [8, 9]
2. Medium speed and medium accuracy
(i) Successive Approximation ADC [10-12]
3. High speed and low-to-medium accuracy
(i) Two-step Flash ADC [13-17]
(ii) Pipeline ADC [18]

Microwave radar and signal processing use two-step flash ADC because of its higher speed and better accuracy requirements.

Sample and hold, comparator, op-amp, bias, TGB encoder, subtractor, residual amplifier, and DAC blocks are the components that make up this circuit. The implementation of the Op-amp is the main design requirement. Thus, the task began with designing the op-amp in accordance with the specifications. Another important component is the comparator. The Clocked Comparator configuration is used to implement it. To analyze the comparator's performance, a number of parameters are calculated, including speed, offset, and delay. Op-amps must adhere to space application requirements regarding slew rate, gain bandwidth product, CMRR, and offset voltage.

2. Body of Paper

Prior to selecting an Opamp, one must determine which particular parameters are most important for the given application

2.1.1 Parameters of Opamp

1. Offset Voltage

The input offset voltage is required to balance mismatches caused by unavoidable process variations. It is a small voltage that sits between the op-amp's inverting and non-inverting inputs. Vos is the acronym for this. Vos is modeled as a non-inverting voltage source that supplies power to the input.

2. Common mode gain

The common-mode gain quantifies how much the output fluctuates in response to changes in the common-mode input level. The ideal common-mode gain of an op-amp is zero. The amplifier should only amplify the differential-mode signal, ignoring the common-mode level.

3. CMRR

The common-mode rejection ratio, or CMRR, is an important design parameter for operational amplifiers. By dividing the differential-mode gain by the common-mode gain, it can be computed. The CMRR of an amplifier should ideally be infinite. In actuality, designers strive for CMRR > 60 dB, though certain applications may require much higher values. The bias point of the in-put differential pair is influenced by the common-mode input. Because of the intrinsic mismatches in the input circuitry, the offset voltage varies, affecting the bias point and ultimately the output voltage.

4. PSRR (Power Supply Rejection Ratio)

Although it shouldn't, the output of an op amp typically does change when the supply does. If adjusting the supply by X volts causes the same output change as adjusting the differential input by Y volts, then the PSRR on that supply is X/Y. The definition of PSRR presupposes that both supplies are altered equally and in opposing directions; if not, the analysis will become more complex and include both a supply change and a common-mode change. This effect results in observable differences in PSRR between the positive and negative supplies.

5. Slew Rate

The rate at which a step input modifies the output voltage is known as the slew rate (SR). The units it employs are / . AC analysis is used to determine the small-signal bandwidth of the op amp. Large signal effects, such as slew rate—the fastest speed at which an operational amplifier can charge and discharge its load—limit the speed of amplifiers. As shown below, configure the op amp as a unity-gain buffer in order to measure slew rate.

6. Unity Gain Bandwidth

The unity-gain bandwidth (B1) and gain bandwidth product (GBW) are very similar. In an open loop configuration, GBW denotes the output loaded and the gain-bandwidth product of the Op-Amp:

=

The frequency at which the Op-Amp's is 1 is indicated by B1.

7. -3dbSmallSignalBandwidth

An operational amplifier's -3 dB bandwidth typically exceeds its full power bandwidth due to reduced signal swing. The bandwidth grows as the Vp decreases.

8. Rise Time and Fall Time

For high-speed op amps, we may also have rise and fall times specified. Though there is usually some variation in practical operational amplifiers, they should all be the same. Rise and fall times are calculated by feeding a square wave into an op amp and monitoring the output waveform. This has a close relationship to the slew rate. To avoid overshoot and ringing, we typically take measurements between 10 and 90 points, as is done for slew rate. The input wave is usually full scale, but on rare occasions, a smaller input signal may be required.

9. Phase Margin

The phase margin at unity gain (fm) is the difference between the amounts of phase shift a signal experiences through the Op-Amp at unity gain and 180∘.

=180∘ − 1

To ensure stability, any amplifier's phase margin should be at least 45∘ C (ideally 60∘ C). A phase margin below 45∘ C leads to longer settling times and propagation delays. The Op-Amp system can also be thought of as a simple second order linear control system, where the phase margin directly affects the system's transient response.

The phase margin can be measured using the following steps in the Cadence design tool:

1. Get the AC response simulation.
2. Delete all outputs from the ADE window.
3. Select the AC response curve, which will turn yellow.
4. In the Analog Design Environment (ADE) window, navigate to Magnitude and Phase.
5. Follow the prompt at the bottom of the schematic window to select the output node.
6. From the ADE window, plot the data.
7. You will receive the magnitude and phase frequency responses. Split the graphs.

10. Gain Margin

The difference between gain at unity and gain at 180°C phase shift is known as the gain margin. =1− @180∘Cphaseshift

11. Settling Time

The signal propagates through the internal circuitry of an op-amp in a finite amount of time. As a result, a step change in the input signal causes the output to react slowly. Typically, the output exceeds the desired value, exhibits damped oscillations, and eventually settles at a final value.

The amount of time needed for the output voltage, given a step input, to settle to within a given percentage of the final value is known as the settling time, or ts. When signals are changing quickly, data acquisition circuits are designed with settling times.

High gain Op-Amp must be provided by ADC for high speed. High-end Op-Amp specifications are only appropriate for requirements involving space. A few specifications are given in the table below.

Table 1: Opamp Specification

Sr.no	Parameters	Required Value
1.	Gain	≥55
2.	UGB	≥400
3.	Phase margin	≥50∘C
4.	Slew rate	≥250/.
5.	CMRR	≥50
6.	PSRR	≥45

The Op-Amp's stability under various conditions, such as temperature and supply, is verified by a number of parameters, including phase margin and gain margin. Computed are additional parameters, such as the CMRR and PSRR. The listed specification value is ascertained by means of the literature review. To meet this need, several Op-Amp topologies are employed here.

2.2 Telescopic Cascode Amplifier

When compared to other topologies, telescopic opto-amps provide low power. Because there is less offset with a telescopic optoamp, the output swing is limited.

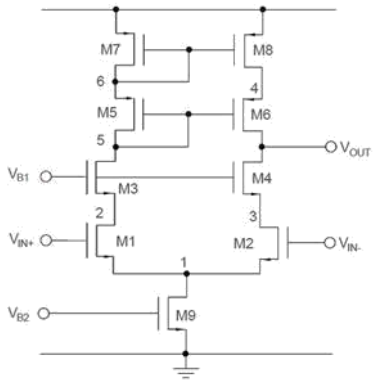

Figure 1: Telescopic Opamp

The M9 transistor limits the voltage swing at the telescopic Op-Amp's output. The telescopic Op-Amp schematic is displayed in Fig. 3.1. To produce a steady current at the load, it consists of a differential input pair and a current mirror load. High gain is possible with this configuration. Adding more loads is not a good idea because it will worsen the output voltage swing.

The Op-Amp current mirror load implementation, which changes the differential input to a single ended output, is shown in Fig 2. Phase margin and gain of an Op-Amp are restricted by the M12 transistor.

2.3 Two Stage Opamp

An op-amp is a kind of two-stage amplifier in which the first stage increases gain and the second stage increases output voltage swing. During the transfer function, two poles are closer to one another, which results in design instability.
To eliminate this, Miller compensation is used. Miller compensation has the lowest offset of any compensation configuration and never reduces performance relative to gain.

In this instance, differential can be used as the first stage, but CS, which offers a much larger swing, must be used as the second stage. Consequently, each stage generates a single pole response and is a gain stage. The design may occasionally have a buffer stage, also known as a third stage. This stage is usually not used with capacitive loads. When an op-amp receives compensation for negative feedback, stability is maintained. 2.4V biasing is not required; 1.65V biasing is. The design needs to be resistant to parameter changes because its primary function is to be fabricated. For this reason, a trustworthy source is needed. The internal supply voltage should be the one producing the bias.

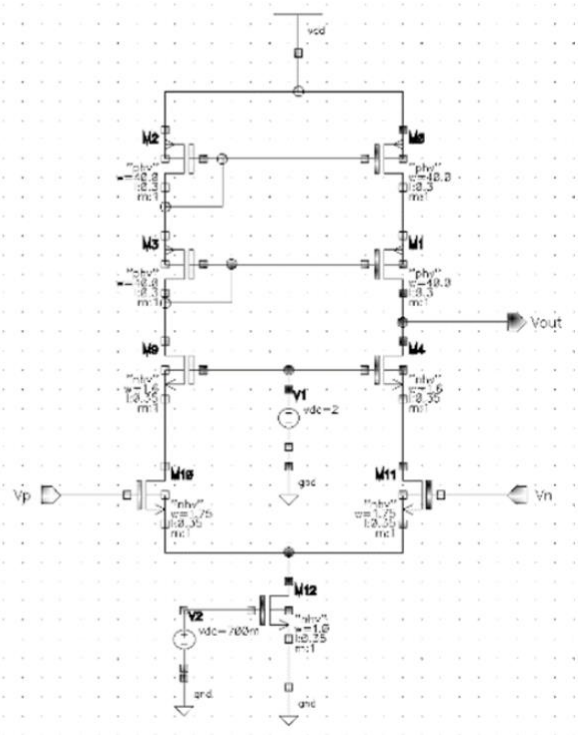

Figure 2: Schematic of telescopic opamp

2.4 Folded Cascode Amplifier

A folded cascode Op-amp combines a gain-boosting amplifier with a two-stage Op-amp. It combines these two benefits into one. A differential input pair on a folded cascade operational amplifier can drive a special current mirror sink. Figure 3.7 displays the Op-amp schematic.

High end balance is required at the differential amplifier's input for a folded cascode op-amp. Here, the transistor drains are linked to one another to provide the differential amplifier's common mode voltage input. Here, bias currents I3, I4, and I5 are de-signed to prevent the current in the mirror from ever reaching zero. There is also an additional delay when the sink's current is zero.

The parasitic capacitance causes it to turn on slowly.

An Op-amp operating at a maximum gain bandwidth of > 500MHz is required for an 8-bit ADC operating at 250 MSPS. In section 4, additional parameter computations are displayed.

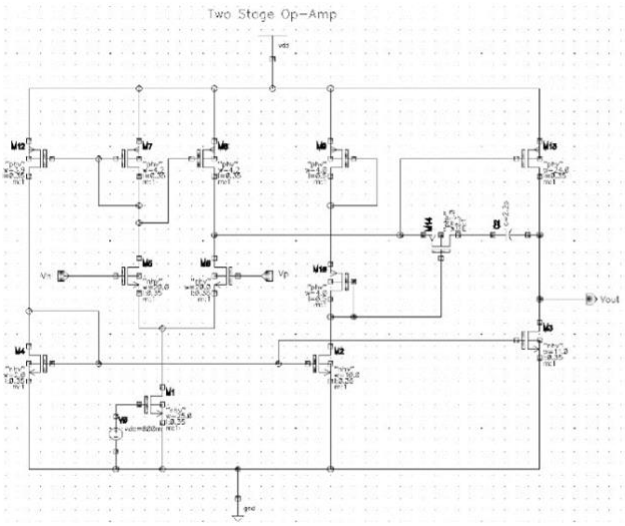

Figure 3: Implementation of Two Stage Opamp

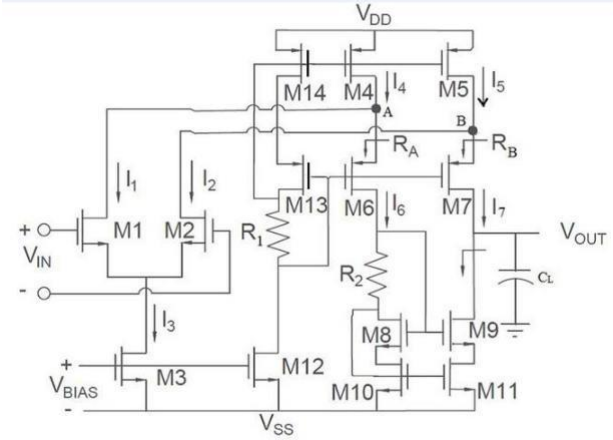

Figure 4: Folded cascode opamp

The benefits of the current mirror sink include reduced power dissipation, self-biasing, and smaller saturation voltage. The Folded Cascode Op-Amp schematic diagram, created in Cadence Virtuoso 6.1.5, is displayed in Figure 5. Here, during the fabrication process, a transistor is used in place of a resistor. The bias circuit schematic diagram is displayed in Figure 6.

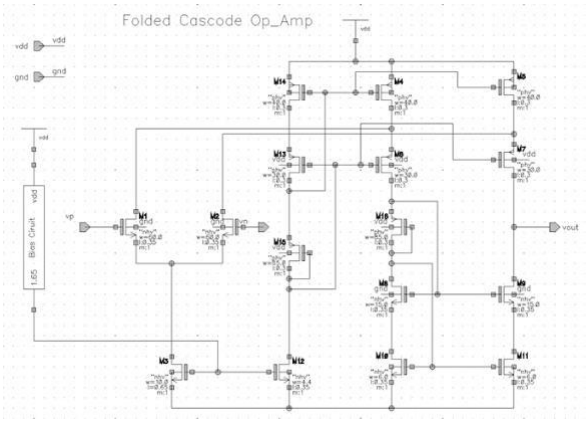

Figure 5: Schematic of Folded cascode opamp

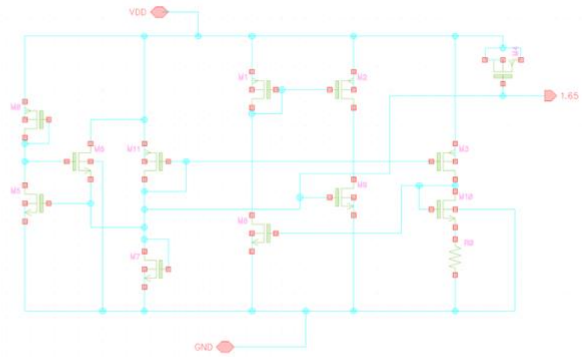

Figure 6: Schematic of Bias Circuit.

3. Results and Discussion

3.1 Telescopic Cascode Amplifier

3.1.1 Waveform

Fig. 7 shows the ac simulation result for the telescopic Op-Amp. With this setup, the gain is high but the UGB is extremely low. Gain, frequency at 3 dB, and UGB are displayed on the graph. The design is simulated using the hspiceD simulator. The gain plot is shown in red, and the magnitude plot is shown in blue.

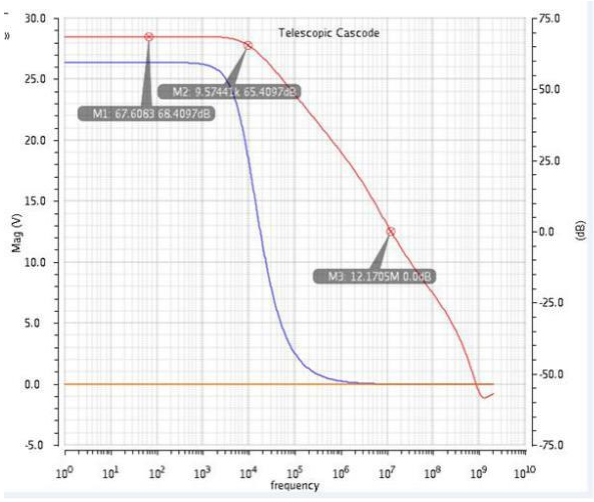

Figure 7: Telescopic Cascode Amplifier Simulation

3.1.2 Result

By connecting a 1 pF load capacitance to an Op-amp's output terminal, a gain plot can be produced. By applying supply variation and connecting an op-amp's output as feedback to the negative terminal, PSRR is computed. Applying a tiny signal to both of an Op-amp's inputs allows for the calculation of CMRR. A thorough summary of the calculation of an additional parameter is provided in a later section. The telescopic Op-Amp's detailed parameters are displayed in the table below.

Table 2: Specifications of Telescopic Opamp

Sr.no	Parameters	Value
1.	Gain	68.4dB
2.	3dBbandwidth	9.57KHz
3.	UGB	12.17MHZ
4.	Phase margin	
5.	Output Swing	1.72V

6.	Slew rate	58.7volt/Âț.sec
7.	CMRR	53.3db
8.	PSRR	45.7db
9.	Offset Voltage	2mV

3.2 Two Stage Opamp
3.2.1 Waveform
Fig. 8 shows the gain-boosted Op-Amp AC simulation. The design is simulated using the hspiceD simulator and cadence virtuoso 6.1.5. The design is tested using a 1 pF load at the output.
3.2.2 Result
Despite having a high gain of 45.47 dB, the two-stage Op-Amp is not able to support high speed ADC. Additionally, the use of two-stage operational amplifiers is restricted by the 3.4 mV offset. If the Op-Amp is not accurately compensated, its performance is affected. 64.26 dB of CMRR and 54.25 dB of PSRR are achieved with this setup. The two stage Op-Amps have better phase margin and UGB. Table 3 shows the other achieved specification of the two-stage Op-Amp.

3.2.3 Limitations of the Two-Stage Opamp
1. Insufficient gain
2. Poor power supply rejection ratio

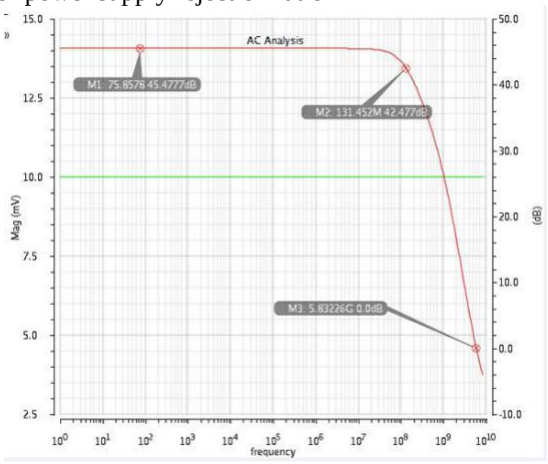

Figure 8: Two Stage Opamp Simulation

Table 3: Specifications of Two Stage Opamp

Sr.no	Parameters	Value
1.	Gain	34.17dB
2.	3dBbandwidth	138.5MHz
3.	UGB	3.17MHZ
4.	Phase margin	
5.	Output Swing	2.62V
6.	Slew rate	335.8/sec.
7.	CMRR	61.26db
8.	PSRR	54.25db
9.	Offset Voltage	3.4 mV

3.3 Folded Cascode Amplifier
3.3.1 Waveform
The cascade that is folded The ac simulation result for the opt-amp is shown in Fig. 9. Here, the resistor is replaced by the diode-connected load. Gain will increase if M1, M2, and M3 values are raised. Greater R1 and R2 values decrease phase margin but also increase gain. On the graph in the figure below, various pointer markers represent the gain, or UGB.

Figure 9: Folded Cascode Amplifier Simulation

3.3.2 Result
It should be mentioned that folded cascode with a 633.04 MHz UGB is used to achieve a gain of 57.87 db. The phase margin of folded cascode is 60◦ C. Every other parameter, including CMRR, PSRR, and slew rate, is computed with a 1 pF load in mind. The parameter computed with cadence 180 nm CMOS technology is displayed in the table.

Table 6: Specifications of Folded Cascode Opamp

Sr.no	Parameters	Achieved Value
1.	Gain	57.877dB
2.	UGB	633MHZ
4.	Phase margin	
6.	Slew rate	299.3volt/
7.	CMRR	76db
8.	PSRR	54.27db

3. CONCLUSIONS

Modern wireless communication devices require high data rates and low power consumption. An analog-to-digital converter is one of the essential components of the portable device that interfaces the analog and digital domains. Low-power techniques for high-speed applications are becoming increasingly important as the portable device market grows. The use of small feature-size processes can lower power consumption. On the other hand, process variances and other factors impact the device's overall performance when power consumption decreases. For portable devices, the main criteria are low power consumption, medium resolution, and high speed. The goal of this project is to design a 250 MSPS 8-bit ADC. This ADC ASIC is a mixed signal. This design uses a sub-ranging type of 2-step flash ADC architecture. The ADC is designed in two steps: a 4-bit flash-type ADC. ADC design consists of a sample and hold block, comparator block, op-amp, bias circuit, and TGB encoder. A general-purpose op-amp has been designed, and it can be used in 3 different modules: ADC, S/H amplifier, subtractor, and residual amplifier. After an in-depth analysis of different op-amp topologies concerning given specifications, the stage-folded cascade topology is selected. The ADC has been designed,

implemented, and analyzed using 180nm technology using Cadence Virtuoso 6.1.5 in the spiced simulator.

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