International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 10 Issue: 11 | Nov - 2026 SJIF Rating: 8.659 ISSN: 2582-3930

A 10-Bit 400 MS/S Hybrid Voltage-Time Pipelined ADC with a Ci-Sar Coarse Stage and Time-Domain Fine Quantization

IQJAZ JAMEELATH RAAHINA S A

Master of Engineering in VLSI DESIGN

Dr. Sivanthi Aditanar College of Engineering

Tiruchendur, India

ijraahina2003@gmail.com

Abstract **- This paper presents a hybrid voltage-time domain pipelined analog-to-digital converter (ADC) that replaces the coarse stage of a recently reported reference-embedded time-domain-residue ADC with a 6-bit charge-injection successive-approximation-register (CI-SAR) ADC. The CI-SAR stage uses a six-cell segmented charge-injection DAC (CI-DAC), gm-boosted StrongARM comparators, a six-transistor TSPC bit trigger, a temperature-aware bias generator and CAL-DAC offset calibration. A voltage-to-time converter (VTC) converts the residue pair into three time-domain signals, which a 5-bit time-to-digital converter (TDC) quantizes. A one-bit overlap between the stages gives a 10-bit output at a target rate of 400 MS/s, while consuming 1.57mW.**

Keywords - charge-injection SAR (CI-SAR), hybrid voltage-time pipelined ADC, time-to-digital converter (TDC), voltage-to-time converter (VTC).

I. INTRODUCTION

The increasing demand for high-speed, high-resolution, and energy-efficient electronic systems has made Analog-to-Digital Converters (ADCs) essential components in modern integrated circuit design. ADCs convert continuous analog signals into digital data and are widely employed in wireless communication, medical instrumentation, sensor networks, image processing, and high-speed data acquisition systems. Among various ADC architectures, Successive Approximation Register (SAR) ADCs are widely adopted due to their simple structure, low power consumption, and efficient hardware utilization. However, conventional SAR ADCs face limitations in achieving high resolution at increased sampling rates, creating the need for alternative architectures that balance conversion speed, accuracy, and power efficiency.

To address these limitations, this project initially implements a conventional hybrid pipelined SAR ADC that combines voltage-domain and time-domain conversion techniques. Subsequently, a modified hybrid voltage-time-domain pipelined CI-DAC SAR ADC is developed to improve the conversion architecture.

The proposed design incorporates a 6-bit Charge-Injection SAR (CI-SAR) stage for coarse conversion, followed by a Voltage-to-Time Converter (VTC) and a 5-bit Time-to-Digital Converter (TDC) for fine quantization. A one-bit overlap between the conversion stages is employed to achieve a nominal resolution of 10 bits. Additionally, a segmented Charge-Injection Digital-to-Analog Converter (CI-DAC) and modified circuit parameters, including capacitor size and boost factor, are incorporated into the design. The overall architecture aims to reduce the dependence on conventional residue amplification while providing an efficient approach to high-speed and low-power ADC implementation.

II. LITERATURE REVIEW

Su et al. [1] presented a SAR-assisted hybrid ADC combining voltage-domain conversion with time-domain sub-range quantization. Moon et al. [3] introduced a three-stage voltage-current-time ADC in 28-nm CMOS technology, demonstrating the effectiveness of hybrid conversion techniques for high-speed operation. Wu et al. [4] developed a 14-bit pipelined-SAR ADC operating at 300 MS/s using redundant SAR stages to improve conversion accuracy. Lee et al. [5] proposed a 7-bit Charge-Injection SAR ADC operating at 1.5 GS/s, incorporating a segmented CI-DAC, gm-boosted

StrongARM comparator, and PVT-tracking metastability detector. Lim et al. [6] presented a hybrid voltage-time-domain pipelined ADC in 40-nm CMOS technology, achieving 150 MS/s, 61.1 dB SNDR, and 75.5 dB SFDR with 2.54 mW power consumption. This architecture provides the foundation for the proposed work.

Padash et al. [7] presented a flexible differential resistive-ladder SAR ADC, while Feng et al. [8] demonstrated a two-stage SAR ADC using asynchronous pipelining and reference snubbers to improve dynamic performance. Other studies investigated floating-inverter amplifiers, PVT stabilization, and background calibration techniques to improve residue accuracy and circuit efficiency. Although these architectures demonstrate improvements in conversion speed, resolution, and power consumption, achieving all three simultaneously remains challenging. Therefore, the proposed work combines a 6-bit Charge-Injection SAR coarse stage with a Voltage-to-Time Converter (VTC) and a 5-bit Time-to-Digital Converter (TDC). A one-bit overlap between the stages is employed to obtain a nominal 10-bit resolution.

III. DESIGN DESCRIPTION

A. *Proposed Architecture*

Fig 1 illustrates the proposed architecture is a hybrid voltage-time-domain pipelined ADC designed to achieve a nominal resolution of 10 bits. It combines a 6-bit Charge-Injection SAR (CI-SAR) coarse conversion stage with a time-domain fine conversion stage consisting of a Voltage-to-Time Converter (VTC) and a 5-bit Time-to-Digital Converter (TDC). A one-bit overlap between the two stages is used to obtain the final 10-bit digital output.

Initially, the analog input signal is sampled using a bootstrapped sample-and-hold circuit. The sampled signal is then processed by the 6-bit CI-SAR stage, which performs coarse quantization using a segmented Charge-Injection Digital-to-Analog Converter (CI-DAC) and comparator-based successive approximation. The remaining voltage residue is transferred to the VTC, where it is converted into a corresponding time interval.

The time-domain signal is then processed by the 5-bit TDC to perform fine quantization. The architecture uses three Interpolating Time Converters (ITCs) for time-domain residue processing. Finally, the coarse and fine digital outputs are combined using digital correction logic to generate the 10-bit output code. This architecture aims to reduce dependence on conventional residue amplification while supporting high-speed and low-power conversion.

B. *Block Diagram*

The overall block diagram of the proposed hybrid voltage-time-domain pipelined CI-DAC SAR ADC is shown below

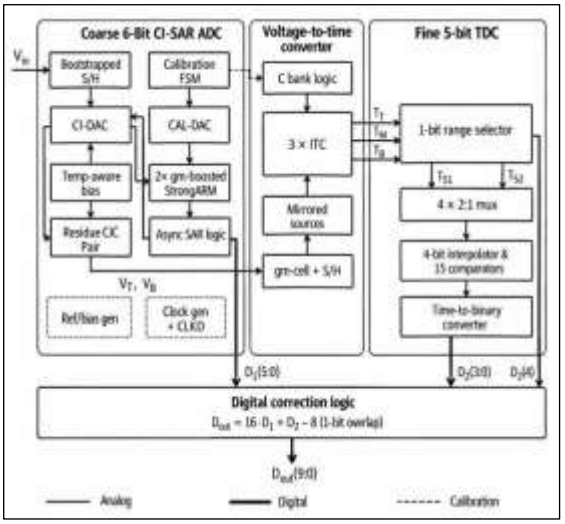


Fig 1: Block Diagram of Hybrid Voltage-time domain Pipelined CI-DAC SAR ADC

C. *Flow Chart*

The flowchart Fig.2 shows the operating cycle of the proposed Hybrid Voltage-time domain Pipelined CI-DAC SAR ADC.

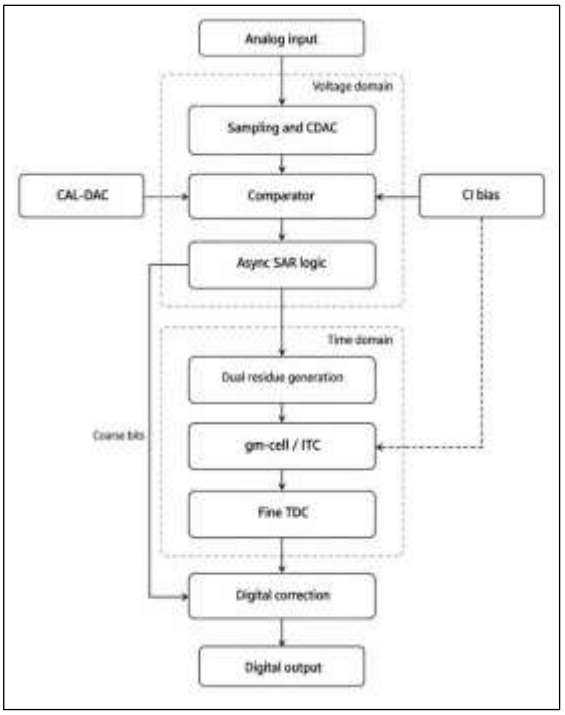


Fig 2: Flow-Chart of Hybrid Pipelined CI-DAC SAR ADC

IV. COARSE 6 – BIT CI-SAR ADC

The proposed 6-bit CI-SAR coarse stage performs the initial conversion of the sampled analog input into a 6-bit digital code and generates the residue for subsequent fine quantization is shown in Fig 3. It uses a segmented CI-DAC consisting of four MSB cells and two LSB cells to produce the required voltage levels through controlled charge injection. This reduces the need for a conventional binary-weighted capacitor array. Two gm-boosted StrongARM comparators operate in a ping-pong arrangement to support fast successive comparisons, while asynchronous SAR logic controls the conversion process.

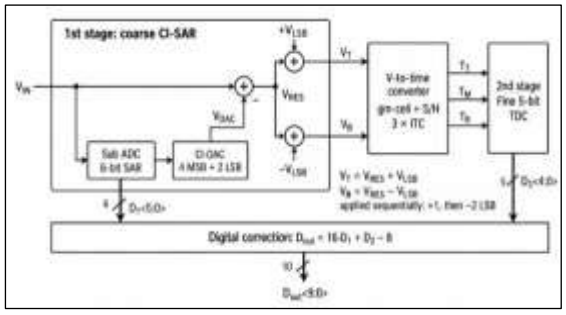


Fig 3: Coarse 6-bit CI-SAR ADC

A temperature-aware bias circuit using PTAT and CTAT components helps maintain stable charge-injection current under temperature variations. Additionally, a CAL-DAC-based offset calibration technique reduces comparator decision errors and improves coarse conversion accuracy. Overall, these techniques aim to improve conversion speed, reduce DAC complexity, and provide a reliable residue for the fine conversion stage.

V. VTC, TDC AND DIGITAL CORRECTION

The proposed Voltage-to-Time Converter (VTC) converts the two residue voltages, $V_T$and V_B, generated by the 6-bit CI-SAR stage into corresponding time-domain signals. A Gm-cell with a sample-and-hold circuit performs the voltage-to-time conversion, reducing the dependence on conventional high-gain residue amplifiers. The design incorporates three modifications: the capacitor value is reduced from 150 fF to 100 fF, the boost factor from 4× to 3×, and the resolution from 12 bits to 10 bits. The fine 5-bit TDC processes the timing signals $T_T, T_M, and\ T_B$ generated by the VTC. It uses a 1-bit range selector, a 4×2:1 multiplexer, a 4-bit time interpolator is shown in Fig 4 with 15time comparators, and a time-to-binary converter. The interpolator divides the selected timing range into 16 intervals to identify the fine timing position. Finally, the coarse and fine digital outputs are combined using one-bit overlap to obtain a nominal 10-bit ADC output.

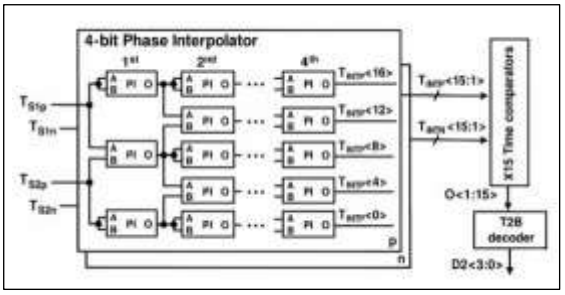


Fig 4: 4-bit Phase Interpolator

VI. METHODOLOGY AND IMPLEMENTATION

The proposed Hybrid Pipelined CI-DAC SAR ADC was implemented in Verilog HDL and synthesized in Xilinx Vivado 2025.1 for an Artix-7 device. It was evaluated using behavioural simulation at a sampling rate of 400 MS/s. The simulation results provide information about the RTL structure, power consumption, area utilization, and noise analysis. The implementation uses 1375 Slice LUTs, 227 Slice Registers, and 464 Slices. It also utilizes 14 DSPs, 31 Bonded IOBs, and one BUFGCTRL resource. The estimated total power consumption is 1.574 mW.

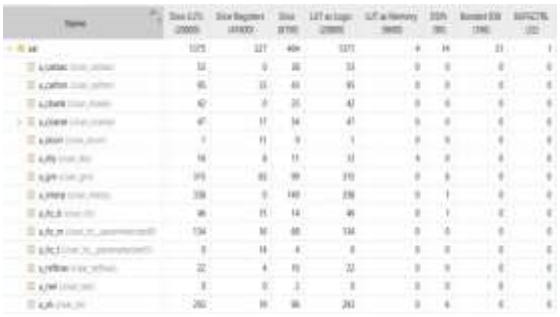


Fig 5: Utilization of Hybrid Pipelined CI-DAC SAR ADC

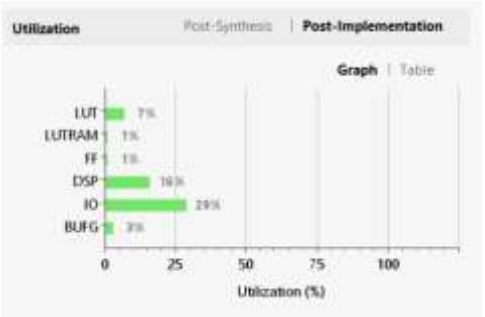


Fig 6: Post-Implementation Resource Utilization Summary

Block	Power (mW)	Share
Bootstrapped S/H	0.0400	2.5%
6-bit CI-SAR	0.2476	15.7%
gm-cell + S/H	0.5120	32.5%
3 × ITC	0.1794	11.4%
Fine TDC (5-bit)	0.3860	24.5%
Clock generation + CLKD	0.1100	7.0%
Reference/bias + T-bias	0.1000	6.3%
Total	**1.5749**	**100%**

Fig 7: Power Consumption of Hybrid Pipelined CI-DAC SAR ADC

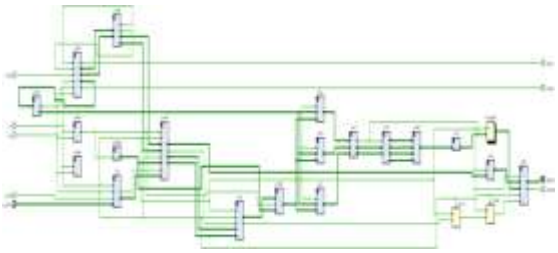


Fig 8: RTL schematic of the Hybrid Pipelined CI-DAC SAR ADC.

TABLE I. Post-Implementation Power Comparison

Parameter (W)	***Hybrid Pipelined SAR ADC***	***Hybrid Pipelined CI-DAC SAR ADC***
ADC Average Power	2.54 mW	1.57 mW
Device Dynamic power	0.313 W	0.075 W
Device static power	0.071 W	0.072 W

The proposed Hybrid Pipelined CI-DAC SAR ADC reduces the average power consumption from 2.54 mW to 1.57 mW, achieving a 38.19% reduction compared with the existing design. The device dynamic power decreases from 0.313 W to 0.075 W, representing a 76.04% reduction. However, the device static power increases slightly from 0.071 W to 0.072 W, corresponding to a 1.41% increase. Overall, the proposed design improves power efficiency by significantly reducing average and dynamic power consumption while maintaining nearly the same static power level.

TABLE II. Post-Implementation Resource Utilization

Resource (available)	***Hybrid Pipelined SAR ADC***	***Hybrid Pipelined CI-DAC SAR ADC***
Slice LUTs (20800)	4267	1375
Slice Registers (41600)	71	227
Slices (8150)	1223	464
DSP (90)	7	14

The resource utilization table shows that the proposed Hybrid Pipelined CI-DAC SAR ADC reduces Slice LUT usage from 4267 to 1375, achieving a 67.78% reduction. Slice usage decreases from 1223 to 464, representing a 62.06% reduction. However, Slice Registers increase from 71 to 227, corresponding to a 219.72% increase, while DSP utilization rises from 7 to 14, representing a 100% increase. Overall, the proposed design uses fewer LUTs and slices, indicating improved logic resource efficiency, although it requires more registers and DSP resources.

VII. CONCLUSION

This paper presents a 10-bit hybrid voltage-time-domain pipelined ADC operating at a target sampling rate of 400 MS/s. The proposed implementation aims to reduce hardware resource utilization and power consumption while maintaining the required ADC functionality. The behavioural simulation results demonstrate the successful implementation of the proposed design. Compared with the existing hybrid pipelined SAR ADC, the proposed design reduces Slice LUT utilization by 67.8% and slice utilization by 62.1%. The total cell count is also reduced by 53.5%, while the estimated average power consumption decreases by approximately 37.2%. The number of Bonded IOBs is reduced from 36 to 31, indicating lower I/O resource utilization. Although the usage of slice registers, DSPs, LUTRAM, and nets increases, the overall implementation shows improvements in several key hardware and power parameters. These results demonstrate the potential of the proposed design for area-efficient and low-power ADC implementation.

VIII. FUTURE SCOPE

Future work will focus on evaluating the ADC performance by extracting the dynamic parameters, including Signal-to-Noise and Distortion Ratio (SNDR), Spurious-Free Dynamic Range (SFDR), and Effective Number of Bits (ENOB), through sine-input FFT analysis. The static parameters, Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), will be determined using a code-density test. The Walden figure of merit (FoM) will also be calculated to evaluate the ADC's power efficiency.

REFERENCES

[1] Su. Z et. al, "A 280-MS/s 12-b SAR-Assisted Hybrid ADC With Time-Domain Sub-Range Quantizer in 45-nm CMOS," Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), 2019, DOI: 10.1109/CICC.2019.8780209

[2] Liu. J et al., "A calibration-free pipelined SAR ADC with feedback coefficient compensation-based pipelined residue amplification stage," in Proc. Int. Conf. Frontiers Technol. Circuits Syst. (FTCS), 2025, DOI: 10.1109/FTCS68006.2025.11405815

[3] Moon. K. J et al., "A 28-nm CMOS 12-bit 250-MS/s voltage-current-time domain 3-stage pipelined ADC," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 2843–2847, Dec. 2020, DOI: 10.1109/TCSII.2020.2990910

[4] Wu. G et al., "A 5-bit High-Linearity, Binary-Recombination-Redundancy Sub-SAR ADC in 300-MS/s, 14-bit Pipelined-SAR ADC," Proceedings of the IEEE 14th International Conference on ASIC (ASICON), 2021, DOI: 10.1109/ASICON52560.2021.9620444

[5] Lee. C, "A 1.5-GS/s 7-bit Charge-Injection SAR ADC Using a PVT-Tracking 1-bit Metastability Detector," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 73, no. 2, pp. 108–112, Feb. 2026, DOI: 10.1109/TCSII.2025.3637288

[6] Lim. J. G et al., "A Hybrid Voltage-Time Domain Pipelined ADC With Reference-Embedded Time-Domain Residues," IEEE Journal of Solid-State Circuits, vol. 61, no. 2, Feb. 2026, p. 566, DOI: 10.1109/JSSC.2025.3579913

[7] Padash. M et al., "A Natively Flexible 8-bit Differential Resistive Ladder SAR-ADC," Proceedings of the 2025 IEEE International Circuit and System Symposium (ICSyS), 2025, DOI: 10.1109/ICSyS65149.2025.11379912

[8] Feng. J et al., "A 200-MS/s, 77-dB-DR Two-Stage SAR ADC With Asynchronous Pipelining and Reference Snubbers," Proceedings of the 2025 IEEE European Solid-State Electronics Research Conference (ESSERC), 2025, DOI: 10.1109/ESSERC66193.2025.11214048

[9] Guo. Y et al., "A low power PVT stabilization technique for dynamic amplifier in pipelined SAR ADC," in Proc. IEEE MWSCAS, 2021, DOI: 10.1109/MWSCAS47672.2021.9531829

[10] Razavi. B, "The StrongARM latch [a circuit for all seasons]," IEEE Solid-State Circuits Mag., vol. 7, no. 2, pp. 12–17, Jun. 2015, DOI: 10.1109/MSSC.2015.2418155

[11] Tang. X et al., "A bandwidth-adaptive pipelined SAR ADC with three-stage cascoded floating inverter amplifier," IEEE J. Solid-State Circuits, vol. 58, no. 9, pp. 2564–2574, Sep. 2023, DOI: 10.1109/JSSC.2023.3268719

[12] Miao. R et al., "Background calibration for capacitor mismatch in SAR ADC based on split-delta architecture," in Proc. ISSET, 2026, DOI: 10.1109/ISSET70600.2026.11682677

[13] Lee. C et al., "A 17.4 fJ/conv.-step, 202 µm², 1.5 GS/s and PVT-tolerant 7-bit charge-injection SAR ADC in 28 nm CMOS using a background-calibrated 1-bit metastability detector and a gm-boosted StrongARM comparator," in Proc. IEEE CICC, Boston, MA, USA, Apr. 2025, pp. 1–3, DOI: 10.1109/CICC63670.2025.10983098

[14] You H. et al. (2024), 'SAR-MemPipe: A Hybrid Pipeline-SAR Memristive ADC for Analog Resistive Arrays', IEEE International Symposium on Circuits and Systems (ISCAS), 2024, DOI: 10.1109/ISCAS58744.2024.10557966

[15] Kim H. et al. (2023), 'A 9-Bit 500-MS/s 4-Stage Pipelined SAR ADC With Wide Input Common-Mode Range Using Replica-Biased Dynamic Residue Amplifiers', IEEE Access, Vol. 11, 2023, DOI: 10.1109/ACCESS.2023.3248784