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A 45nm AND 65nm CMOS IMPLEMENTATION OF 12T SRAM CELL WITH SOFT ERROR READ STABILITY OF MULTINODE UPSET RECOVERABILITY FOR AEROSPACE APPLICATION

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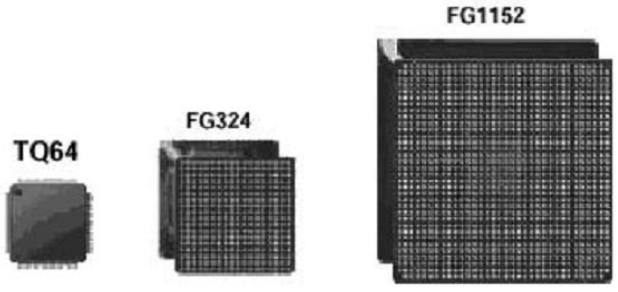
Abstract – *With technology advancing rapidly, the size of transistors and the distance between them is decreasing quickly. This reduction in size is causing the critical charge of sensitive nodes in SRAM cells to decrease, making them more susceptible to soft errors, especially in aerospace applications. When a radiation particle strikes a open node in a standard 6T SRAM cell, the storage data in the cell can be changed, leading to a single-event upset (SEU). To address this issue, a new Soft Error Read and write Stability improves Low Power 12T (SARP12T) SRAM cell has been introduced in this study to reduce the impact of SEUs. The performance of SARP12T has been compared to other recently developed soft-error-aware SRAM cells like QUCCE12T, QUATRO12T, RHD12T, RHPD12T, and RSP14T. SARP12T is designed for the recoverability of all stored data in sensitive nodes even if they are affected by radiation strikes. Additionally, SARP12T can overcome single-event multi-node upsets (SEMNUs) that may happened at its sensitive node pair. This proposed cell also boasts the higher read stability, as the storage node holding '0' can regain from any upset during read operations. Moreover, SARP12T consumes the minimum amount of hold power, has greater write ability, and lower write delay compared to other similar cells. Despite a almost greater read delay and higher read and write energy consumption, the improvements in the proposed SARP12T cell make it a promising solution for mitigating soft errors in SRAM cells.*

1. INTRODUCTION:

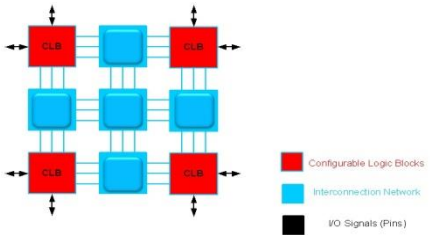
The aviation industry has improved the quality of human life by providing many useful services (satellite communications, military surveillance, navigation systems, etc.). and increase security. Microprocessors play an important role in aerospace technology by performing tasks such as control and guidance, engine control and inertial navigation. Processors are now equipped with multiple cores to enhance their capabilities. More cores in the processor improves performance. The amount of cache memory required is important for good performance of the processor. SRAM cells used as cache memory are important in increasing energy efficiency, space utilization and reducing processor latency. In the vastness of space there are high voltage devices that can affect the operation of memory circuits. When these objects collide with the surface of the combination, such as the symbol of the electronic device, they form electrical devices and holes. The electron and substrate/n-well produced by the inversion of the diffusion zone appear to be the forward source for the minority carriers produced by the collision. As a result, these minority carriers move towards the drain region and create positive or negative voltage when they accumulate. If this spike exceeds the threshold switch in the logic circuit and persists long enough, it can cause the stored data to change unexpectedly, causing what is known as a transient, pressure (SEU), or software error. In addition, as the distance between the technology and the components of the integration continues to increase, a single crash can affect many nodes, resulting in a widespread disturbance state (SEMNU).



Triple Module Redundancy (TMR) approach is adopted to reduce the impact of Single Event Error (SEU) on memory performance. This strategy involves using three copies of the data store and using majority voting to identify and create the correct data. If there is a slight deviation in one of the replicas, the other two replicas will go through a voting process to ensure the correct products are retained. However, the drawback of TMR is its large area and power requirement, making it impractical for many design applications.

Another way to reduce the impact of a single stress event (SEU) is to use error correction codes (ECC). However, ECC also has disadvantages such as increased power consumption, larger area usage, delays due to repetition in processing, connection and decision circuits and the need for additional hardware. Therefore, software error-sensitive SRAMs are preferred over ECCs as they use more power, area, and latency. Additionally, SRAM cells should be better able to recover from multiple interrupts as well as their ability to recover from SEUs.

The excellent response of cross-coupled inverters in 6T SRAM cells allows automatic changes in the value of the contents of the storage space when a stressful event (SEU) occurs. This unique behaviour means that 6T cells do not have the necessary characteristics of a small bug known as SRAM. Many other fault-sensitive SRAM cell designs have been proposed in various publications. As described in [13], the QUATRO10T design is able to change "1" to "0" with a single stress event (SEU). However, it is not possible to recover SEUs associated with "0" remaining storage space. Also, QUATRO10T is more likely to have write errors. To solve this problem, the authors introduced a modification called QUATRO12T in [14]. Despite the improvements, QUATRO12T still provides partial protection against SEU.



1.1 OBJECTIVE:

To design this 12T Soft error aware read stability enhanced SRAM cells at 45nm and 65nm CMOS technology and proved the comparisons of area, power, and delay.

To extend this 12T SRAM cell up to 8-bit.

2. LITERATURE SURVEY:

[1] P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” - Physical mechanisms responsible for nondestructive single-event effects in digital microelectronics are reviewed, concentrating on silicon MOS devices and integrated circuits. A brief historical overview of single-event effects in space and terrestrial systems is given, and upset mechanisms in Dynamic Random Access Memories, static random access memories, and combinational logic are detailed. Techniques for mitigating single-event upset are described, as well as methods for predicting device and circuit single-event response using computer simulations. The impact of technology trends on single-event susceptibility and future areas of concern are explored.

[2] J. D. Black, P. E. Dodd, and K. M. Warren, “Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction,” - Physical mechanisms of single-event effects that result in multiple-node charge collection or charge sharing are reviewed and summarized. A historical overview of observed circuit responses is given that concentrates mainly on memory circuits. Memory devices with single-node upset mechanisms are shown to exhibit multiple cell upsets, and spatially redundant logic latches are shown to upset when charge is collected on multiple circuit nodes in the latch. Impacts on characterizing these effects in models and ground-based testing are presented. The impact of multiple-node charge collection on soft error rate prediction is also presented and shows that full circuit prediction is not yet well understood. Finally, gaps in research and potential future impacts are identified.

[3] M. Fazeli, S. N. Ahmadian, S. G. Miremadi, H. Asadi, and M. B. Tahoori, “Soft error rate estimation of digital circuits in the presence of multiple event transients (METs),” - In this paper, we present a very fast and accurate technique to estimate the soft error rate of digital circuits in the presence of Multiple Event Transients (METs). In the proposed technique, called Multiple Event Probability Propagation (MEPP), a four-value logic and probability set are used to accurately propagate the effects of multiple erroneous values (transients) due to METs to the outputs and obtain soft error rate. MEPP considers a unified treatment of all three masking mechanisms i.e., logical, electrical, and timing, while propagating the transient glitches. Experimental results through comparisons with statistical fault injection confirm accuracy (only 2.5% difference) and speed-up (10,000X faster) of MEPP.

[4] S. Lin, Y.-B. Kim, and F. Lombardi, “Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset,”- The occurrence of a single event with a multiple-node upset is likely to increase significantly in nanoscale CMOS due to reduced device size and power supply voltage scaling. This paper presents a comprehensive treatment (model, analysis, and design) for hardening

storage elements (memories and latches) against a soft error resulting in a multiple-node upset at 32-nm feature size in CMOS. A novel 13T memory cell configuration is proposed, analyzed, and simulated to show a better tolerance to the likely multiple-node upset. The proposed hardened memory cell utilizes a Schmitt trigger (ST) design. As evidenced in past technical literature and used in this work, simulation of all node pairs by current sources results in an assessment similar to 3-D device tools; the simulation results show that the proposed 13T improves substantially over DICE in the likely and realistic scenarios of very diffused or limited charge sharing/collection. Moreover, the 13T cell achieves a 33% reduction in write delay and only a 5% (9%) increase in power consumption (layout area) compared to the DICE cell (consisting of 12 transistors). The analysis is also extended to hardened latches; it is shown that the latch with the highest critical charge has also the best tolerance to a multiple-node upset. Among the hardened latches, the ST designs have the best tolerance, and in particular, the transmission gate configuration is shown to be the most effective. Simulation results are provided using the predictive technology file for 32-nm feature size in CMOS. Monte Carlo simulation confirms the excellent multiple-node upset tolerance of the proposed hardened storage elements in the presence of process, voltage, and temperature variations in their designs.

[5] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," - Trends in terrestrial neutron-induced soft-error in SRAMs from a 250 nm to a 22 nm process are reviewed and predicted using the Monte-Carlo simulator CORIMS, which is validated to have less than 20% variations from experimental soft-error data on 180-130 nm SRAMs in a wide variety of neutron fields like field tests at low and high altitudes and accelerator tests in LANSCE, TSL, and CYRIC. The following results are obtained: 1) Soft-error rates per device in SRAMs will increase x6-7 from 130 nm to 22 nm process; 2) As SRAM is scaled down to a smaller size, soft-error rate is dominated more significantly by low-energy neutrons (<; 10 MeV); and 3) The area affected by one nuclear reaction spreads over 1 M bits and bit multiplicity of multi-cell upset become as high as 100 bits and more.

[6] R. C. Baumann, "Soft errors in advanced semiconductor devices-part I: The three radiation sources," - In this review paper, we summarize the key distinguishing characteristics and sources of the three primary radiation mechanisms responsible for inducing soft errors in semiconductor devices and discuss methods useful for reducing the impact of the effects in final packaged parts.

[7] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," - We propose a quad-node ten transistor (10 T) soft error robust SRAM cell that offers differential read operation for robust sensing. The cell exhibits larger noise margin in sub-0.45 V regime and 26% less leakage current than the traditional soft error tolerant 12 T DICE SRAM cell. When compared to a conventional 6 T SRAM cell, the proposed cell offers similar noise margin as the 6 T cell at half the supply voltage, thus significantly saving the leakage power. In addition, the cell exhibits 98% lower soft error rate than the 6 T cell in accelerated neutron radiation tests carried out at TRIUMF on a 32-kb SRAM implemented in 90-nm CMOS technology.

[8] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," - A novel design technique is proposed for storage elements which are insensitive to radiation-induced single-event upsets. This technique is suitable for implementation in high density ASICs and static RAMs using submicron CMOS technology.

[9] R. Rajaei, B. Asgari, M. Tabandeh, and M. Fazeli, "Design of robust SRAM cells against single-event multiple effects for nanometer technologies," - As technology size scales down toward lower two-digit nanometer dimensions, sensitivity of CMOS circuits to radiation effects increases. Static random access memory cells (SRAMs) that are mostly employed as high-performance and high-density memory cells are prone to radiation-induced single-event upsets. Therefore, designing reliable SRAM cells has always been a serious challenge. In this paper, we propose two novel SRAM cells, namely, RHD11 and RHD13, that provide more attractive features than their latest proposed counterparts. Simulation results show that our proposed SRAM cells as compared with some state-of-the-art designs have considerably higher robustness against single-event multiple effects. Moreover, they offer a sensible area overhead advantage so that our proposed RHD11 SRAM cell has 19.9% smaller area than the prominent dual-interlocked cell. The simulation results and analyses show that our proposed SRAM cells, particularly the proposed RHD13, have to consider lower failure probability among the considered recent radiation-hardened SRAM cells.

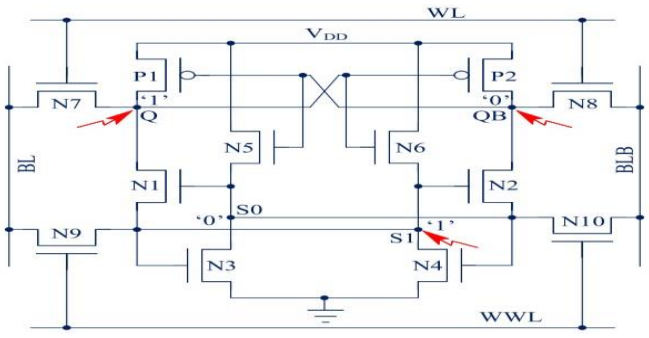
3. THE EXISTING 12T SRAM CELL:

In today's world, there is a trend to reduce the size of silicon wafers for speed and performance. This involves reducing the size of the device by focusing on parameters such as electronic components and the size of the transistor, which are mainly controlled by design engineers.
In general, the power supply is reduced to reduce static electricity consumption, but it is also necessary to reduce the starting voltage to achieve high performance. However, lowering the nominal voltage causes smaller power lines to expand further, resulting in higher power consumption. This voltage loss is mainly caused by subthreshold current and gate leakage current.

In microprocessors, cache memory takes up more than half of the chip area, so cache power is an important part of power consumption. To ensure the stability of SRAM cells, there is no noise such as noise-free static voltage, current, voltage change, instant change of registers. This test is important in memory formation. The total leakage current in an SRAM cell depends on the contribution of the leakage current of each transistor. The principle of leakage current is that the current is related to the initial leakage current and the gate leakage current. With current technology, inter band tunnel leakage is now negligible.

As the gate oxide thickness decreases, the gate leakage current increases exponentially and becomes comparable to the subthreshold leakage current at thin oxide thickness. SRAM plays an important role in digital systems where factors such as speed, power consumption and performance are very important.

Reducing the power consumption of digital circuits helps reduce power consumption but also affects static noise and transistor mismatch. Since the device size is small, different methods may affect the noise level.



Changes in negative voltage resulting from changes in the process will affect the stability and reliability of SRAM cells. It is difficult to design the perfect phone for SRAM because the supply voltage, threshold voltage and transistor size ratio play an important role.

Transistor mismatch can lead to significant differences in the electrical parameters of adjacent transistors, making designs difficult to predict and control. The stability of SRAM cells is affected by increased switching and decreased power consumption.

3.1 DRAWBACKS:

- Writing and reading operations require more effort
- Latency and effort are greatly improved.
- Low reading stability
- Low writing ability

4. PROPOSED 12T SRAM CELL:

Software Error Low Power 12T SRAM with Multi-Node Translation Improved Read Stability As a direct result of technological advancement, single transistors and the gap between them are rapidly decreasing. When an electronic particle hits the sensor of a conventional 6T SRAM cell, the information stored in the cell is inverted, causing a distortion event (SEU). The authors of this study recommend the use of small, error-sensitive read stability-enhanced low-power 12T (SARP12T) SRAM cells as a way to reduce the risk of SEU occurrence. A comparison was made between the SARP12T and other recently announced error-sensitive SRAM cells. This allows assessment of the relative activity of SARP12T.

In addition to these advantages, the proposed 12T SRAM cell has the highest level of read stability and lower write capacity compared to most existing SRAM cells; but the SARP12T combines this with better write capability and shorter write latency. All these improvements in mobile phone can be achieved by using slightly longer reading and more reading and writing power to build 12T soft error detection security improvement SRAM 65nm and 45nm CMOS technology, which expands 12T soft error detection security - upgrade SRAM 65nm and 45nm Control patch area, latency and power comparison using up to 8-bit and Tanner EDA tools designed using CMOS technology. Advances in memory technology have led to the widespread use of large dynamic random access memories (DRAM) and static random access memories (SRAM) in modern systems on chips (SoCs). The balance of large and small memory leads to all sizes,

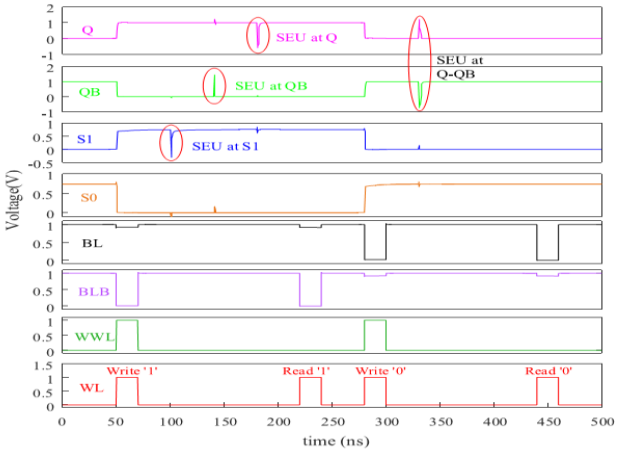
making SoCs more board-like than ever before. Large onboard memory gives SoCs many benefits, including improved bandwidth and performance that can only be achieved with onboard technology.

Whether onboard DRAM and/or large blocks of SRAM are available in the SoC depends on the density of manufacturability. The use of embedded DRAM, which uses a small cell based on a minimal transistor and a ditch capacitor, provides significant advantages over traditional CMOS-based SoCs. However, to enable area- and power-efficient operation of DRAM cells, there is a need to develop techniques for high-V low-leakage transistors and trench capacitors, which increases the cost and limits allowing use in certain SoCs running on specific SoCs. low to medium speeds.

4.1 SEU RECOVERY ANALYSIS:

The table below gives a brief summary of what the proposed building will do when its sensitive area is affected by a disturbance (SUE). The sensitive area refers to the area around the reverse bias current diffusion region of the OFF transistor. If an electrical particle hits the flow of the PMOS, it will create a transient pulse from “0” to “1” or “1” to “1” depending on the raw data stored in the node. Conversely, if a high-energy particle strikes a NMOS, a transient pulse of “0” to “0” or “1” to “0” is created. It should be noted that the internal node "0" (S0) of the SARP12T tank is surrounded by the flow port of the NMOS transistor, which only results in a screw size of "0", which does not affect the electrical equipment. . The state of the logical node. Therefore, in the "1" storage scenario of SARP12T (Q = "1", QB = "0", S1 = "1" and S0 = "0"), node S0 is insensitive while other nodes (Q, QB and S1) are sensitive.

When SEU affects the internal part of S1 which stores the value "1", the node will be changed to "0". This causes transistor 5 (included in QB) to remain open as there is no interference at Q. When both the pull-up and pull-down paths of the QB are open, the QB node enters high impedance. Normally the high impedance state does not change the logic state of the node, so QB retains its original logic value and N5 remains closed. As a result, S0 also goes into a high impedance state (since N5 and N3 are closed) and maintains its original value. Since Q, QB, and S0 maintain their states, S1 eventually returns to its original state.



When SEU affects storage Q in the first place, it will cause the origin of the node to change to "0". This causes transistors P2 and N6 to be temporarily enabled and disabled, respectively. When N6 closes and N4 remains closed due to waiting, S1 node enters a high impedance state and maintains its logic value. This causes N2 and N3 to open. Although P2 is on, the larger size of NMOS transistors N2 and N3 compared to PMOS transistor P2 ensures that the QB remains at its original logic level. This leaves P1 active and N5 deactivated. Additionally, when N3 is turned on, S0 remains at "0" and N1 remains unused. This process allows Q to regain its original properties without loss.

When a strong event (SEU) affects the QB storage, which stores the value "0", the logic value changes to "1". This causes P1 to temporarily close and N5 to temporarily open. Even though N5 is ON, node S0 maintains its logic state because N3 is larger than N5 (2.5×) and remains ON in hold mode. Therefore N1 and N4 are still closed. When the pull-up (P1) and pull-down (N1) transistors Q are turned off, node Q enters the high impedance state and maintains its original logic state. Since N4 is still closed and N6 (driven by Q) is still open, S1 maintains its initial value and keeps N2 and N3 open. As a result, the QB node is released to GND.

When the QB node changes from "0" to "1", the SEMNU event occurs, which affects both the storage Q and the QB, where Q changes from the logic level -1- to -0-. This results in P2 up and N6 down at QB and P1 down and N5 up at QB. Even though N5 is activated, the logic level of node S0 remains unchanged. Therefore transistors N1 and N4 are disabled. When both N6 and N4 are off, node S1 enters the high impedance state and maintains the first logic level. This causes N2 and N3 to remain active, causing QB to go to GND. Node Q returns 1 when N1 is off and P1 starts from QB. Therefore, both Q and QB return to their original values.

5. STIMULATION RESULTS:

Tanner EDA [Electronic Device Automation] is a tool which is used to stimulate and analysis the 45 and 65nm SRAM cells of their area, power and delay.

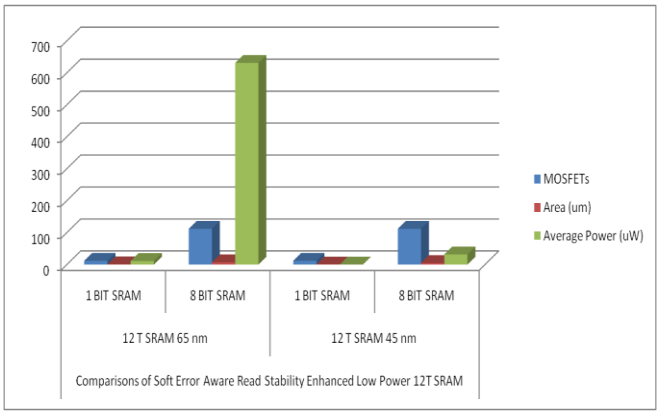
5.1 Software requirements:

1. S-EDIT (schematic edit)
2. T-EDIT (simulation edit)
3. W-EDIT (waveform edit)
4. L-EDIT (layout edit)

Using this tool engine SPICE programs provide a place where new ideas can be used for design and simulation in analog ICs.
The simulation results are plotted in the comparison table.
The column chart indicates the how the 65 and 45nm SRAM cell consume their area, power, and delay.

Comparisons of Soft Error Aware Read Stability Enhanced Low Power 12T SRAM CELL:

	Comparisons of Soft Error Aware Read Stability Enhanced Low Power 12T SRAM			
	12 T SRAM 65 nm		**12 T SRAM 45 nm**	
	1 BIT SRAM	8 BIT SRAM	1 BIT SRAM	8 BIT SRAM
MOSFETs	12	112	12	112
Area (um)	0.780	7.280	0.540	5.040
Average Power (uW)	11.550	631.03	0.3381	31.8857



6. ADVANTAGES:

- Low power consumptions in writing and reading operations.
- Very less improvement in Delay and energy consumptions.
- High read stability.
- High write ability.

7. CONCLUSION:

This research demonstrates a new low-power SRAM cell designed to prevent software errors and ensure read stability; This makes it ideal for aerospace applications. The SARP12T unit can recover original information on sensitive nodes even if this information has been altered due to electric shock. It can also survive multiple stress caused by single ion attacks between storage pairs. Additionally, the SARP12T unit has the highest RSNM, consumes the least power, and exhibits excellent write performance compared to other similar units. It also showcases EQM at its best, demonstrating its superiority over rival cells in the industry. Overall, the SARP12T unit is the best choice for use in aerospace applications due to its superior performance and low resistance to electrical faults.

8. REERENCES:

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