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A 7-Level Symmetric Multilevel Inverter with Minimum Numbers of Switches

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Abstract: This paper presents the design and implementation of a 7-level symmetric multilevel inverter (MLI) that utilizes a minimal number of switches. Traditional multilevel inverters often require a large number of power electronic components, which can increase system complexity, cost, and power losses. The proposed topology addresses these challenges by significantly reducing the number of required switches while maintaining the desired output voltage levels and waveform quality.

The design methodology focuses on achieving a symmetric configuration to ensure equal voltage stress across all switching devices. The operational principles of the inverter are analyzed, and the switching sequence is optimized to generate a seven-level output with reduced total harmonic distortion (THD). The performance of the inverter is evaluated through simulation and experimental validation.

Results demonstrate that the proposed 7-level symmetric MLI not only meets the output voltage requirements but also enhances overall efficiency and reliability. This topology is particularly suitable for renewable energy systems, electric vehicles, and other applications where compact, efficient, and cost-effective power conversion is essential.

Key Words: Multilevel inverter (MLI), Symmetric topology, Minimum number of switches, Total harmonic distortion (THD), Cost-effective power conversion.

Introduction

Most of the researches are carried out in cascaded MLI configuration. But still the new trends are involved in the evolution of renewed multilevel inverters. Modifications are made in its inbuilt structure. A 7-level MLI was generated with 9 switches reducing 3 switches from the main conventional CMLI. It offers good results yielding desired a 7-level output with low THD. A 7 level MLI with 7 switches reducing 2 more switches from the previous topology made a far improvement in the investigation of the switch reduction. Yet another topology of 7-level MLI was configured with 4 dc sources and just 6 switches to get 7-level output. The latter made a drastic move in topology development since the THD is low, and gate circuits used to drive the switches are less.

It is mentioned everywhere that simplicity is the main advantage of CMLI to generate 5 levels using 8 switches, 7 levels with 12 switches, 9 levels with 16 switches, and so on. It clearly reveals that an increase in levels demands more number of switches. Then the comment on simplicity of CMLI is simply contradictory. Hence, the focus was eyeing on a real solution to this problem, that is, how to simplify the complex circuit. Then arise the concept of “switch reduction”.

Exploring the existing topologies on basic 7 level, switch reduction was made from 12 switches to 9, gradually to 7 and then to 6.

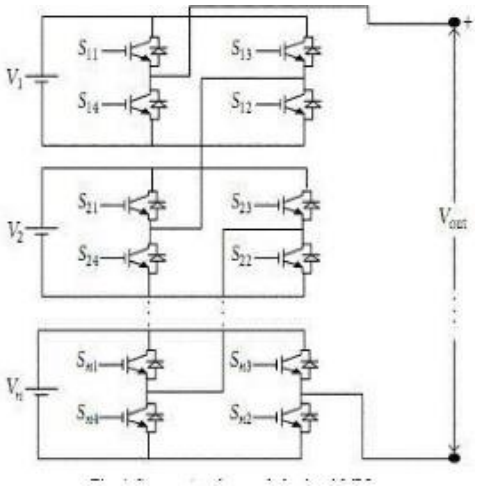


Fig. 1: Cascaded connection of n-level MLI

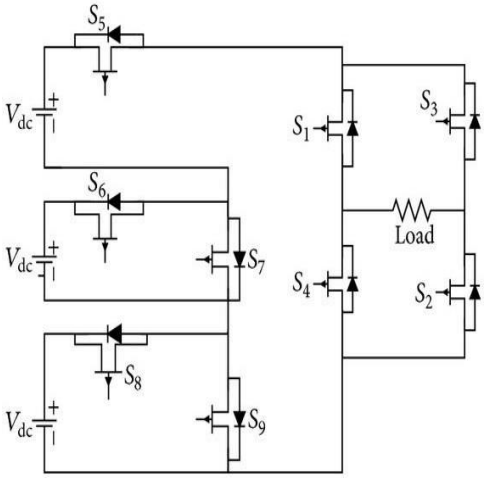


Fig. 2: 7 level 9 switch topology

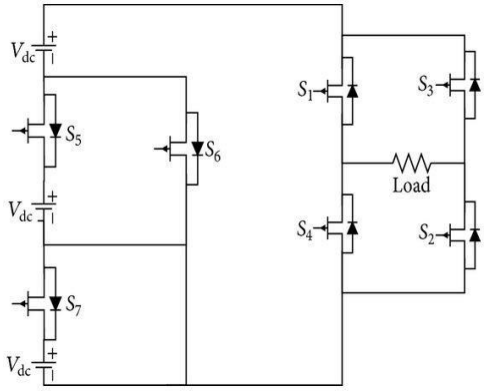


Fig. 3: 7 level 7 switch topology

Aiming at reducing the switches to the maximum possible extent and reducing complexity, the new topology is introduced with 5 switches for 7 levels, and this would be the least possible reduction. The new MLI configuration is made of 5 switches eliminating 1 switch from the existing 6 switches, 7-level topology in a special arrangement with 4 inputs DC sources to generate 7 level output. The less switches we use lessen the cost of circuit building. The circuit credibility is checked without using PWM. Then identifying the effectiveness in working simulated the circuit with the subject POD, and APOD using MATLAB/SIMULINK.

(1) Conventional Topology- Using 3 DC voltage sources, 3 H-bridge units each with 4 switches together forming 12 switches in total are used in conventional CMLI which is represented in Figure 1. General expression for output voltage
levels, m= (n+ 2)/2 where m is the number of switches in the configuration. Each Bridge is outputting 3 Levels, +Vdc, 0, −Vdc. Cascading 3 Bridges in such a fashion to produce stepped 7 level staircase waveforms.

(2) Existing Topology

(a) 7-Level, 9 Switches. This topology which is shown in Figure 2 is built with 3 dc sources, 1 H-Bridge composed of 4 switches and then additional 5 more switches for producing stepped 7 levels, for positive and negative half cycles. Table 1 represent the switching scheme for this topology.

(b) 7-Level, 7 Switches. This topology is made of 7 switches and 3 dc sources and is shown in Figure 3. One H-bridge present in the topology is mainly for polarity change. Here, three switches conduct at a time for level generation. The switching scheme is given in Table 2.

(c) 7-Level, 6 Switches. This is a special configuration in which consisting of four dc sources and six switches. One switch across the load is used for zero level. S1, S2, S3 used for level generation and S4, S5 switches for polarity changing Figure 4 represent the 7-level 6-switch topology and the corresponding switching pattern.

Table 1: Switching scheme for 7-level 9- switch topology

S no.	S1	S2	S3	S4	S5	S6	S7	S8	S9	Output Voltage
1	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	+Vdc
2	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	+2Vdc
3	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	-Vdc
6	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	-3Vdc

Table 2: Switching scheme for 7-level 7- switch topology

S no.	S4	S5	S6	S7	S1	S2	S3	Output Voltage
1	ON	ON	ON	OFF	ON	OFF	ON	+Vdc
2	ON	ON	OFF	OFF	ON	ON	OFF	+2Vdc
3	ON	ON	OFF	OFF	ON	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	OFF	ON	OFF	-Vdc
6	OFF	OFF	ON	ON	OFF	OFF	ON	-2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	ON	-3Vdc

Table 3: Switching scheme for 7-level 6- switch topology

S No.	S1	S2	S3	S4	S5	S6	Output Voltage
1	OFF	OFF	ON	OFF	ON	OFF	+Vdc
2	OFF	ON	OFF	OFF	ON	OFF	+2Vdc
3	ON	OFF	OFF	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	ON	0
5	ON	OFF	OFF	ON	OFF	OFF	-Vdc
6	OFF	ON	OFF	ON	OFF	OFF	-2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	-3Vdc

Proposed Five-Switch Topology.

The proposed 7 level MLI as shown in Fig. 5 is about redesigning of existing 6-switch topology eliminating 1 switch attaining the tag of 5 switch configuration. The circuit thus obtained is the simplest design compared to conventional and all other existing topologies. It consists of four dc sources of 7 levels, for 9-level, 5 dc sources and so on.

Generalized expression for output voltage levels for the new topology proposed is m = (2∗n−3), where m = number

of output voltage levels, n = number of switches m= (2 ∗ V −1), where V = number of dc

sources.

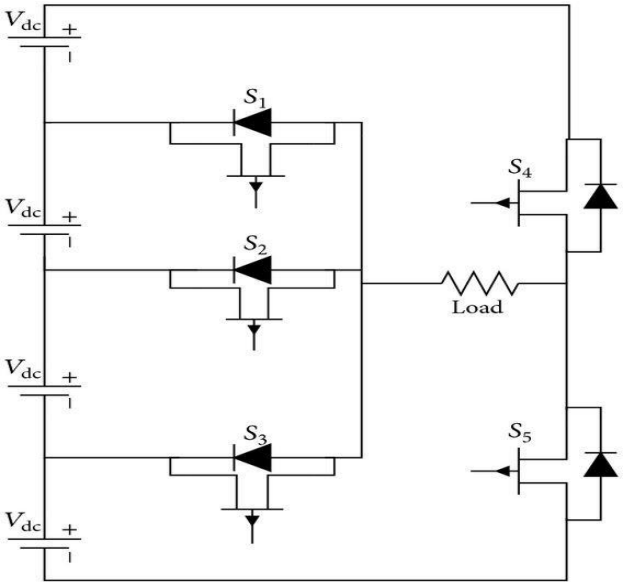


Fig. 4: 7 level 5 switch topology

The design of pulse generation circuit makes the topology differ from others so as to obtain the unique pulse pattern to trigger the switches at the proper instant. Switches S1, S2 and S3 need to be compulsorily unidirectional or else the output waveform will get distorted. Reduced switches make the circuit compact and user-friendly.

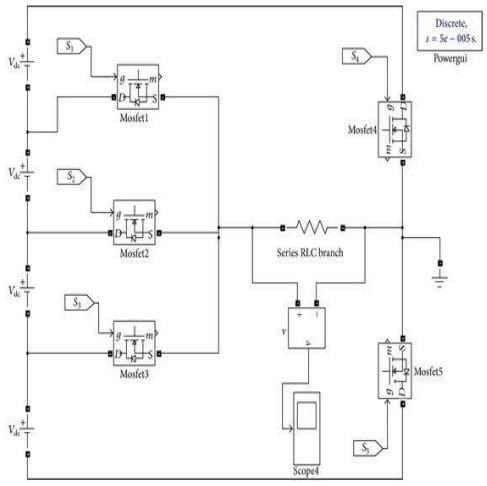
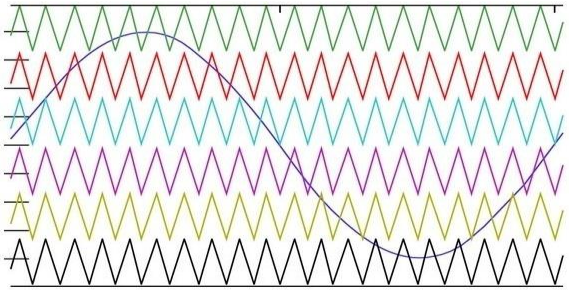
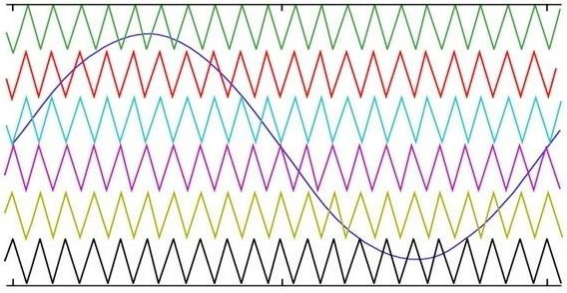


Fig. 5: Simulation diagram of proposed topology

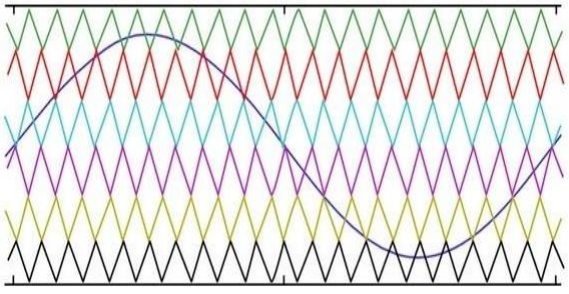
Though the usage of 4 dc sources for the generation of 7-level MLI results in less utilization of sources, switch reduction benefits in low switching losses. No H-Bridge is used. Just 2 switches play the role of polarity reversal. Table 4 represent the switching scheme for the proposed topology.



PD PWM



POD PWM



APOD PWM

Fig. 6: Carrier alignment of carrier based PWM technology

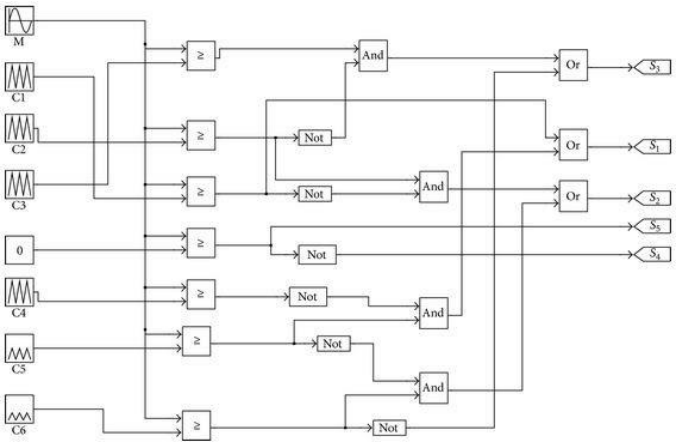


Fig. 7: PWM generation circuit

Switching scheme for **Proposed Five-Switch Topology**

s no.	S1	S2	S3	S4	S5	S6	Output Voltage
1	OFF	OFF	ON	OFF	ON	OFF	+Vdc
2	OFF	ON	OFF	OFF	ON	OFF	+2Vdc
3	ON	OFF	OFF	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	ON	0
5	ON	OFF	OFF	ON	OFF	OFF	-Vdc
6	OFF	ON	OFF	ON	OFF	OFF	-2Vdc

1. Cascaded H-Bridge (CHB) configuration has recently become very popular in high power AC supplies and adjustable-speed drive applications. A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units ineach of its three phases. Each H-bridge unit has its own dc source, which for an induction motor would be a battery unit, fuel cell or solar cell. Each SDC (separate D.C. source) is associated with a single phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Through different

combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, +Vdc, -Vdc and zero. The AC outputs of different full bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters (i.e. diode clamped and flying capacitor). In this topology, the number of output-phase voltage levels is defined by m= 2N+1, where N is the number of DC sources. A seven-level cascaded converter, for example, consists of three DC sources and three full bridge converters. Minimum harmonic distortion can be obtained by controlling the conducting angles at different converter levels. Each H- bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs‟ switching timings. Each switching device always conductsfor 180° (or half cycle) regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching devices current stress equal. In the motoring mode, power flows from the batteries through the cascade inverters to the motor. In the charging mode, the cascade converters act as rectifiers, and power flows from the charger (ac source) to the batteries.

The cascade converters can also act as rectifiers to help recover the kinetic energy of the vehicle if regenerative braking is used. The cascade inverter can also be used in parallel HEV configurations. This new inverter can avoid extra clamping diodes or voltage balancing capacitors.

The combination of the 180° conducting method and the pattern-swapping scheme make the cascade inverter voltage and current stresses the same and battery voltage balanced. The main advantages of using the cascade inverter in an induction motor include:

(1) It makes induction motor more accessible/safer and open wiringpossible for most of an induction motor power system.

(2) Traditional 230 V or 460 V motors can be used; thus higher efficiencyis expected as compared to low voltage motors.

(3) No EMI problem or common-mode voltage/current problem exists.

(4) Low voltage switching devices can be used.

(5) No charge unbalance problem exists in both charge mode and drivemode.

Cascade inverters are ideal for an induction motor that has many separate dc sources and (batteries) available for the individual H-bridges, these inverters are not an option for series of hybrid inductionmotors because cascade inverters cannot be easily connected back-to-back. For series-configured induction motors where an onboard combustion engine generates ac power via an alternator or generator, a multilevel back-to-back diode clamped converter drive can

best be interface with the source of ac power and yet still easily meet thehigh power and/or high voltage levels requirements of the induction motor

2. Simulation Circuit

In the proposed 7-level MLI, the circuit is built of 5 MOSFET unidirectional switches. It can also be built with 3 unidirectional and 2-bidirectional switches. The load is resistive with a value of 10 ohms. Four 10-volt symmetric DC input voltages are used Figure 6 represent the simulation circuit of the proposed topology.

Note that in order to obtain the shaped 7-level output without distortion, MOSFET block parameters in MATLAB should vary according to the load used. Here for 10-ohm resistive load, MOSFET block parameters are set as follows:

FET resistance = 0.01 ohms, internal diode resistance = 10 kilo ohms.

Methodology

The pulse generation is essential in order to trigger the switches with appropriate pulse pattern to produce the desired 7-level output. It is inevitable to analyze which PWM suits the new topology. The simplest PWM technique is the carrier-based PWM (CBPWM) technique. It can be further categorized into level and phase shifting CBPWMs,

respectively. Since the phase shifting CBPWM yields more harmonics comparatively, the level shifting CBPWM is preferred over it. Therefore, the new circuit design is analyzed with level shifting carrier -based PWMs, that is, PD, POD, and APOD PWMs. Interestingly, it is noted that POD gives lower THD and is found to be theapt PWM for proposed topology. The PWM generation circuit is the heartof the circuitry. One reference sine waves of amplitude 0.8 and frequency 50 Hertz is compared with C1 to C6 triangular carriers of frequency 1 KHz. If m-level needs to be synthesized, (m − 1) carriers are required.

Whenever the reference sinusoid exceeds the carrier, instant pulses are generated to trigger the switch to 0N state. Higher triangular carrier amplitude is taken as one.

The carrier alignment for the carrier based PWM technique is shown in Figure 7. In PD or phase disposition technique, (m−1) carriers are alignedin the same direction/phase.

In POD or phase opposition disposition for 7-level, 6 carriers are aligned as symmetric mirror images above and below the Zero reference axis. In alternate phase opposition disposition, alternate carriers are in the same phase and neighboring carriers in the opposing phase.

Simulation Results

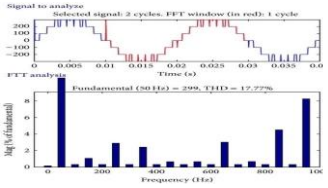


Fig.10 FFT analysis of existing 6-switch topology using PD pwm

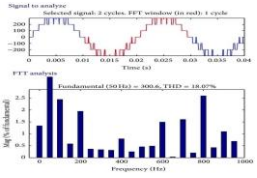


Fig 13 FFT analysis of proposed topology using PD PWM

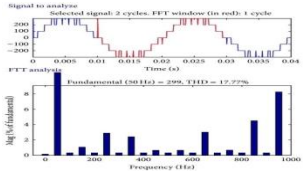


Fig. 11 FFT analysis of existing 6-switch topology using POD PWM

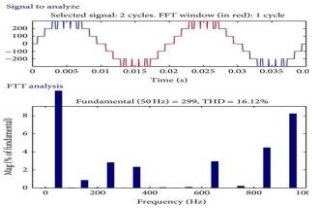


Fig 14 FFT analysis of proposed topology using POD PWM

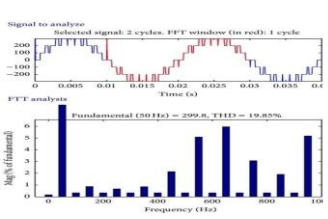


Fig. 12 FFT analysis of existing 6-switch topology using APOD PWM

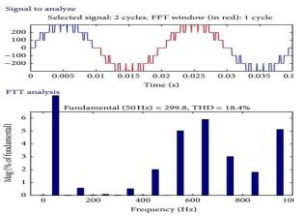


Fig 15 FFT analysis of proposed topology using APOD PWM

Conclusion

The 7-level MLI using just 5 switches is successfully introduced simulating the circuitry using MATLAB/SIMULINK and observed a clear stepped 7-level waveform. It is found that the POD-PWM dominates all other PWMs in the proposed configuration. The new design is simple in its outlook with very few components. The novel 7-level MLI has lower THD compared to conventional symmetric and asymmetric topologies.

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