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A Comparative High Frequency Performance Analysis of GFET

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Abstract: Graphene has been extensively investigated in the context of electronic components due to its attractive properties, such as high carrier mobility and saturation velocity. In the past decade, the graphene field-effect transistor (GFET) has been considered one of the potential devices to be used in future radio frequency (RF) applications and can help usher in the Internet of Things and the 5G communication network. This review presents recent developments of GFETs in RF applications with a focus on components such as amplifiers, frequency multipliers, phase shifters, mixers, and oscillators. Initially, the figures of merit (FoMs) for the GFET are briefly described to understand how they affect these RF components. Subsequently, the FoMs of GFET-based RF components are compared with other non-GFET-based RF components. It is found that, due to its zero-band gap and ambipolar characteristics, GFETs are more suitable for use in frequency multiplier and phase shifter applications, outperforming non-GFET-based RF components. Finally, future research on GFETs themselves as well as GFET-based RF components is recommended. This review provides valuable insights into such components that could give rise to innovative applications in industry

Keywords: Current gain, f_T and f_{MAX}, graphene, graphene FET (GFET).

1 INTRODUCTION

Transistors are fundamental requirement of all the modern-day electronics. These days, mass production of Si MOSFETs of 20nm gates is going on. As physical limitations are there in crystalline form of silicon under 10nm, so, research for technology rather silicon is in high demand [1]. Graphene has been taken for its capable use in electronics because it was firstly known a material which would take place of silicon and which could make devices faster and less tedious to manufacture. Even it remains highly reliable and conducting, when it is molded into devices 1nm wide.

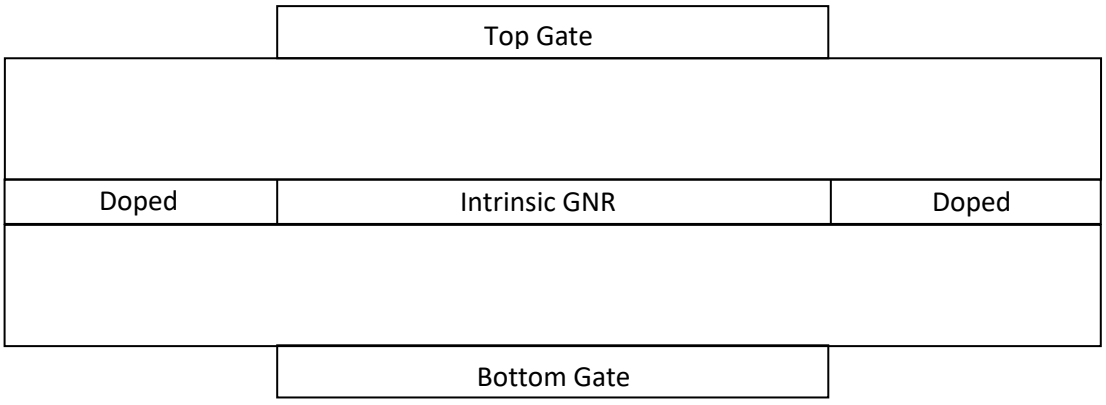

Figure 1: Cross sectional geometry of Graphene Field Effect Transistor.

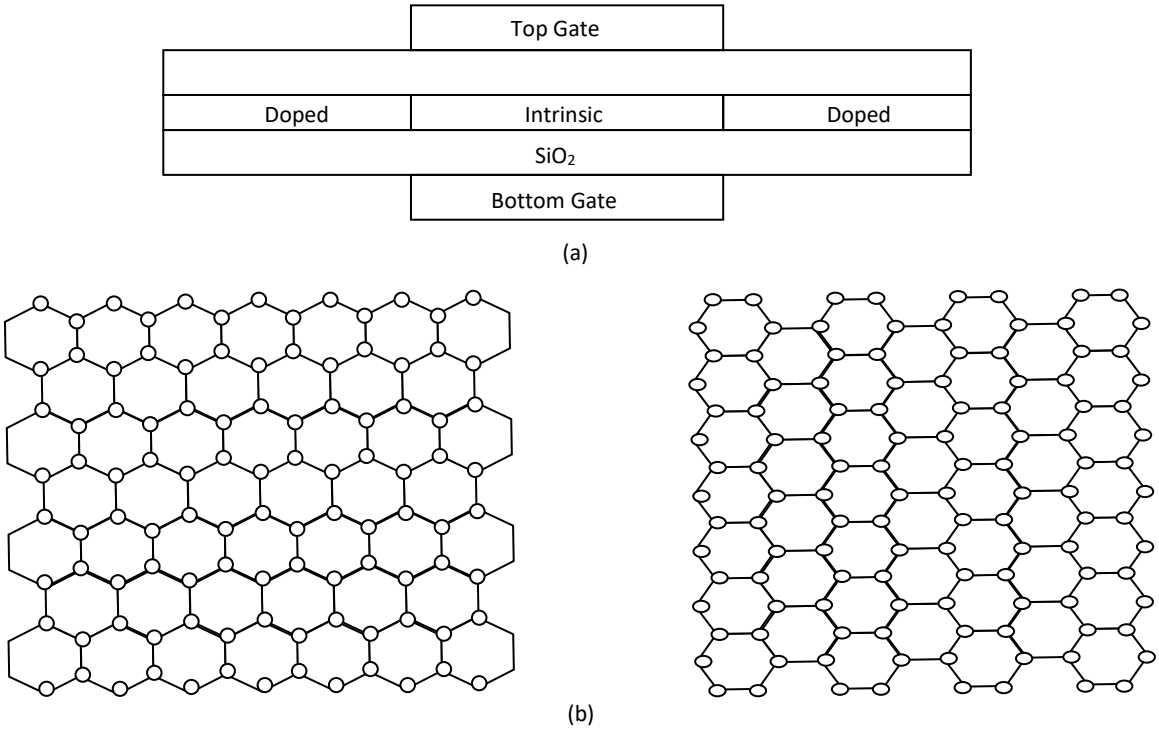

Figure 2(a-b) Graphene nanoribbon FET

2. GFET SIMULATION OF THE STRUCTURE

Figure 8.1(c) depicts simplified diagram of the proposed design[2]. Deposited over the SiO_2 layer graphene layer is used as channel layer.

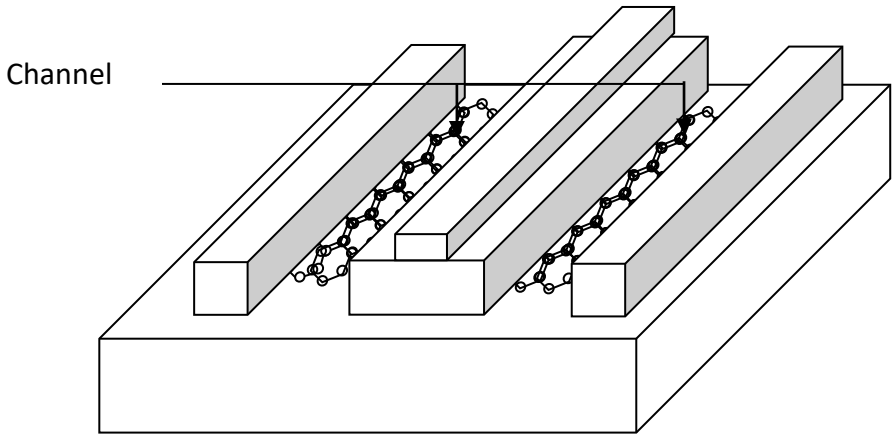

Figure 3 (c) Proposed Structure of GFET

RF Performance Simulations

We have considered a prototype h-BN encapsulated GFET, the scheme of which is depicted in Fig. 1. The h-BN/graphene/ h-BN stack is on the top of a thick SiO2 layer, which is, in turn, on the top of a highly doped Si wafer acting as the back gate. We have considered 30-nm-thick h-BN top and bottom layers with relative permittivity of 3 [3-5] and a 285-nm SiO2 layer

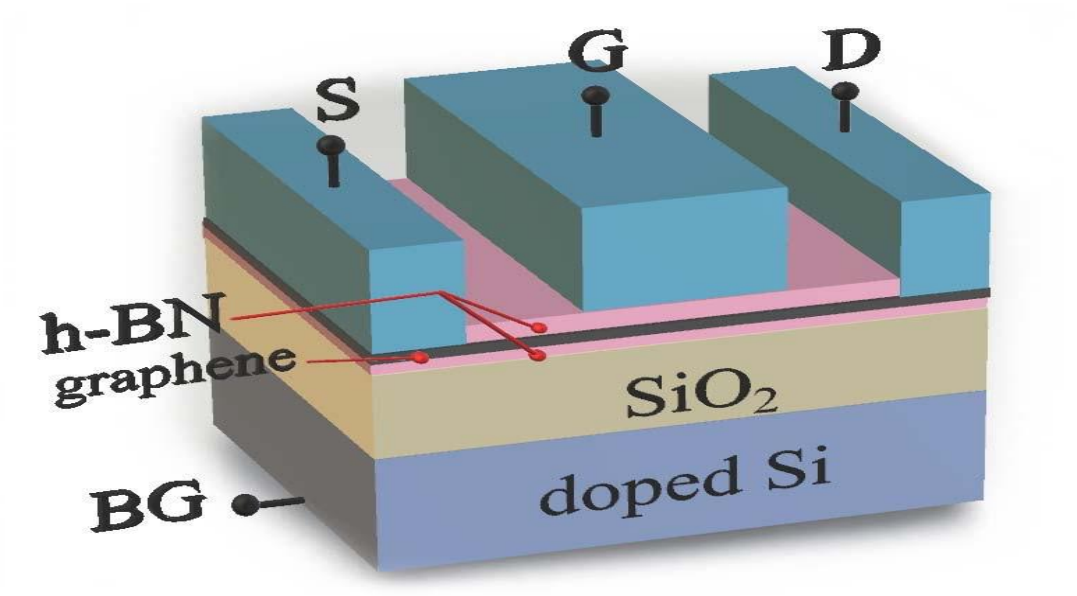

Fig. 1. Schematic of the h-BN encapsulated GFET considered in this paper. The terminals are named as S (source), G (gate), BG (back gate), and D (drain).

with relative permittivity of 3.9, which are typical values for h-BN encapsulated GFETs [1], [16]. Drain and source series resistances are assumed to have the state-of-the-art values of 100 □ · μm [17]. Narrow width effects can be neglected since channel width has been considered sufficiently large.

Low-field carrier mobility μLF and carrier saturation veloc- ity vsat in h-BN encapsulated graphene were obtained by a self-consistent ensemble Monte Carlo (EMC) simulator at steady-state conditions that accounts for the scatter- ing mechanisms in this particular encapsulated graphene structure [6-8]. The scattering mechanisms include graphene intrinsic phonons, remote SPPs from h-BN encapsu- lating layers, carrier–carrier collisions, and scattering caused by defects and charged impurities. A complete description of the formalism used for each scattering mechanism and the parameters chosen can be found in the supplementary material of [9]. Moreover, the hot phonon effect is also included, which is particularly important at high-field conditions in graphene [10]. The levels of impurities and defects have been adjusted so the carrier mobility as a function of the carrier concentration *n* fits the experimental values obtained for h-BN encapsulated graphene in [11]. The values presented here are obtained considering the average velocity for a large number of particles in the simulation and an additional time average once the stationary conditions are reached. The statistical uncertainty is noticeably small: when using five different seeds for

the random number generation, the standard error is less than 0.7% in the worst case, which clearly indicates that the numerical error is minimum. A number of particles between 4×10^4 and 4×10^5 have been considered in the simulations, depending on the carrier concentration. This guarantees that the margin of error in the results for a 99% confidence level is less than 0.7%. The results for μ_{LF} and v_{sat} have been plotted in Fig. 2(a) and (b), where it can be observed that both magnitudes tend to decrease with the carrier concentration, reaching an approximately constant minimum value for carrier concentrations above 10^{13} cm^{-2}.

Throughout this paper, we assume that the grain boundaries in graphene are not affecting the carrier transport[12]. This should be valid for monocrystalline graphene and polycrystalline graphene samples with grain size much greater than the chan- nel length. The grain size, in the latter case, is quite sensitive to the growth technique and values of mobility ranging from 2500 to 350 000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ have been reported in the literature; the former case corresponding to all chemical vapor eposited (CVD) h-BN/graphene/h-BN samples [13], and the latter case to transferred CVD graphene encapsulated between exfoliated h-BN layers [14].

Importantly, EMC simulations allow calculation of the mean free path (MFP) and differentiation of the contribution of each scattering mechanism. Fig. 2(c) confirms that the MFP is smaller than the channel length *L* in all cases of channel length and carrier concentrations in graphene considered in this paper, which guarantees the validity of the drift-diffusion mechanisms as the driving forces of the carrier transport[15]. The separate influence of different scattering mechanism types can be perceived in Fig. 3, where the average number of scattering events suffered by a carrier per unit time is presented as a function of the electric field for several carrier concentra- tions. Carrier–carrier scattering is the dominant mechanism[16]. However, given its Coulombic nature and the momentum and energy conservation laws for the pair of interacting particles, the influence of each individual collision on the total velocity of colliding carrier pairs is minimal due to the preferred small wavevector transitions, therefore, implying a reduced influence on saturation drift velocity and specially in mobility in comparison with other types of mechanisms. Moreover, at larger carrier concentrations and low fields its rate for each single electron is lower due to the Pauli exclusion principle that restricts carrier–carrier interactions to those particles close to the Fermi surface [17].

TABLE 1. Material Parameters of GFET

Band Gap E_g (eV)	Permitivity (χ)	Electron Mobility μ_n (cm^2/V-s)	Hole mobility μ_p (cm^2/V-s)	Affinity X (kg/mole)	Electron Saturation Velocity V_{sat}
0	25	10000	10000	4.248	4x

List of design requirements in modeling the structure is given in Table 8.2. The channels dopping is source or drain as heavy doping in n-type $1x10^{20}cm^3$ and p-type $1x10^{16}cm^3$, to meet specific ITRS physical gate length requirement conditions to device simulation

TABLE 2 Proposed Design Parameters

Parameters	Gate length (L) nm	Dielectric thickness (nm)	Channel doping (cm^3)	Drain/Source doping (cm^3)	Substrate doping (cm^3)
Values	350	5	$1x10^{15}$	$1x10^{20}$	$2x10^{15}$

5. RESULTS AND DISCUSSION

5.1 I-V CHARACTERISTICS

Transfer characteristics of 350nm gate GFET, simulated with a Vds of 0.1V and 0.2V are shown in Figure 8.2. The transfer curve (I_{DS} vs V_{gs}) for gate-source voltage Vgs varying from -3.5 to +3.5V and drain-source voltage V_{DS}=0.1V and Vds=0.2V. The curve in figure 3 is experimental as well as theoretical expectations shows second linear region . The output curve for all +ve and -tive values of V_{GS} with different gate length is analyzed to study properties of graphene-channel to change in the conductivity through top-channel, as V_{DS} is changed from 0 to 3.5V at V_{step} = 0.1V. The predicted behavior output is shown .

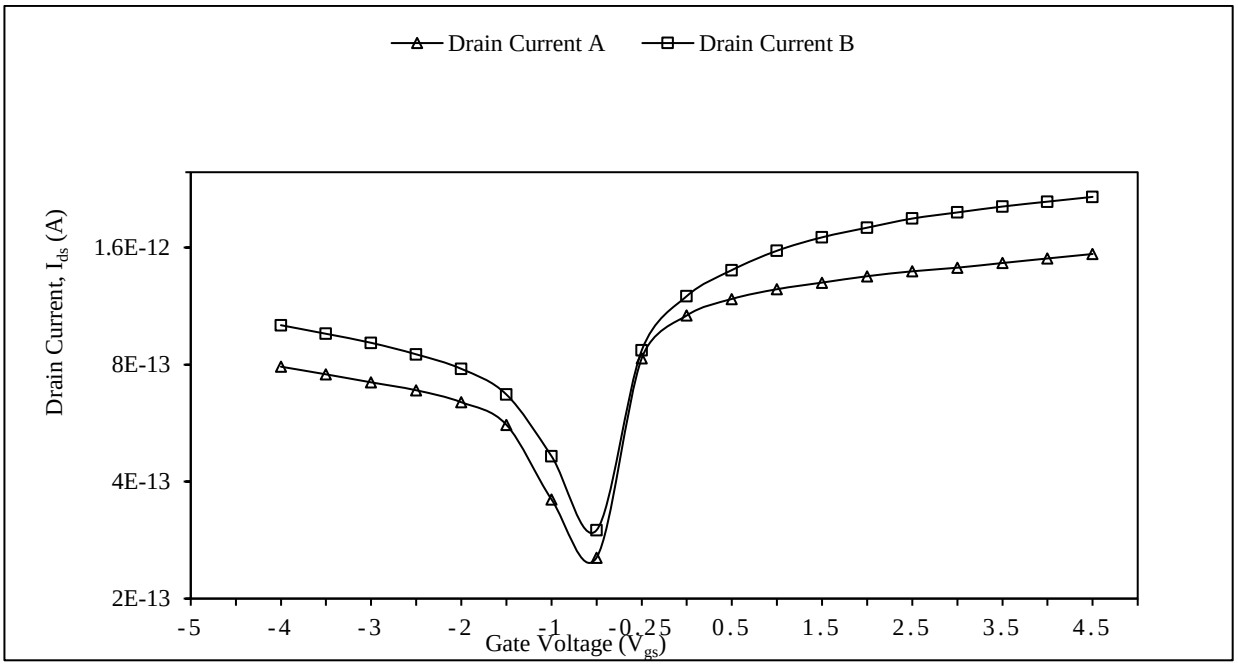

FIGURE 4: V-I curves of the device simulation shows transfer curve

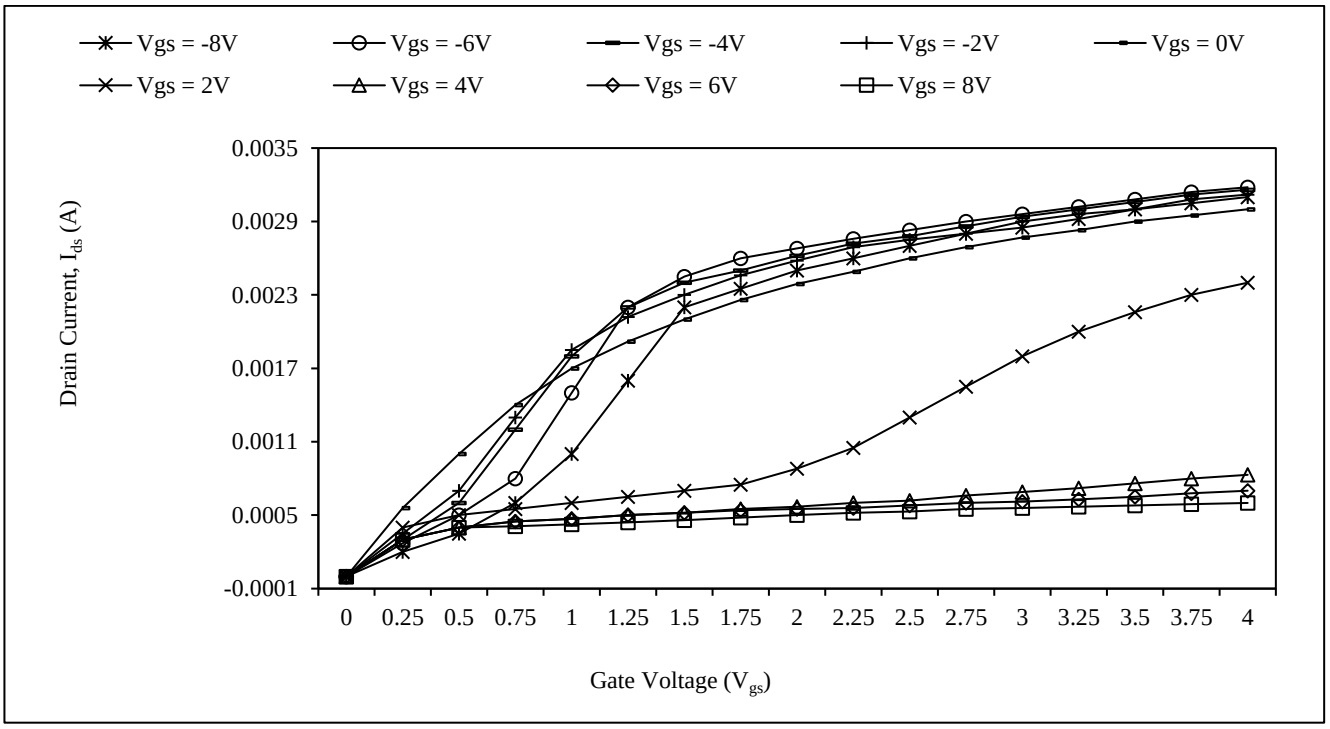

FIGURE 5: V-I simulated output characteristics curves

5.2 RF PARAMETERS

The RF application FoMs are transconductance, having cut-off frequency alongwith maximum cut-off frequency (f_T) . Intrinsic capacitances have been shown in figure 8.4(a-b), C_{gs} and C_{gd} are functions of V_{gs} for sub-threshold. This plot of capacitances curves, C_{GD} and C_{GS} were done on AC small signal. The capacitances between electrodes are measured at 1GHz using a DC slope signal ranging from 0V to 2.5V steps of 0.1V each. To make more robust solution of inversion/deep depletion region the DIRECT parameters may be added.

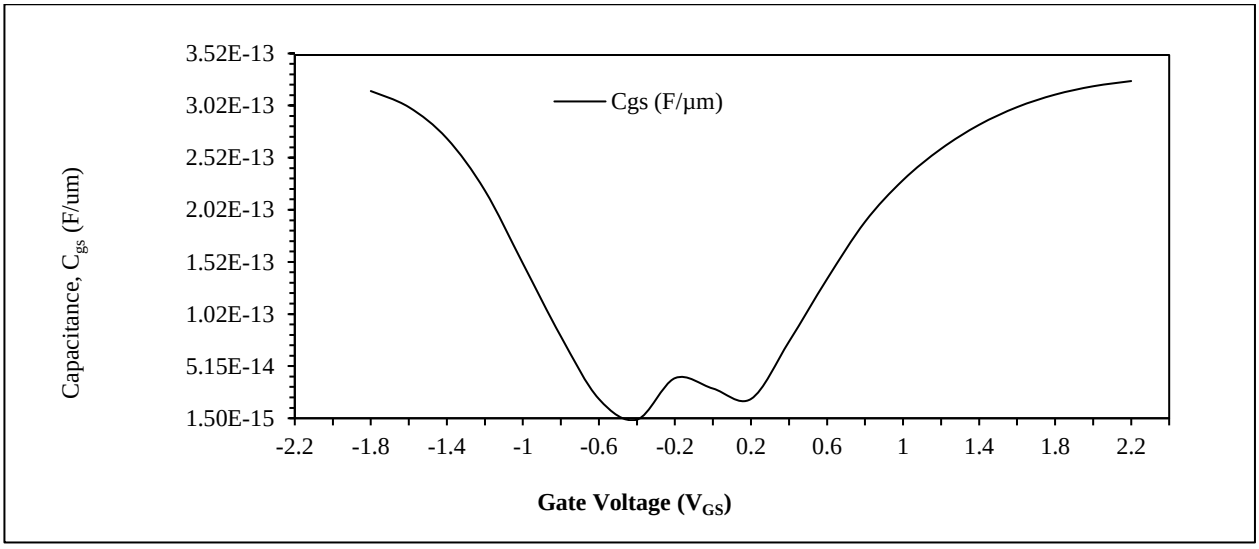

FIGURE 6: Capacitance curves showing capacitance between gate and source, C_{gs}

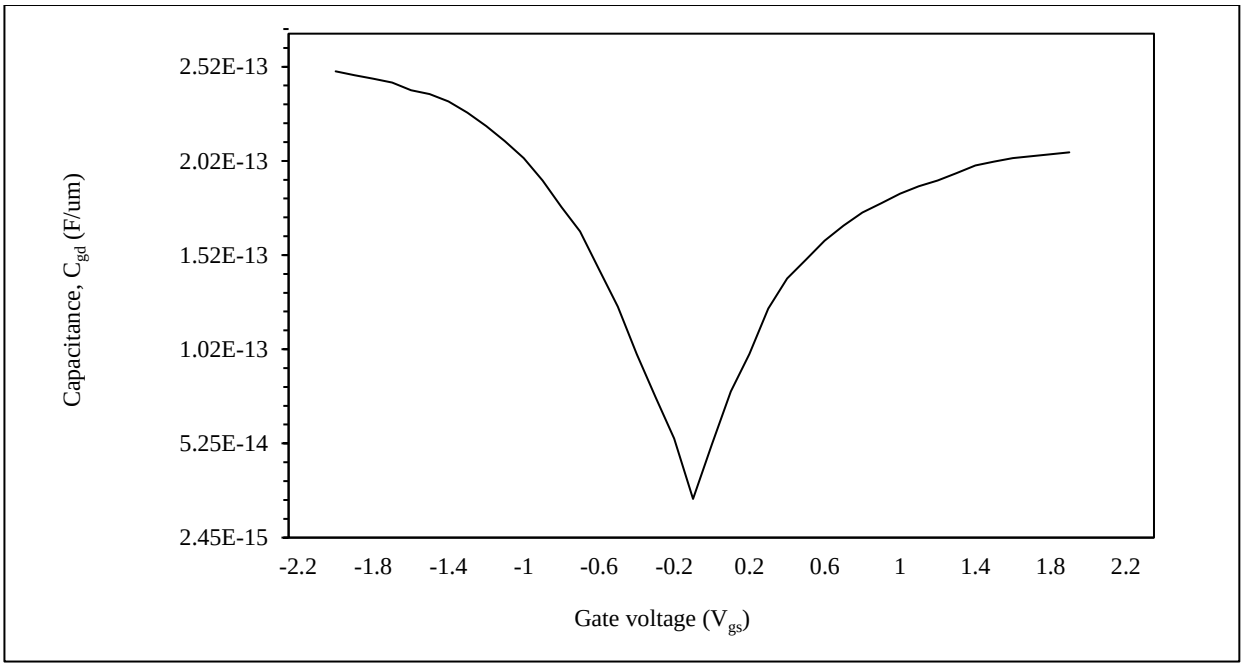

FIGURE 7: (b) Capacitance curves showing capacitance between gate and drain, C_{gd}

The frequency as current gain approaches unity is cut-off frequency and frequency as the power gain approaches maximum cut off frequency . In figure 8.5(a-b), unilateral power gain and current gain are plotted to extract exact values of f_{max} and f_T.

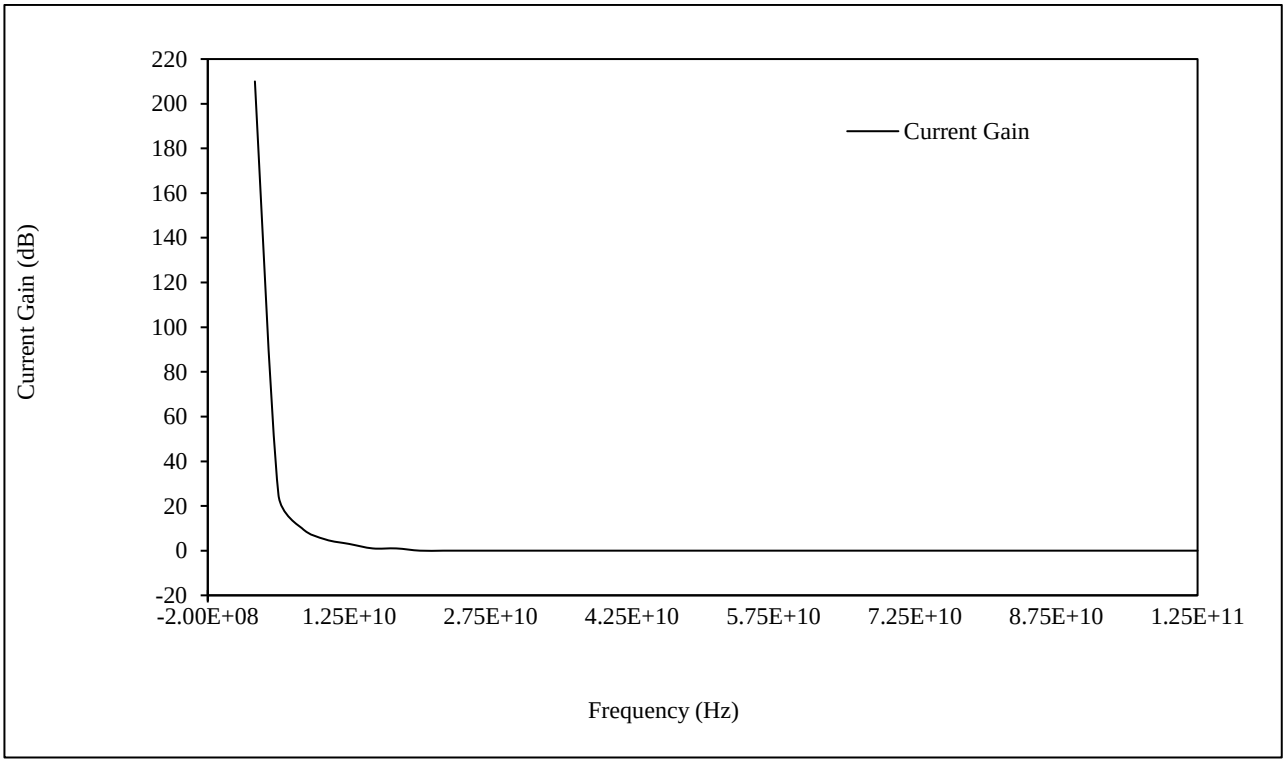

FIGURE 8: (a) current gain curves to extract and fmax and f_T

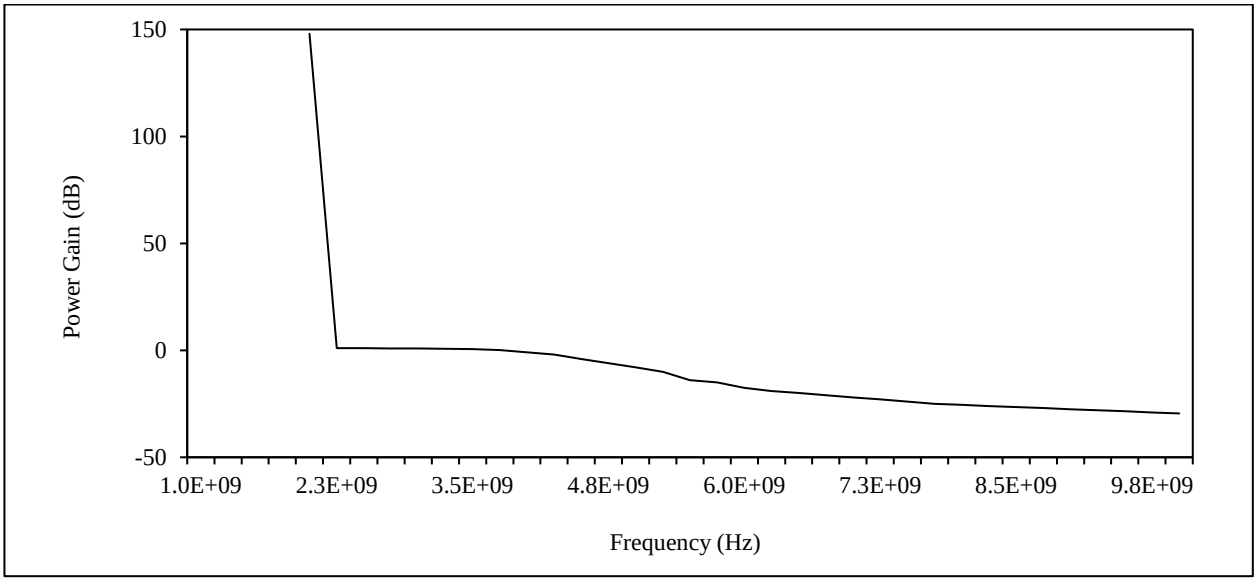

FIGURE 9: (b) Curves to extract f_T and f_{MAX} for power gain curve

5.3 CHANGING THE CHANNEL LENGTH

The simulation task started with changing the channel length because channel length is the most vital parameter of electronic industry. Channel length which is more formally called as the technology is so much significant that the manufacturer rate the device on basis of its channel length [189]. Lesser is the channel length better is the technology. This thesis discusses variation in channel length. As we increase the channel length, the channel current starts decreasing. The current of the channel becomes highest when the length of channel is reduced to 100nm. These results are obtained by the simulation of GFET as shown in figure 8.6.

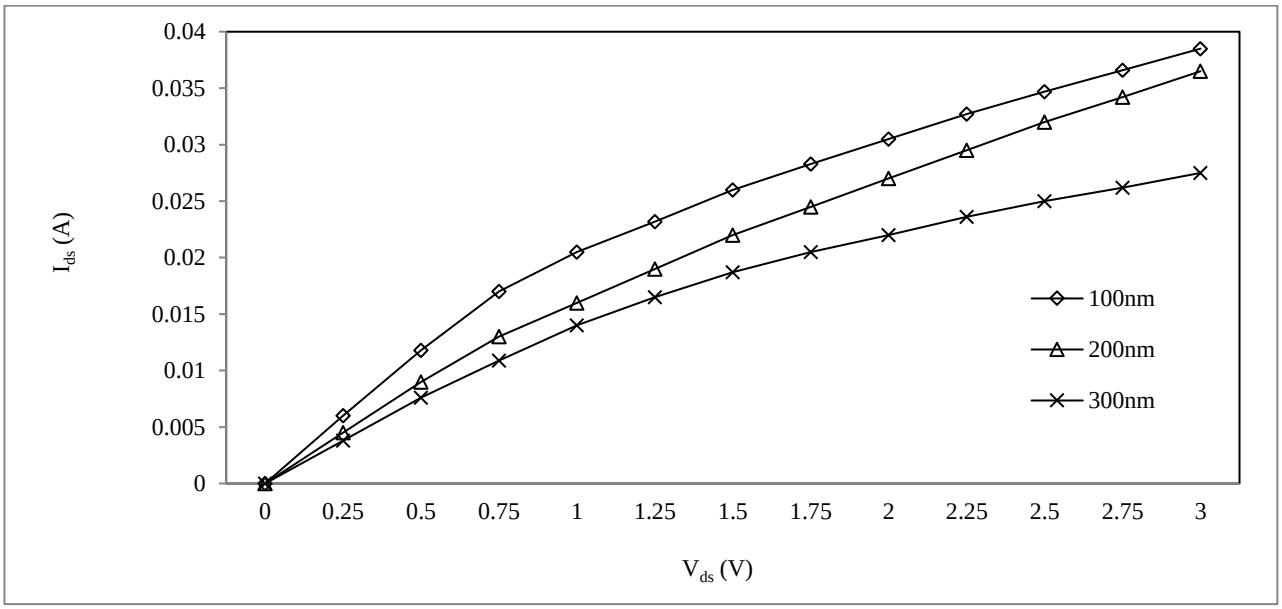

FIGURE 10: Output characteristics of GFET at various channel length

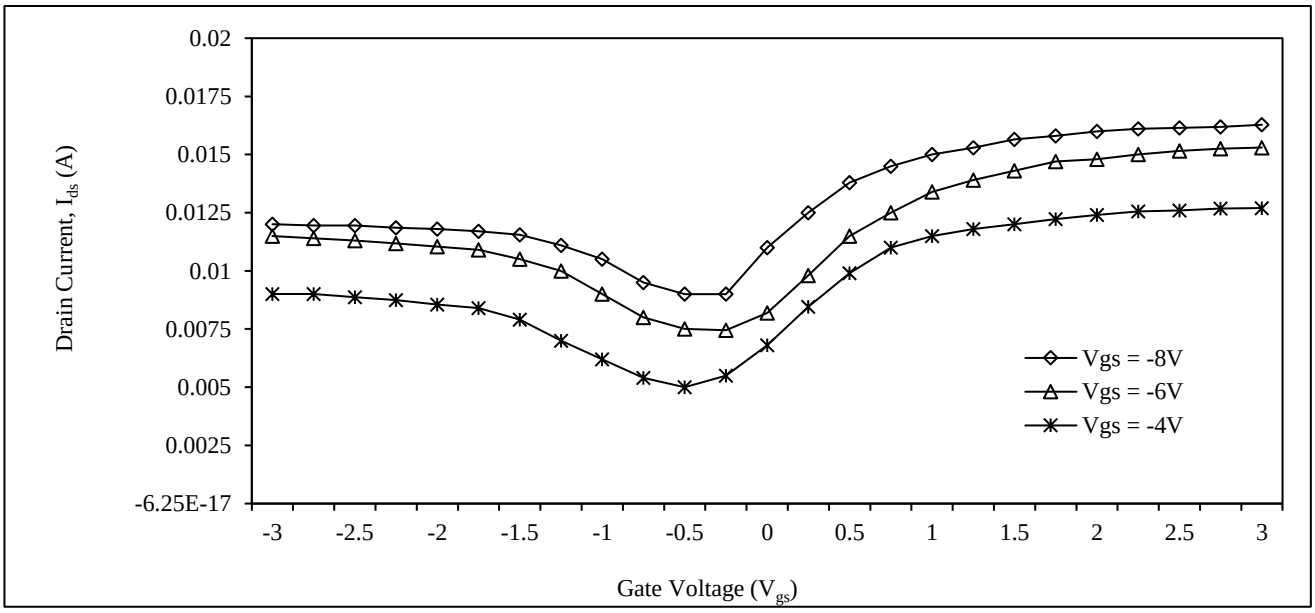

FIGURE 11: Input characteristics of GFET at drain voltage of 0.3V at different channel lengths

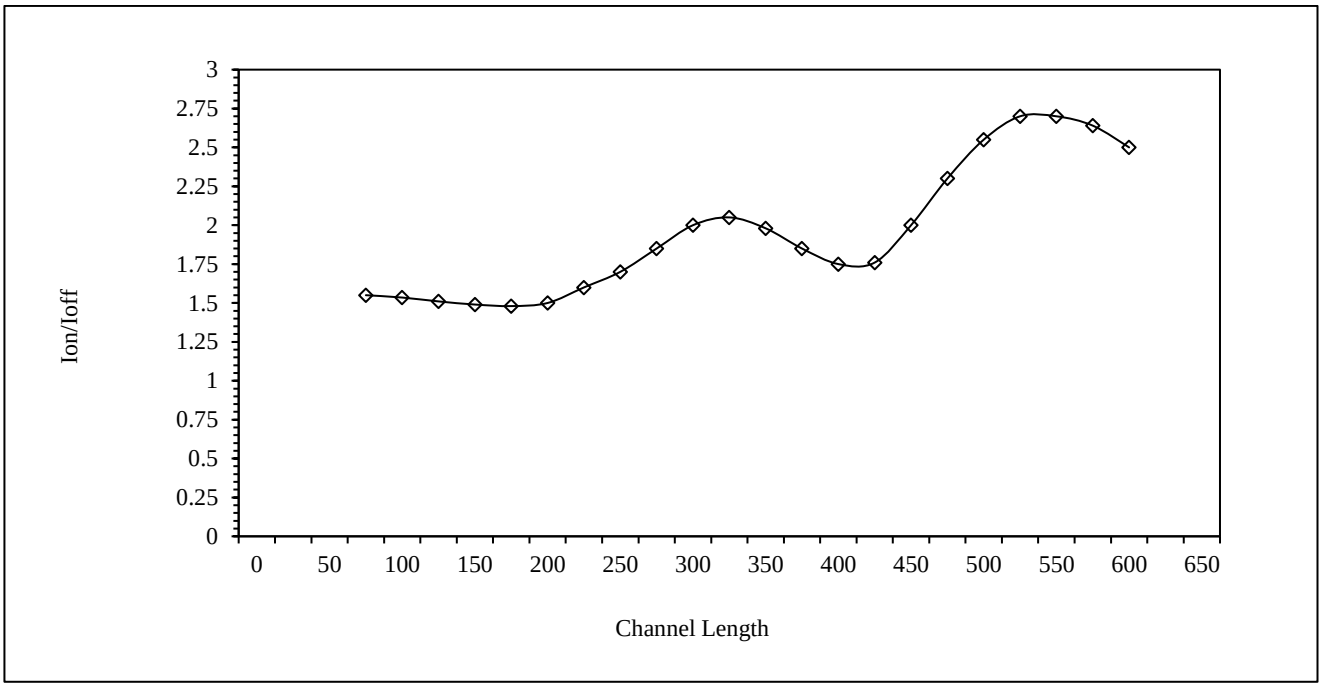

FIGURE 12: I_{ON}/I_{OFF} Vs channel length at drain voltage of 0.3 V

Figure 8.7 depicts input characteristics of device at various channel lengths. These plots gives the idea the as the channel length reduces more charge density is there and more is the current so at minimum channel length of 100nm we have the maximum current value. But as we decrease the channel length the I_{ON}/I_{OFF} ratio is increased as shown in figure 8.8.

6. CONCLUSION AND FUTURE SCOPE

The 2D device simulator (classic) is used to present a novel engineering approach for simulating Radio frequency characteristics of GFET. The performance parameters of ac analysis are done. The evaluation of RF and design/characteristics of GFET has been done. The maximum oscillation frequency (f_{MAX}) and cut-off frequency (f_T) are found with good estimation. The output characteristic and transfer curve are drawn to plot characteristics curves. There is much research going on for progressive various models for graphene field effect transistor (GFET). A comparative study can be done w.r.t. various physics models. Also the physics model can be developed in other languages like verilog or Hspice keeping all the optimized parameter in mind .

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