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A Comprehensive Review of Power Consumption in Digital Logic Circuits at Ultra-Low Subthreshold CMOS Levels

[1]Tripti Raj Laxmi , [2]Prof. Dilip Kumar, [3]Sandip Nemade
[1,2.3.4]Technocrats Institute of Technology, Bhopal
[1]Gmail id - triptirajlaxmi@gmail.com
[2]Gmail id - dilipgin23@gmail.com
[3]Gmail id - nemadesandiptit@gmail.com

Abstract— **In the anticipated spectrum, a lot of work has gone into managing the trade-offs between power, location, and efficiency in the moderate efficiency, moderate power region. However, research into the extremities of this spectrum remains restricted. In particular, there hasn't been enough research done on the extremes of extraordinarily low power consumption with appropriate efficiency and extraordinary efficiency with energy that is within realistic bounds. In this work, very low subthreshold power levels are used to study the power consumption characteristics of digital logic circuits in static Complementary Metal-Oxide-Semiconductor (CMOS) devices. The study shows that operating transistors below their threshold voltage might result in significant energy savings. This research emphasises the significance of subthreshold design strategies for contemporary electronic circuits that aspire for low-power operation without sacrificing efficiency. The results highlight the potential for significant progress in energy-efficient circuit design and highlight the delicate balance between preserving performance and cutting power usage. As a result, this research adds to our understanding of low-power electronics and provides information that may lead to the development of future technologies that are more efficient and sustainable.**

Keywords— Power consumption analysis, Digital logic circuits, Ultra-low power, Subthreshold operation, Static CMOS gates

I. INTRODUCTION

The growing need for low-power Very Large-Scale Integration (VLSI) has forced advances in a number of design levels, such as the technological phases related to building, circuitry, structures, and procedures. Choosing the right logic type during the circuit design phase is essential because it affects all of the important variables that effect power loss, such as shifting capacitance, transitional action, and short-circuit power currents. This work extends to a broader class of logical gates, enabling both qualitative and quantitative comparisons of energy degradation qualities. Previous research have mostly concentrated on particular logical cells.

The increasing need for low-power Very Large-Scale Integration (VLSI) can be satisfied by utilising a number of design layers, including constructional, circuit, structural, and procedural technological phases [1]. A multi-element circuit can save a significant amount of energy during the circuit design phase by choosing the right logic type. This is due to the fact that all the important variables that effect power loss—such as shifting capacitance, transitional action, and short-circuit power currents—are greatly impacted by the logic type selected [2]. It is impossible to create universal rules for perfect logical designs since different efficiency factors need to be taken into account depending on the application, kind of circuitry, and design methodology.

Energy dissipation plays a crucial role in VLSI design, and energy consumption is given special significance by sub micrometer and nanoscale approaches. Interest in

low-power goods has increased due to the growing popularity of battery-operated portable devices and the emphasis on energy conservation in embedded circuits. Knowing the power characteristics of digital logic circuits in static CMOS gates is crucial since operating these circuits at subthreshold voltages drastically lowers power usage.

This study investigates and evaluates the energy-use behaviour of digital logic circuits inside static CMOS gates when they are functioning in the subthreshold range. The study intends to illustrate the efficiency and trade-offs of subthreshold logic circuits in comparison to conventional CMOS techniques by thoroughly assessing energy consumption.

Nevertheless, research on low-power logical types that have been published in the literature has largely focused on particular logical cells that are utilised in particular mathematical circuitry, like complete adders [3]. These investigations are extended by this study to a far wider class of logical gates and, consequently, to any combination of circuits. Energy degradation qualities of various current logic designs can be compared both qualitatively and quantitatively thanks to real-world logic gate constructions and computations under realistic circuit configurations and operating settings [4].

Energy dissipation is one important consideration that must be made in VLSI design. Submicrometer and nanoscale techniques have now given energy consumption a distinct relevance, whereas in the early days of computerised circuit design, the main concerns were efficiency and die surface. When many technical node choices are unavailable, it is critical to carefully select methodologies and circuit designs in order to realise the greatest energy savings possible during this stage of the design process [5].

The popularity of battery-operated portable devices and the increased emphasis on energy efficiency in embedded circuits have led to a recent spike in demand for low-power goods. Virtual logical circuits that function at incredibly low voltages below the threshold have been proposed as a possible remedy for this issue [6]. By using transistors in the below-threshold region—where the gate-source voltage is below its threshold potential—below-threshold operations significantly reduce power consumption when compared to standard CMOS operations. To optimise their usefulness and incorporate them into contemporary electronic devices, it is vital to comprehend the power characteristics of these circuits in static CMOS gates [7].

The aim of this work is to investigate and evaluate the energy-use behaviour of digital logical circuits in static CMOS gates operating in the below-threshold region. This study intends to clarify the economics and efficacy of below-threshold logical circuits in contrast to conventional CMOS techniques by a comprehensive assessment of energy consumption [8]. Along with looking into additional efficiency criteria, the study project will also examine trade-offs related to below-threshold operation, such as speed, noise margins, and robustness against processing swings. These realisations are critical to propel future generations of low-power device circuit builders forward and elevate the bar for affordable digital electronic technology [9].

II. RELATED WORKS

Dynamic power elements and static power elements are the two basic categories into which energy utilisation in contemporary VLSI circuits can be divided. Typically, dynamic power consumption happens when the output nodes of the gate receive a transitional signal. Due to its two independent components—the charging and discharging of circuit capacitors and short circuits brought on by finite slopes in the input signal transitions—all networks are nonetheless able to function simultaneously [10]. As a result, the current has a low-resistance path from the power supply to the rails. As this essay concentrates on, efficiency is not the main consideration when planning for extremely low energy loss. Electronic circuits operating in sub-threshold state is one method for achieving this goal [11].

The reason for running the system in subthreshold mode is the ability to employ subthreshold leakage current as the operational driving power. Gate voltage and subthreshold current have an exponential connection, which is expected to cause delays to increase significantly and energy consumption to decrease significantly [12]. The results of the simulation show that power consumption often decreases with each shift because the voltage decrease is greater than the lag gain [13].

Dynamic power elements and static power elements are the two main categories of energy consumption in contemporary VLSI circuits. At gate output nodes, dynamic power consumption usually happens during transitional signals, whereas static power elements are linked to undesired power currents brought on by less-than-ideal devices. With subthreshold leakage current serving as the operational driving force, this work focuses on the subthreshold mode operating of electronic circuits. The subthreshold current and gate voltage exponential connection leads to a notable energy savings, but at the expense of longer delays.

Because logic type selection affects wire complexity, dimensions, energy consumption, and speed, it is critical to circuit efficiency. Few studies compare the energy consumption of extremely low-energy subthreshold digital logic devices with typical CMOS static gates, despite the variety of logic types. Furthermore, the efficiency trade-offs between CMOS and subthreshold circuits in static environments, as well as the difficulties in integrating and scaling subthreshold logic circuits into existing CMOS designs, have not received much attention.

S. No.	Title	Year	Methodology	Advantage	Limitation
1	Power Consumption Analysis of CMOS Gates Using Subthreshold Leakage Reduction Techniques	2019	Subthreshold leakage reduction techniques	Significant power savings in CMOS gates	Increased design complexity
2	Efficient Low-Power CMOS Gate Design with Improved Power-Delay Product	202	Power-delay product optimization	Enhanced power efficiency and performance	Trade-offs with circuit speed
3	Analysis of Power Consumption in CMOS Inverter Circuits Operating at Ultra-Low Power Levels	2019	Ultra-low power design methodologies	Reduction in energy consumption	Lower performance in speed and noise margins
4	Ultra-Low-Power Digital CMOS Circuit Design Using Subthreshold Techniques	2020	Subthreshold operation techniques	Substantial power reduction	Susceptibility to process variations
5	Power-Efficient CMOS Logic Circuit Design for Low-Power Applications	2019	Energy-efficient logic circuit design	Improved power efficiency	Limitations in scaling

6	A Comprehensive Study of Low-Power CMOS Gate Techniques for IoT Devices	2020	Low-power design for IoT applications	Enhanced power efficiency for IoT devices	Potential performance trade-offs
7	Evaluation of Power Consumption in CMOS Digital Circuits Using Dynamic Voltage Scaling	2020	Dynamic voltage scaling	Optimized power consumption	Increased circuit complexity
8	Design and Analysis of Low-Power CMOS Gates with Adaptive Body Biasing	2019	Adaptive body biasing techniques	Improved power efficiency and adaptability	Complexity in design implementation
9	Energy-Efficient CMOS Gate Design for Subthreshold Operation	2019	Energy-efficient subthreshold operation	Reduced power consumption	Lower speed performance
10	Low-Power CMOS Logic Design Using Multi-Threshold Techniques	20	Multi-threshold CMOS techniques	Enhanced power savings	Increased susceptibility to noise

Table 1: Showing Recent works CMOS Gate

Research Gap

Very few research compares the energy consumption of below-the-threshold digital logic devices and standard CMOS static gates.

The trade-offs between CMOS and below-the-threshold circuits in terms of efficiency (speed, resilience) in static environments have not received enough attention.

The difficulties in incorporating and scaling below-the-threshold logic circuits into existing CMOS architecture designs are not well studied.

Research on the effects of below-the-threshold operations on circuit durability and variation control in static CMOS situations is scarce.

III. PRELIMINARIES

Subthreshold Operation

In the subthreshold zone, when the transistor functions below its threshold voltage, digital circuits can function. In the subthreshold region, the drain current is determined by:

$$I_{DS} = I_O \exp\left(\frac{V_{GS} - V_{th}}{n\, V_T}\right)$$

Where I_0 is a scale factor, V_{GS} is the gate-source voltage, V_T is the thermal voltage, and n is a subthreshold swing coefficient.

CMOS Inverter Operation

A CMOS inverter's delay can be roughly expressed as follows:

$$T = \frac{C_{load}(V_{DD} - V_{thn})}{I_{DSp}(V_{DD} - V_{thp})}$$

Where C_{loud} is the load capacitance, V_{DD} is the supply voltage, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS transistors respectively, and I_{DSp} is the drain-source current of PMOS transistor.

Energy Consumption

An electronic circuit's energy consumption is computed as follows:

$$E = P \times T = \frac{1}{2} C_{load} V_{DD}^2$$

Where P is the power dissipation, T' is the operating time, C_{loud} is the load capacitance, and V_{DD} is the supply voltage.

Dynamic Power Dissipation

The dynamic power $P_{dynamic}$ dissipated during switching activities in CMOS circuits is given by:

$$P_{dynamic} = \alpha C_{loud} V_{DD}^2 f$$

Where α is the activity factor (average fraction of switches toggling per clock cycle); C_{loud} is the load capacitance being switched; V_{DD} is the supply voltage; f is the switching frequency.

Power Delay Product (PDP)

The power delay product quantifies the trade-off between power dissipation and circuit speed. It is defined as:

$$PDP = P_{dynamic} \times \tau$$

Where τ is the delay of the circuit

Energy Dissipation per Cycle

The energy E_{cycle} dissipated per cycle due to switching activity is:

$$E_{cycle} = P_{dynamic} \times \tau$$

Switching Energy

The switching energy E_{switch}, which is the energy consumed per transition of a node, can be approximated by:

$$E_{switch} = \frac{1}{2} C_{loud} V_{DD}^2$$

The analysis of dynamic power dissipation and energy consumption during switching activities in digital CMOS circuits relies heavily on equations (1–7). They are essential for maximising performance and power efficiency in integrated circuit design.

Static CMOS

Most static energy application comes from power currents that run through a system while it is not moving or in a continuous condition. It consists of all the unwanted power currents generated by the system's less-than-ideal devices. The subthreshold current (Isub), the opposite of the bias junction electricity, and the tunneled gate material electricity are three essential components required for the proper operation of electronic circuits, as seen in Fig. 1. Because the VDD and thresholds are near together, the first one takes place in the weakest inverted operations zone. It is the main source of dynamic loss in electronic VLSI circuits and can be identified by the following characteristics in Fig. 1.

$$I_{sub} = I_{off} . 10^{\frac{V_{GS} + n(V_{DS} - V_{DD}) - K_y V_{SB}}{S}} \quad (8)$$

Ioff is therefore below the threshold power and Ky is a technology-related factor for VGS=0 and VDS=VDD. It is evident that there is an exponential relationship between the voltage applied and the VGS and VDS of this component.

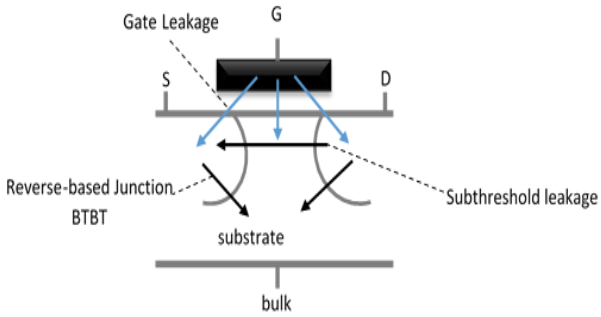


Fig 1. Illustration of static currents in MOS device

Power Consumption

Power can be divided primarily into two groups: static and dynamic parts. The first one often occurs when the gate output node presents an interim message. Two networks can still function simultaneously since they can still be classified into two types: the short circuit caused by the input transition's restricted slope and the charge/discharge of the connecting circuit capacitances. It creates a path with little resistance for electricity to go between the power source and the rails. The charging and discharging element has a form that is well known, to be exact. It depends on the node capacitor values, supply

voltage, and circuit velocity. This is an illustration of what is seen in Fig. 2.

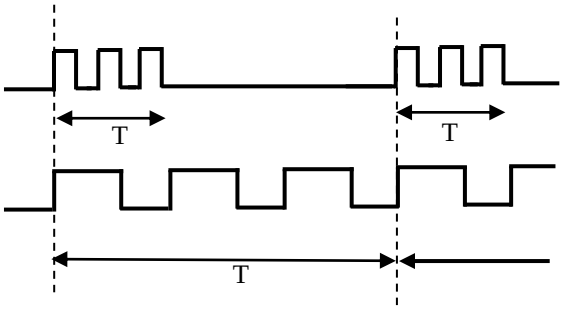


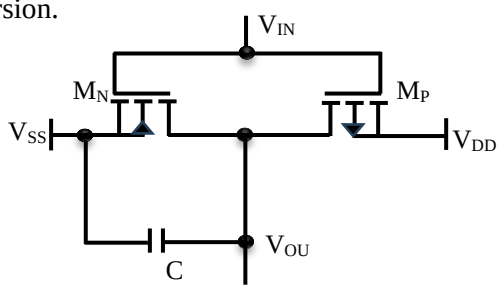
Fig. 2: Subthreshold circuit in bursty computation

IV. Circuit Design

The miniature signal circuit equivalent to a CMOS inverter with sub thresholds. The first type of assessment, depicted in Fig. 3(a) and (b), considers the Barkhausen stability requirements as well as the small-signal comparable description of the sub-blocks. This approach considers the single gates as operating at a specific point in time (biassing or linearity criteria) and analyses the entire system in the time domain.

Subthreshold CMOS Inverter Circuit

This circuit illustrates how an inverter functions at the subthreshold region, which is the weak inversion mode for both PMOS and NMOS transistors. With gate-source voltages V_{GSn} and V_{GSp} , respectively, below their threshold voltages V_{thn} and V_{thp}, the NMOS and PMOS transistors are biassed. It uses less power than conventional CMOS inverters to accomplish logic inversion.



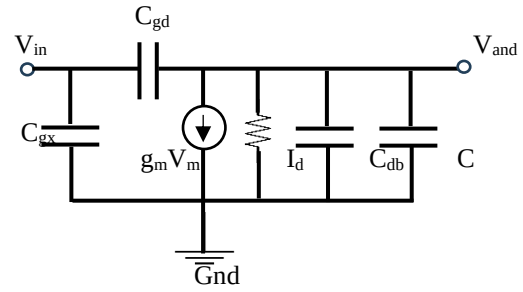


Fig. 3. (a) Conventional CMOS inverter (b) Small-signal circuit of sub thresholds CMOS inverter

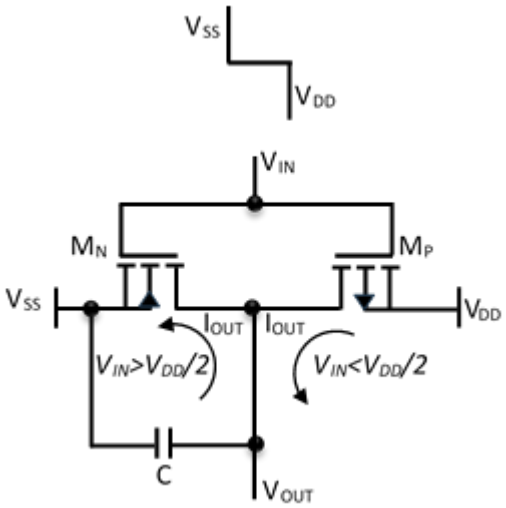
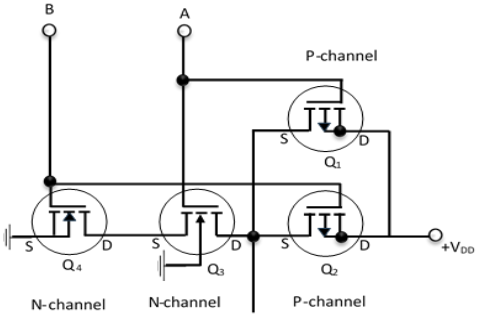


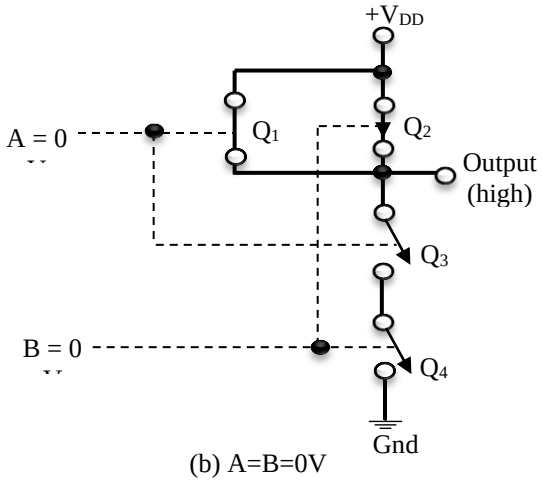
Fig. 4. Subthreshold CMOS Inverter

Subthreshold CMOS NAND Gate

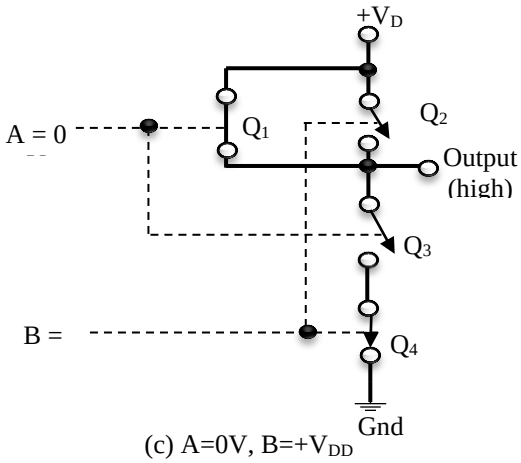
This design demonstrates the construction of a NAND gate using subthreshold CMOS logic. Multiple stages of below-the-threshold converters are connected to achieve NAND performance. Because subthreshold functioning reduces both static and dynamic power consumption, it is suitable for low-power applications.



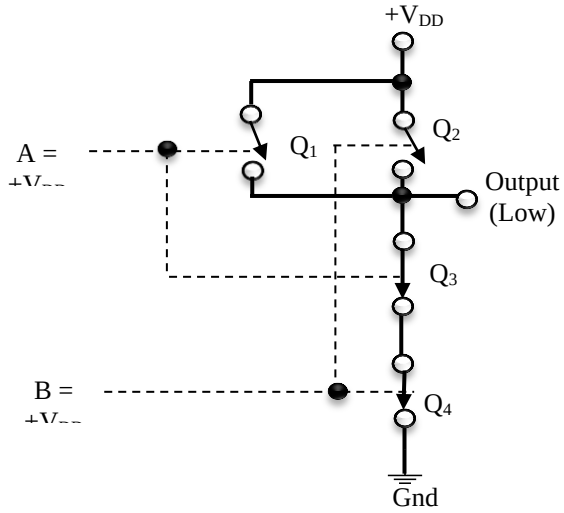
(a)



(b) A=B=0V
$V_{GS1} = V_{GS2} = -V_{DD}$
$V_{GS3} = V_{GS4} = 0V$



(c) A=0V, B=+V_{DD}
$V_{GS1} = -V_{DD}$
$V_{GS2} = V_{GS3} = 0V$
$V_{GS4} = V_{DD}$



(d) A=B=+V_{DD}
$V_{GS1} = V_{GS2} = 0V$
$V_{GS3} = V_{GS4} = +V_{DD}$

Fig 5. CMOS NAND gate

A Subthreshold CMOS NAND gate circuitry uses subthreshold operating concepts to achieve lower energy costs without compromising the functionality of traditional CMOS logic gates. This circuit design connects multiple levels of subthreshold CMOS inverters to produce a NAND gate. The transistors that comprise each step depicted in Fig. 5(a) through (d) are both NMOS and PMOS, and they are located below the threshold zone, where gate-source concentrations are lower than the corresponding criteria voltages. Because the result of each inverting phase is connected in series, the NAND gate's ultimate output is only low in this architecture when both inputs are strong.

This design approach significantly reduces both static and dynamic power consumption when compared to traditional CMOS NAND gates, making it suitable for battery-powered devices, biomedical implants, Internet of Things sensors, and other applications requiring ultra-low power operating. The subthreshold CMOS NAND gate exhibits low active power consumption and reduced current leakage, which underscores its potential for energy-efficient integrated circuit development for various low-power applications.

CMOS SRAM Cell Below Threshold

This section displays a Static Random-Access Memory (SRAM) cell made using subthreshold CMOS techniques. use memory made of subthreshold transistors to access nodes in the operation depicted in Figure 6. They are ideal for ultra-low energy use in storage controllers because they have less write/read electricity consumption and ocean current leakage.

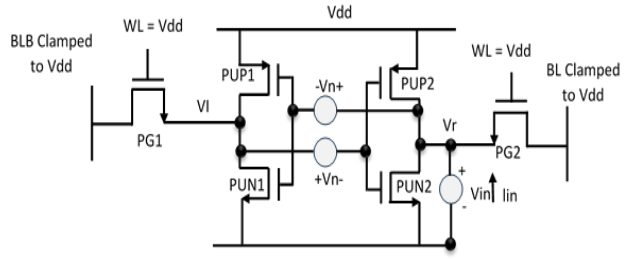


Fig. 6. CMOS SRAM cell

V. RESULTS AND DISCUSSION

This section discusses how circuit topologies affect the power loss of a single logic gate. An industrial method with a pitch of 0.35 μm is used for transistor modelling.

The importance of the two dynamical power elements is first investigated with regard to the CMOS inverter gate dimensions, the consequent loads, and the input slopes. Table 2 shows the variable power power for a minimal calibrated inverter for each cycle (that is, a high-to-low and a low-to-high transition), keeping the ratio Wp/Wn = 2 to create an asymmetrical gate.

	Energy (fJ)
Charge/Discharge	100
Short-Circuit	22

Table 2 Power Consumption of Subthreshold CMOS Inverter

Because smaller transistors require less resistance and a lower voltage supply, scaling reduces the amount of energy used. This result is a byproduct of efforts to keep chip energy density constant as technologies advance.

VI. CONCLUSION

There is a significant opportunity for lowering the power consumption of contemporary electronic devices, according to an analysis of power consumption in digital logic circuits operating at extremely low subthreshold power levels within static CMOS gates. Minimizing active and leakage currents is achieved by using the subthreshold region, where transistors function with gate-source voltages below their threshold values. Despite trade-offs including slower switching rates and increased sensitivity to process fluctuations, threshold operation in static CMOS gates is optimal for ultra-low power applications.

VII. FUTURE DIRECTIONS

1. Boost subthreshold circuit reliability in the face of temperature and process changes.
2. Create resilient design strategies to reduce performance trade-offs.
3. Investigate hybrid strategies that combine above- and below-threshold reasoning.
4. Look into new transistor topologies and materials to further cut subthreshold leakage currents.
5. Apply subthreshold logic to a wider range of applications, such as edge computing devices and artificial intelligence.
6. Subthreshold SRAM cell optimization is needed for greater density and quicker access times.
7. Cutting-edge methods and tools for precise modelling and simulation.
8. Next-generation wearables and IoT devices should have energy-efficient subthreshold circuitry.

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