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A DFT -Compatible Timing Error Detection and Correction Structure Featuring Low Area and Test Overhead

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ABSTRACT

As integrated circuits become more susceptible to process, voltage, and temperature variations, timing error resilience through EDAC structures is essential. However, conventional EDAC approaches often introduce design-for-testability (DFT) issues due to the presence of latch-based data paths and additional control logic. This paper proposes a DFT-compatible EDAC structure featuring a Scannable EDAC Cell (SEDC) that enables seamless integration of error detection in functional mode and efficient shift operations in scan mode. The architecture allows simplified control of detection logic and leverages global error propagation for straightforward observation. A shift-based testing methodology is further presented, minimizing test-pattern complexity and test time while preserving high fault coverage and low area overhead.

KEY WORDS: DEF-compatible, EDAC (Error Detection and Correction), SEDC (Scannable EDAC Cell), Scan mode, Fault coverage, Low area overhead, Shift-based testing, Global error propagation, Test pattern complexity, Functional and test modes

I. INTRODUCTION

An adder is a fundamental digital circuit used to perform arithmetic addition, forming the backbone of the Arithmetic Logic Unit (ALU) in processors. It plays a crucial role in systems like Digital Signal Processors (DSPs), Application-Specific Integrated Circuits (ASICs), and microprocessors. However, adders are vulnerable to faults—categorized as permanent, transient, or intermittent—caused by factors like electromagnetic interference, cosmic rays, and power supply noise. Transient faults are particularly challenging to isolate, often requiring the replacement of the entire adder. Since perfect systems are impractical, fault tolerance becomes essential. A fault-tolerant system continues to function correctly even when faults occur, making it indispensable for high-performance, safety-critical, and mission-critical applications. Traditional fault-tolerant designs rely on redundancy, which increases system complexity and cost.

To address these challenges, a novel self-checking and self-repairing fault-tolerant full adder is proposed. This design can detect and correct both single and double faults, including transient and permanent errors, with minimal area overhead. Unlike conventional redundancy-based methods that struggle to locate faults, the proposed adder efficiently identifies and repairs errors without excessive transistor count. It integrates fault detection and correction mechanisms that enhance reliability while maintaining compactness and speed. The design achieves faster addition operations and superior fault coverage compared to existing solutions, making it a promising approach for robust and efficient digital systems.

II. LITERATURE REVIEW

1.Design And Analysis of Low-Power 10-Transistor Full Adders Using Novel Xor -Xnor Gates: Introduces 41 novel 10-transistor full adder designs using XOR-XNOR gates, optimized for low power and high speed. Simulations show up to 10% power savings over conventional designs, though pass transistor threshold loss remains a limitation.

2. **Analysis of Various Full-Adder Circuits In Cadence:** Analyzes and compares various 1-bit full adder designs ranging from 6 to 28 transistors using Cadence Virtuoso with the 45nm GPDK kit. It evaluates each design based on power, speed, and area to identify the most efficient configurations.

3. Gdi based full address for energy efficient arithmetic applications: Three low-power full adder designs using full swing AND, OR, and XOR gates to overcome threshold voltage issues in GDI logic. These designs eliminate the need for extra inverters and show improved performance. SPICE simulations with 45nm models confirm lower energy consumption compared to CMOS, CPL, hybrid, and traditional GDI designs.

4. Repairing Adder Using Fault Localization: 16nm always-on DNN processor optimized for IoT workloads under tight energy constraints. It features adaptive clocking and multi-cycle SRAM reads for efficient voltage scaling and robust performance. The design achieves up to 1.36 GHz speed with ultra-low power consumption and top-tier computational efficiency.

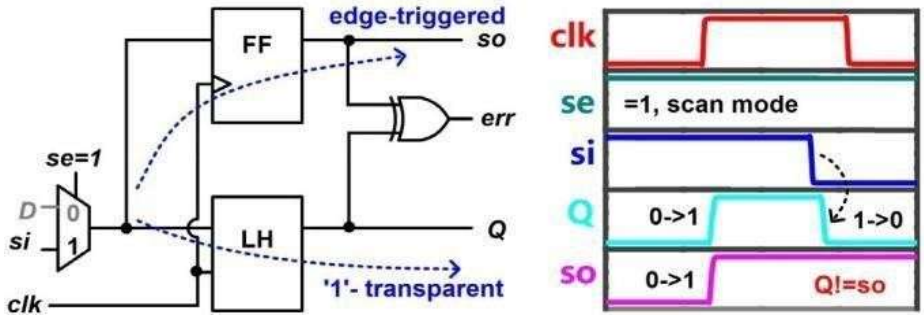
5. A Near-Threshold Spiking Neural Network Accelerator with A Body Swapping Based Detection and Correction Technique: This project introduces a novel in-situ error detection and correction method using fine-grained body-swapping, tailored for non-Von Neumann architectures operating at near/sub-threshold voltages. It eliminates the need for instruction replay and handles delay variability efficiently. The prototype achieves 49.3% better energy efficiency and 35.6% higher throughput with just 4.1% area overhead

6. PUSH PULL: SHORT-PATH PADDING FOR TIMING ERROR RESILIENT CIRCUITS: The severe short-path padding issue in resilient IC designs used for timing error detection and correction. Unlike prior local heuristic methods, it uses a global optimization approach with spare cells and dummy metal to implement effective padding. Experimental results confirm the method's effectiveness in validating error-resilient circuits.

7. THE UNDER VOLT: ENABLING AGGRESSIVE VOLTAGE UNDER- SCALING AND TIMING ERROR RESILIENCE FOR ENERGY EFFICIENT DEEP LEARNING ACCELERATORS: A fault injection framework for analyzing reliability in systolic array-based CNN accelerators used in safety-critical applications. It identifies vulnerabilities like bit flips and stuck-at faults across model layers and storage. Using saca-FI, the study evaluates network resilience and proposes two energy-efficient error protection strategies.

III. WORKING PRINCIPLE

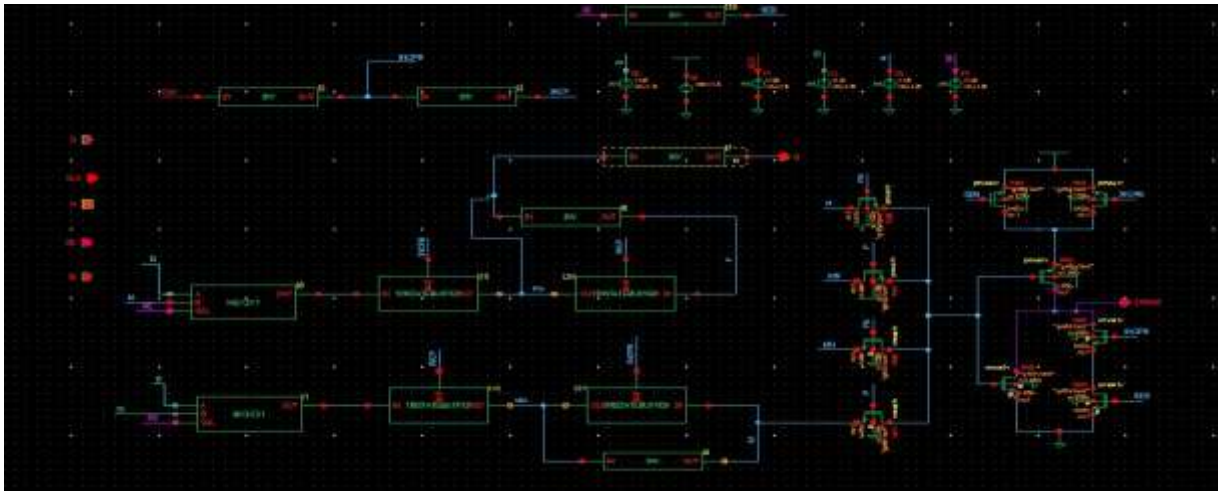
The EDAC (Error Detection and Correction) structure enhances timing-error resilience by enabling in-situ detection of timing violations, thereby reducing the need for pessimistic timing guard bands. In a resilient processor, the first five pipeline stages—IF, DE, RA, EX, and MEM—were protected by replacing 12% of flip-flops at critical path endpoints with EDAC cells. These cells use XOR-based detection logic to flag late-arriving data, aided by positive latches that offer metastability immunity and time-borrowing capability. Local error signals from each EDAC cell are aggregated via an OR-tree to produce stage-specific error signals, which are pipelined to an error control unit. The adaptive clock controller then adjusts the operating frequency to correct timing errors. Since process, voltage, and temperature (PVT) variations occur infrequently, the energy savings from reduced guard bands outweigh the overhead introduced by EDAC, resulting in a more efficient performance-energy trade-off.

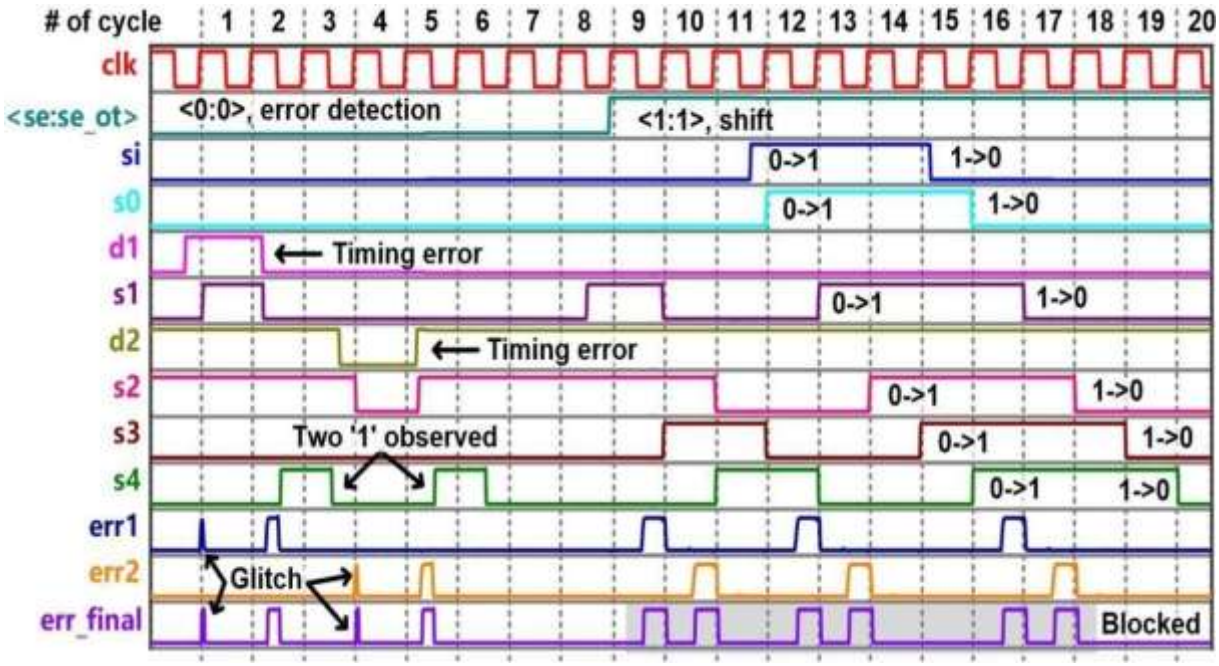


. Fig: Illustration of inconsistency between so and Q in SSFF in a scan shift operation

Error Detection and Correction in Normal Mode:

To monitor the timing errors during the normal mode, *se* and *se_ot* are both settled at "0." Therefore, SEDC1 and SEDC2 monitor the suspicious endpoints and correct the late input transitions with the time-borrowing ability in the high clock phases. Errors, if flagged, would be propagated through the OR tree and captured by the final FF at the negative clock edge to activate the succeeding schemes. As shown in Figure, the SEDCs work in error detection mode from cycle1 to cycle. The data input of SEDC1, $d1$, arrives later than the positive clock edge at cycle 2, then $err1$ flags and be collected as *err_final,* which is finally sampled to $s4$ at the negative edge of cycle 2. A similar process happens on SEDC2 at cycle 5. During unviolated data transitions, glitches exist in error signals at the positive clock edge as discussed but the glitch on *err final* is filtered by the final FF which is triggered by the negative clock edge. In all, two "1" are observed at $s4$ in the normal mode, indicating timing error happens twice in the monitored logic



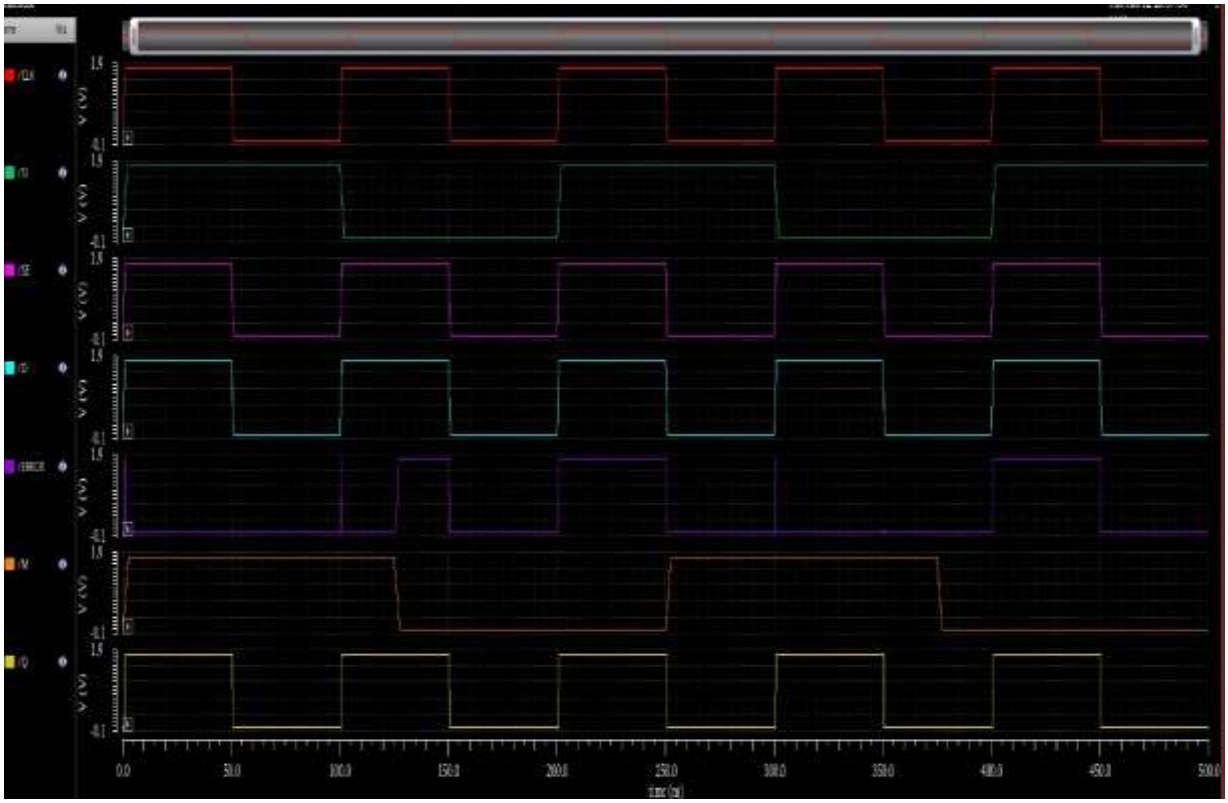


Shift Operation in Scan Mode:

To shift in or out the patterns via the scan chain during the test, *se* and *se_ot* are both settled to "1." SEDC1 and SEDC2 work as conventional FFs, sensitized by the positive edge of *clk* together with other FFs. The final FF takes in the $s3$, and is triggered by the positive edge of *clk* as well. In consequence, they

make up a 5-stage scan chain as noted with the shift path in Fig As shown in Fig the "0 − > 1" transition is assigned into the first stage at the beginning of shift in operation at cycle 12, then the transition propagates. to $s1$. SEDC1 and SEDC2 work as conventional FFs, shifting in or out the transitions. The final FF is also triggered by the positive clock edge. As a result, the "0 − > 1" transition is observed via $s4$ at cycle 16. Similarly, the "1>0" transition is also observed five cycles after it is injected at cycle 15. During the transition propagation, although $err1$ and $err2$ are flagged in order, the change on *err_final* is blocked by *se_ot* at the input of final FF. During the shift operation, if stuck-at faults happen in main or shadow lathes of SEDC cells, the transition pattern would be blocked from the final FF. Similarly, transition faults also lead to delayed sampling and wrong output serials under the specific shift frequencies. So, the fault coverage is not degraded by such SEDC cells

IV. RESULTS



V. CONCLUSION

Timing-error resilient circuit with EDAC structure is bur geoning for their timing-guard band mitigation and high energy efficiency. However, several challenges emerge in testing newly introduced logic efficiently, hinder the DFT implementation, and increase the test overhead. In this article, we propose a novel DFT-compatible EDAC structure which supports normal EDAC function, scan shift operation, and purposive timing error generation as well as observation for the test. Benefiting from the testability of hardware design, a set of the shift-based test method is also proposed to test the EDAC structure with low pattern complexity and test time overhead.

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