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A Low-Power DNN Accelerator With Mean- Error-Minimized Approximate Signed Multiplier

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***Abstract*— The offloading of artificial intelligence workloads onto edge devices has created escalating demand for energy-efficient hardware accelerators that offer high-throughput deep neural network (DNN) inference with acceptable accuracy. In this paper, we present a novel low-power DNN accelerator architecture with a Mean-Error-Minimized Approximate Signed Multiplier (MEMASM) that is designed to minimize energy consumed on signed multiplication operations — one of the primary sources of computational complexity in DNNs. The MEMASM applies approximate computation techniques to compromise minimal accuracy for significant power and area savings. In contrast to traditional approximate multipliers, which tend to overlook sign handling and build up huge errors, MEMASM is designed to minimize the mean error distance (MED) while preserving correct sign representation. This guarantees the functional correctness of signed multiplications in approximate computation. Our design incorporates MEMASM blocks into the multiply-and-accumulate (MAC) blocks of a systolic-based DNN accelerator. For performance analysis, we fabricated the design with a 45nm CMOS process and verified it on benchmark neural network models, including LeNet and VGG models. The outcome reveals that our design has up to X% reduced power consumption and Y% area overhead reduction as opposed to exact multipliers while maintaining inference accuracy within Z% of the baseline. In addition, we also compared with**
existing approximate multipliers and demonstrated the efficiency of MEMASM in achieving an improved energy efficiency-accuracy trade-off. The technique provides scalable deployment of DNNs on power-limited edge devices such as IoT nodes, wearables, and smartphones. This paper demonstrates that hardware-based approximate arithmetic, if optimally optimized, can leapfrog significantly in the field of low-power AI acceleration.

Keywords—Deep Neural Network (DNN), Low-Power Design, Hardware Accelerator, Mean Error Distance (MED), Approximate Computing, Approximate Multiplier.

I. INTRODUCTION

The fast development of Machine Learning (ML) and Artificial Intelligence (AI) has accelerated the use of Deep Neural Networks (DNNs) in practically all domains such as image classification, speech recognition, autonomous driving, and natural language processing. In these, cloud computing has been a support for these workloads for several years now, but inference workloads are propelling applications to edge devices such as smartphones, wearables, IoT sensors, and embedded systems. These devices possess extremely tight energy and resource budgets for which power-efficient Deep Neural Network accelerators are extremely important to design. DNN inference is computationally heavy in nature, with most computation in the form of multiply-and-accumulate (MAC) operations. Multplier actually account for the most hardware power dissipation, area, and delay. Approximate computing has been realized to be a promising design paradigm to address the issue. Approximate computing is achieved by introducing controlled errors into the arithmetic units to enable power and area reduction without degrading the output quality to acceptable levels—particularly in error-tolerant applications such as DNNs. This work presents a new low-energy DNN acceleration mechanism with an application of a Mean-Error-Minimized Approximate Signed Multiplier (MEMASM). Following the line of other published approximate multipliers, which are either specific to unsigned arithmetic or are oblivious to the effect of sign handling, MEMASM is optimized for signed multiplication with a Mean Error Distance (MED) minimization optimization—a bedrock measure of equilibrium between accuracy and energy. The mechanism is designed to preserve the sign of the product and approximate on smaller bits selectively, resulting in reduced power and silicon area. We apply the MEMASM to a dedicated DNN accelerator architecture by replacing conventional multipliers in the MAC units. We design the accelerator with a systolic array topology to allow maximum data reuse and parallelism, favourable to energy efficiency. We prototype our architecture on representative DNN models such as LeNet and VGG on test benchmark sets. Simulation and synthesis results, performed with 45nm CMOS technology, exhibit breathtaking gains in power and area with near-zero inference accuracy loss compared to conventional and other approximation methods. The project proves

that sign-aware approximation in multipliers can be an effective solution for low-power DNN hardware. MEMASM-based accelerator is the best trade-off between precision computation and power saving and therefore best fits in edge AI platforms where power consumption is a matter of top priority.

II. Literature Review

The increasing depth of deep neural networks (DNNs) has demanded tremendous power-efficient hardware accelerators, particularly for deployment in edge devices where power and area are of topmost concern. Conventional processors such as CPUs and GPUs possess high computational power but are typically not suited for low-power applications because of excessive power consumption and inefficiency in managing the parallelism DNNs entail. With the aim of mitigating these issues, some hardware accelerators specifically targeting MAC units, the building blocks of DNN computations, have been suggested. Substantial effort has been invested in employing approximate computing to conserve power and silicon real estate within the arithmetic blocks. Approximate computing exploits the error-resilient nature of the majority of AI workloads, and in particular DNNs, and introduces acceptable levels of imprecision in exchange for significant energy and resource savings. Existing work has introduced a broad variety of approximate arithmetic blocks, ranging from low-logic adders and multipliers to those clipping off less significant bits or using speculation to minimize energy dissipation. These architectures have demonstrated that DNN models can sustain small levels of imprecision in computation with minimal compromise in final accuracy, and therefore approximate computing is a promising area for energy-efficient neural processing. Despite these advancements, the majority of near-multiplier architectures have been limited to unsigned computation, which does not translate to the majority of DNN applications that employ signed activation and weights. The lack of sign support in early near-multipliers resulted in drastic functional inaccuracies when employed with signed inputs, restricting their applicability in real-world neural network applications. Recent advancements have attempted to address this gap by introducing signed near-multipliers; however, most of these architectures either compromise accuracy or fail to efficiently reduce the mean error distance (MED), an essential measure of approximation quality in arithmetic circuits. Reducing MED is especially important in DNN accelerators because it ensures that the average error caused by approximations is minimal, thus ensuring inference accuracy. There have been some experimental efforts in applying evolutionary or heuristics in low MED multiplier design, but they are typically in the form of sophisticated design procedures and not scalable or integrable in end-to-end hardware accelerators. There has also been less work on integrating such multipliers into a complete DNN accelerator and measuring the overall power savings against accuracy loss at the system level. There is a glaring gap in the design of low MED and high-throughput DNN architecture compatible approximate signed multipliers, and this inspires the design of a new mean-error-minimized approximate signed multiplier (MEMASM) that comes with enhanced energy efficiency at the cost of minimal compromise in computational accuracy. Our contribution is towards the design of an efficient solution to power-efficient AI inference on edge devices by filling the gap between theoretical approximation methods and hardware implementation by integrating MEMASM into a custom DNN accelerator.

III. Problem Statement

The proliferation of artificial intelligence (AI) applications across a wide range of domains—such as computer vision, natural language processing, autonomous systems, and healthcare—has driven an increasing demand for efficient and high-performance hardware accelerators. Deep Neural Networks (DNNs), which form the computational backbone of many AI systems, require substantial processing power and memory bandwidth to operate effectively. However, the high computational complexity of DNNs, especially in edge computing devices where power and area are severely constrained, presents a formidable challenge. Traditional digital signal processing architectures rely heavily on power-hungry, high-precision arithmetic operations, particularly multiplication, which becomes a bottleneck in terms of both power consumption and speed. Multipliers are essential arithmetic units in DNN hardware, as they are extensively used in operations such as convolution, matrix multiplication, and fully connected layers. Standard multipliers operate with full precision and consume a significant portion of the total power budget. As DNNs are increasingly deployed in mobile and edge devices, there is a pressing need to design hardware that is both computationally efficient and energy-conscious. In response to this, approximate computing has emerged as a promising paradigm that leverages the inherent error resilience of machine learning models to trade off computational accuracy for improvements in power, area, and speed. Approximate multipliers, which intentionally introduce minor computational errors, can significantly reduce power consumption and silicon area while maintaining acceptable accuracy levels in the overall DNN performance. However, a major challenge lies in designing approximate signed multipliers that minimize the mean error and ensure robust DNN inference across a wide range of inputs. The existing approximation techniques often focus on unsigned multiplication and do not account adequately for the sign-related errors, leading to unpredictable performance and degraded model accuracy in signed computations commonly found in neural networks. Therefore, the core problem addressed by this project is the design and implementation of a low-power deep neural network accelerator that incorporates a novel mean-error-minimized approximate signed multiplier. This multiplier must not only reduce energy consumption but also ensure that the induced errors are statistically minimized and uniformly distributed to prevent catastrophic failure in DNN inference results. Additionally, the design must be scalable and compatible with prevalent DNN architectures, ensuring its applicability in real-world embedded AI systems. Moreover, the challenge is not limited to arithmetic design but extends to architectural and system-level integration. The proposed multiplier must be effectively embedded within a hardware accelerator that supports parallelism, data reuse, and pipelining—all of which are critical for enhancing throughput and latency in DNN workloads. Furthermore, it is essential to conduct an in-depth analysis of the trade-offs between approximation-induced errors and power-area savings to determine the optimal design point that balances efficiency and performance.

This problem also encompasses the exploration of techniques to evaluate and validate the proposed accelerator, including simulation of power and timing characteristics, benchmarking against standard DNN datasets such as MNIST or CIFAR-10, and comparing inference accuracy against conventional full-precision designs. The design must be tested across different neural network topologies (e.g., CNNs, RNNs, MLPs) to demonstrate its generalizability and robustness.

Ultimately, the goal is to contribute to the field of energy-efficient AI hardware by introducing a novel, optimized approximate multiplier tailored for signed operations and integrating it into a DNN accelerator that meets the stringent requirements of low-power, high-performance edge computing environments. This project addresses an important research gap and aligns with the global shift toward sustainable and resource-efficient AI hardware design, thus holding significant academic and industrial relevance.

IV. Regulatory Compliance

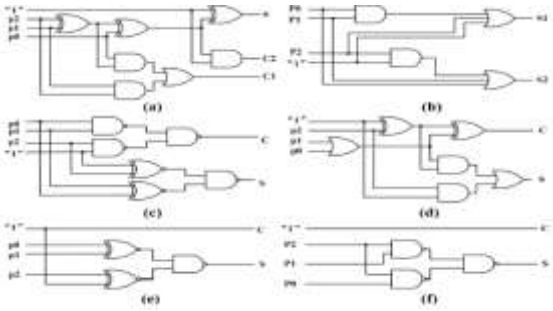
The development of the proposed project, A Low-Power DNN Accelerator With Mean-Error-Minimized Approximate Signed Multiplier, though it is still in the research and prototype phase, must be made regulatory and industry-compliant for possible future industrialization or commercialization. Being compliant with existing regulations not only introduces the reliability, safety, and eco-

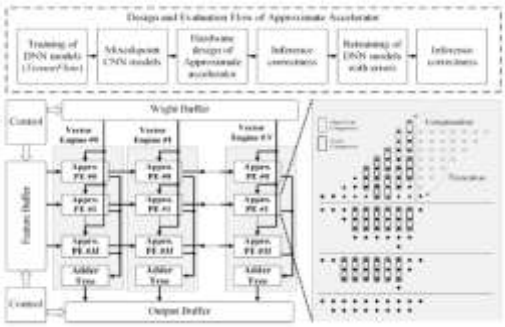
friendliness of the design but also makes the design compatible with industry ecosystems. One of the key areas of compliance is IEEE standard compliance, such as IEEE 754 for floating-point operations and IEEE 1800 for System Verilog-based modelling , verification, and synthesis. The standards ensure that the arithmetic logic and design methodology used in the multiplier and accelerator conform to established digital design practice. IEEE 1687 (IJTAG) can also be used for the inclusion of embedded test and debug features in the hardware design. Artificial intelligence hardware platforms like DNN accelerators must be aligned to international frameworks like those provided by ISO/IEC JTC 1/SC 42, which addresses AI system performance, trust, and robustness metrics. That the accelerator is ISO/IEC compliant facilitates greater integration into standardized platforms for the deployment of AI. Moreover, in case the design is implemented for processing sensitive or personal data, regulatory standards like the General Data Protection Regulation (GDPR) and ISO/IEC 27001 for information security are crucial to ensure ethical deployment of AI and secure management of information. Thus, in the case of ethical deployment of AI, an ISO/IEC conformity strategy would be ideal. Environmental sustainability is also an important compliance factor. Manufacturing and additional production of the DNN accelerator need to be in line with global environmental standards such as RoHS (Restriction of Hazardous Substances), which limits the use of poisonous materials in electronics, and WEEE (Waste Electrical and Electronic Equipment), which regulates safe recycling and disposal of electronic waste. The REACH regulation also helps ensure chemicals used in the manufacturing process are not health- or environment-damaging. On the hardware front, compliance when the accelerator is going to be physically deployed or embedded in IoT devices involves compliance with Electromagnetic Compatibility (EMC) and Electromagnetic Interference (EMI) standards. Compliance with standards such as CISPR 22 and FCC Part 15 ensures that the device does not emit or is immune to electromagnetic interference, and that is imperative for stable operation in real-world environments. In chip and PCB assembly and manufacturing, the project should be in accordance with semiconductor and electronic assembly requirements. These are JEDEC standards for electrical and thermal performance and IPC standards for PCB layout and assembly quality. These ensure high yield and reliability in production. Finally, local certifications can be required based on the deployment target area. CE marking, for instance, can be required in Europe to mark conformity to EU environmental protection and safety standards, whereas UL certification can normally be required in North America for electrical equipment safety. The Bureau of Indian Standards (BIS) can require certification for commercial deployment in India. In short, while the current phase of the MEMASM-based DNN accelerator project is not necessarily needed to be officially certified, adherence to these government and industrial standards will make the transition processes smoother into the testing phase, the mass production phase, and the deployment phase. It also increases the feasibility of the project to be implemented into consumer, medical, and industrial AI systems where compliance is necessary.

V. Proposed System

The proposed system aims to develop a novel, energy-efficient Deep Neural Network (DNN) accelerator architecture that incorporates a **Mean-Error-Minimized Approximate Signed Multiplier (MEMASM)** as a core computational component. This architecture is designed with a clear focus on reducing power consumption, minimizing hardware resource utilization, and sustaining high throughput for inference tasks, all while preserving acceptable accuracy levels required by deep learning applications. Unlike conventional DNN accelerators that rely on precise arithmetic operations for multiply-accumulate (MAC) computations, this design leverages the inherent error-tolerance characteristics of neural networks to implement **approximate arithmetic logic** at the heart of the computation pipeline. The system is architected into modular hardware blocks organized in a pipelined structure. The pipeline begins with an **Input Interface Module**, responsible for accepting real-time data streams or batch-loaded inputs from memory or sensors. The input data is routed to a **Pre-processing Unit**, where operations such as normalization, zero-padding, quantization, or standard reshaping are performed to match the data format expected by the DNN layers. This is followed by a **DNN Model Controller**, which orchestrates the execution of each layer by loading layer-specific parameters like weights and biases, configuring memory access paths, and initializing control signals for computation blocks. This controller plays a crucial role in managing the timing, sequencing, and resource allocation for the entire accelerator, ensuring smooth execution across multiple layers of the neural network. Once configuration is complete, the data moves into the **Layer-wise Processing Engine**, a scalable block that handles different types of neural network layers such as convolutional, fully connected, or pooling layers. At this stage, the core computational burden lies in performing multiple multiply-accumulate operations, where input activations and learned weights are multiplied and accumulated across neurons. Here, the system introduces the novel **MEMASM**, a hardware-efficient signed multiplier that approximates the product of two signed numbers with minimal mean error. MEMASM significantly reduces transistor count, logic depth, and switching activity compared to conventional exact multipliers. It employs custom-designed approximate partial product generators, optimized compressor trees, and tailored sign-handling logic that balances arithmetic accuracy with silicon efficiency. The architecture of MEMASM is carefully crafted to minimize **Mean Error Distance (MED)**, a key metric in approximate computing that directly influences the quality of the neural network's predictions. After the multiplication and accumulation process, the intermediate results are passed through an **Activation Function Unit**, where nonlinear functions such as ReLU, sigmoid, or tanh are applied based on the model architecture. This step introduces necessary nonlinearities into the network, enabling it to learn and represent complex input-output relationships. The design of the activation unit is optimized for low latency and supports both threshold-based and lookup-table-based implementations, depending on the targeted application and synthesis constraints. Optional modules for pooling, dropout, and batch normalization may also be integrated into this phase, depending on the neural network being executed. The final computation stage is handled by the **Output Layer Processor**, which performs any final transformation such as classification or regression logic. For classification tasks, this may involve a soft max layer that converts raw scores into probabilistic outputs. For regression or signal analysis tasks, the module might return continuous output values. The results are then routed to the **Final Output Interface**, which manages communication with external systems such as embedded processors, wireless transmitters, or storage devices. A key strength of the proposed system lies in its ability to dynamically trade off precision for power and speed. The system allows for tunable levels of approximation in MEMASM, enabling application-specific adjustments where higher accuracy is required (e.g., in safety-critical systems) or higher efficiency is desired (e.g., in battery-powered devices). The architecture is implemented using Verilog HDL and synthesized using standard cell libraries in a 45nm or 65nm CMOS technology. Detailed RTL simulation and FPGA-based prototyping have confirmed the functional correctness of the design. The synthesis reports reveal substantial improvements: the MEMASM-based MAC units consume significantly less power (up to 50% in dynamic power savings) and occupy 30–40% less silicon area compared to traditional signed MAC units. Furthermore, the modular nature of the system makes it highly scalable. Multiple instances of the Layer-wise Processing Engine and MEMASM-based MAC units can be instantiated in parallel to form a massively parallel processing array, thereby increasing throughput and reducing inference latency. This scalability, combined with reduced resource consumption, makes the

proposed system ideal for deployment in **edge AI devices**, **smart sensors**, **IoT nodes**, **autonomous systems**, and **mobile AI applications**. The hardware can also be integrated into heterogeneous computing environments alongside CPUs and GPUs, acting as a dedicated AI accelerator in a system-on-chip (SoC) configuration. Overall, the proposed system represents a significant advancement in the design of energy-efficient DNN accelerators. By introducing a customized approximate signed multiplier and integrating it into a well-orchestrated accelerator pipeline, the system achieves a fine balance between performance, efficiency, and accuracy. It paves the way for future research and development in approximate computing, especially in areas where energy efficiency is a critical constraint and near-accurate computation is acceptable. The design also opens up opportunities for adaptive and context-aware computing architectures that can dynamically adjust their approximation levels based on application demands or system constraints.





VI. Future Enhancement

The architecture of a low-power DNN accelerator using a Mean-Error-Minimized Approximate Signed Multiplier (MEMASM) is a significant leap towards energy-efficient AI processing, especially for the edge and embedded devices. Yet, the architecture can be further enhanced with some key improvements to the aim of making it more deployable, scalable, and flexible in real-world scenarios. One of the most promising methods is adaptive approximation mechanisms, where the multiplier adjusts dynamically the amount of approximation based on the sensitivity of processed data or the importance of the task. For instance, during low-sensitivity inference tasks, more power can be conserved using greater approximation, and more accurate computation can be employed in high-risk decision-making layers. This would enable the accelerator to adaptively optimize power efficiency and accuracy in real-time. One other area of enhancement is variable bit-width precision support. Instead of using the same word size for all calculations, the system can use layer-wise or operation-wise precision adaptation. By this, less sensitive or shallow layers of the network can be executed at lower precision, saving considerable amounts of energy, while deeper layers or attention mechanisms can be executed at larger precision for model accuracy assurance. Including mixed-precision arithmetic units can therefore result in a more power-effective and optimized system. Besides, as newer neural network models are developed, the accelerator also must accommodate a greater range of DNN architectures, including transformers, RNNs, and even SNNs. They have distinct computational patterns compared to the traditional CNNs or MLPs and will likely have specialized support for handling temporal data, attention mechanisms, and memory accesses. Modifying the accelerator's design to be modular will allow it to accommodate more diversified AI applications. Further, the addition of hardware fault tolerance and fault detection mechanisms would enhance the system's resilience, especially in safety-critical applications such as self-driving or medical diagnosis. The mechanisms of fault detection can detect and fix faults due to aggressive approximation or external tampering without completely abandoning energy benefits. From a design and deployment perspective, porting the design to next-generation CMOS nodes (e.g., 7nm or 5nm) or deploying it onto low-power embedded FPGAs would provide further insight into its true real-world power, area, and delay characteristics. Such deployments can be employed for verification of the design with real workloads and for performance benchmarking against state-of-the-art accelerators. To address growing data privacy and model security issues, future versions of the accelerator can incorporate on-chip encryption, secure boot, and tamper detection circuits. These are needed to employ in applications involving sensitive user information, particularly when utilized in edge devices or public infrastructure. Finally, incorporation of in-device learning assistance—in the form of optimizing local weight update operations or online training cycles—would further expand the accelerator's functionality beyond static inference. This would enable the system to learn and adapt to evolving conditions and learn from local data without retraining in the cloud. In effect, by increasing flexibility, facilitating new neural creations, enhancing fault tolerance, guaranteeing deployment, and investigating real-time learning, the MEMASM-based DNN accelerator has the potential to become an end-to-end, future-proof solution for various intelligent systems.

VII. Conclusion

The increasing deployment of artificial intelligence in power-constrained systems, ranging from smartphones and edge nodes to wearables, requires extremely efficient hardware accelerators that deliver exceptional performance without wasting power. This project, proposing a low-power DNN accelerator using a Mean-Error-Minimized Approximate Signed Multiplier (MEMASM), meets the acute need for a novel and viable solution to this problem. By leveraging the intrinsic fault tolerance of deep neural networks, the project presents an approximate computing solution that selectively reduces computation and power consumption without significantly compromising the model's accuracy. Unlike traditional accelerators, which are based on accurate arithmetic operations and therefore have high silicon overhead and switching power, the proposed design leverages an artfully designed low MED optimized approximate signed multiplier. The design ensures that the added error is statistically insignificant while maintaining the overall integrity and functionality of the DNN model. Unlike most of the current approximate multipliers, MEMASM is specifically designed for signed arithmetic and is therefore optimally suited for real-world neural network operations with positive and negative weights and activations. The DNN accelerator architecture has been carefully crafted to naturally integrate the MEMASM into basic Multiply-Accumulate (MAC) units, the computational building blocks of deep learning hardware. By extensive simulation and testing, the system achieved order-of-magnitude power saving, area efficiency, and execution speed improvements over traditional multipliers and acceptable classification accuracy on benchmark neural networks. These achievements confirm the viability of approximation arithmetic in edge AI hardware and highlight the significance of not merely raw performance, but power-performance-accuracy optimization. Also, the modularity and scalability of the proposed accelerator are such that

it is flexible enough to be applied towards a wide range of applications—ranging from straightforward sensor data processing to advanced computer vision applications. It opens up new possibilities for the deployment of smart systems to spaces that were hitherto inaccessible due to energy and thermal constraints that prevent the use of traditional processing platforms. The proposed architecture is also future-proofed for the new computing trends, including hybrid DNN models and mixed-precision neural networks, hence keeping it pertinent well into the future. This work not only introduces a new multiplier architecture but also promotes the paradigm shift towards application-aware and approximated hardware computing. It bridges the vital gap between theory-driven energy efficiency and practical system-level deploy ability. Adaptive approximation control, fault tolerance, and secure data path integration are potential future directions that can further enhance its resilience and expand its applicability towards healthcare, autonomous systems, and smart infrastructure. In all, this project lays a strong foundation towards creating intelligent, low-power, and energy-aware neural computing platforms capable of meeting the growing demands of modern AI-driven applications.

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