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A Novel Isolated AC to DC Power Factor Corrector Rectifier with Higher Switching Frequency

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***Abstract* - The primary aim of this research paper is to design a novel low-cost ac-dc power rectifier for improving power factor and total harmonic distortion with higher switching frequency topology using fewer switches on its secondary side. This modified topology converts ac to dc power maintaining the criteria of international power conversion standards. Due to high currents on the low-voltage side and expensive prices, conventional rectifiers have considerable conduction losses, especially when multiple active devices are used in any form either in series, parallel or in combination to attain high voltage and high power levels. The suggested methodology substitutes traditional three-level converters on the secondary side with only two switches and four diodes while retaining its core converter operation. The simulation is performed in the MATLAB2019b environment**.

Keywords- Isolated AC-DC rectifier, lossless switching, ZVS and ZCS, solid-state transformer converter.

I. Introduction

Through standalone ac-dc unidirectional power converters, distribution-level ac currents and voltages are typically configured to serve dc loads such as electric-vehicle battery charger systems [1], [2], hybrid ac-dc wind farms [3], communications systems [4], dc-powered data centers, and UPS. When power must flow in both directions, such as between an electric vehicle (EV) charger and the grid, a bidirectional converter comes in handy [5]. Recent advances in the 10 kV SiC-MOSFET enable a dependable two-stage solid-state transformer (SST) design for converting medium ac voltage to low dc voltage to power dc loads [6]. Many standalone ac-dc SST converter topologies use 10 kV SiC-MOSFETs and demonstrate great efficiency while converting from a 7 kV ac-line to a 400 V dc-bus [7]. In hybrid micro grids, dual power converters that work in a single direction, as well as bidirectional, are commonly utilized to support as well as provide sustainable power management solutions [8].

The number of tumbled cells grows as the power level rises, forming a multilayer voltage appropriate for the rating of the device [9]. For standalone ac-dc power converters, input power factor correction (PFC), low total harmonic distortion (THD), and output voltage regulation are typically the minimal standard [4]. The international standard IEC 61000-3-2:2018 [10] specifies that the harmonic content of the input current is restricted to prescribed values, which are usually met by using these PFC techniques [11].

A balanced voltage distribution throughout the semiconductor devices on the high-voltage side, as well as current sharing between devices on the low-voltage side, are desirable properties for this type of converter to limit power conduction losses and improve the rating of the current and rating of the voltage [12]. However, maintaining high levels of efficient power density while meeting the above-mentioned parameters remains a major issue for scientists [12].

The single-phase, single-stage, bidirectional doubly active bridge converter is one of the most widely used solid-state insulated AC-DC converters. The use of a synchronous rectifier (SR) at the front side has the advantage of shaping the AC to be near to a sinusoidal waveform and in phase with the input voltage, which increases the power factor (PF) and lowers the THD level. In addition, the primary and secondary bridges produce three voltages, namely +v, 0, and –v, which allow complete control of the dc-bus voltage, output power, and output voltage. The use of twelve switching devices with full dc-bus voltage rating (high cost) and tackling the problem of power back-flow are the disadvantages of using this converter, specifically whenever power is streaming in one direction [13].

A three-level single directional insulated single-stage PFC converter with minimal switches, as shown in [15], is also another cost-effective configuration. A three-level neutral point clamping (NPC) converter is connected to a boost inductor and a full-wave diode bridge rectifier on the primary side, while a half-bridge diode rectifier and output inductor are coupled to the secondary side. Implementing this topology following are the major benefits: (i) a limited number of devices; (ii) a high PF when the dc bus voltage is substantially greater than the maximum input voltage; and (iii) switching devices that can endure half of the dc-bus voltage. Moreover, because switching devices are only on the primary side, it is not necessary to alter the dc-bus and output voltages at the same time. Thus, under low-load situations, the dc-bus voltage rises to the stage where switches are subjected to high voltage strains.

[15] Proposes a boost-based topology that regulates both the dc-bus and output voltage levels. To minimize current stress on the secondary side switching devices, the secondary side is made up of two H-bridges coupled to two transformer secondary windings. This design is not suitable for large output voltage purposes since it necessitates the use of eight switching devices to maintain the full output voltage. Furthermore, low-power operation causes secondary side switching devices to suffer soft-switching.

In this paper, we introduce a novel configuration (shown in Fig. 1) that addresses the problems described above while maintaining the fundamental operating principle of three-level insulated ac-dc converters, such as output voltage regulation and dc-bus voltage control in only expected standards defined by the necessity of the load. The current via the boost inductor is discontinuous, allowing for a large PF because the dc-bus voltage is kept at an appropriate level.

The novel secondary side circuit, which has only two switching devices and four diodes, is the suggested topology's most significant addition. In contrast to [15], the secondary side bridge performs at ZVS and ZCS at turn ON in all states of operation and power levels, whereas lossless switching is only assured at a specified region defined by the power level in another state. Furthermore, the primary and secondary switching devices on the primary and secondary sides only support 50% of the dc-bus voltage and 50% of the output voltage, respectively. In [15], on the other hand, the voltage rating of the eight switching devices at the secondary side is analogous to the whole output voltage level. Besides that, power is supplied from the secondary terminals to the load via only one device throughout a half switching period. In a traditional H-bridge, however, the current is circulated across two switching devices.

In this paper, Section II describes the novel topology, along with the circuit layout, steady-state waveforms, and working mechanism. Section III explains the lossless switching study about the suggested topology. The converter's design methodology is detailed in Section IV. In Section V, the conclusion of this research paper is explained.

II. SUGGESTED TOPOLOGY OF AC-DC POWER CONVERTER

In [15], the suggested ac-dc technique utilizes a boost-based forepart diode-rectifier, which eliminates the need for an active rectifier but sacrifices bidirectional power conversion capacity. The high-frequency transformer and the dc-link capacitors are then connected to neutral point clamping. The neutral point clamping serves two purposes: first, it serves as the active switch for the boost-based forepart rectifier. The second purpose of neutral point clamping is the primary-side bridge of a dual active bridge-type configuration made up of the NPC, a novel secondary-side active bridge with the least switching devices possible, and the high-frequency transformer.

A novel secondary side bridge configuration is discussed in the following section.

A. *Circuit layout*

The voltage rating of the two switches in the novel secondary side network is half of the level of the output voltage, as shown in Fig. 1. The lossless switching section will go over the soft transitions between modes in great depth. The boost inductor is coupled to a half-bridge diode rectifier at the front end. To enable the charging and discharging of the stray capacitances, the flying capacitor C_{fc} is positioned in parallel to the two switches (S_{O5}, S_{O6}). Because the primary-side network has previously been described in prior work [15], the examination of the proposed scheme will move on to a novel secondary side network throughout the paper.

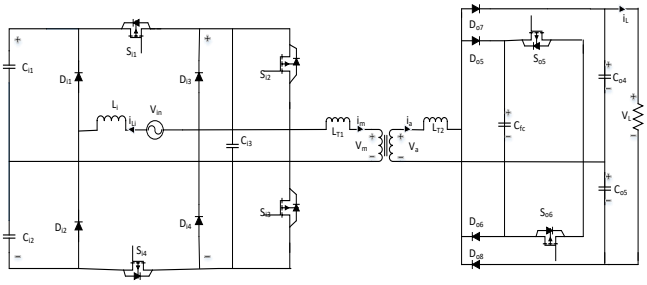


Fig. 1. Basic circuit of an isolated ac-dc converter

B. *Waveforms in a Stable State*

The stable state modulation scheme of the suggested configuration is illustrated by the theoretical waveforms in Fig. 2. Only the primary waveforms for the upper side (V_{So5}, V_{Do7}, I_{So5}, and I_{Do7}) are shown due to the similarity between the upper and lower halves of the suggested secondary side. As illustrated in Fig. 2, the primary and secondary capacitors' voltages (C_{i1}, C_{i2}, C_{o4}, C_{o5}) are represented in the primary and secondary voltages (V_m, V_a) waveforms.

When the secondary current leaves the positive terminal of the high-frequency transformer (HFT), it passes via S_{o5} and D_{o5}, or it passes through D_{o7} to charge C_{o4}, before returning to the negative terminal of the HFT. When S_{o5} switches on during the positive half cycle of the secondary current, diode D_{o7} allows the current to charge C_{o4} while also preventing C_{o4} from short-circuiting its terminals.

When the output voltage is higher than the required value, switch S_{o5} (S_{o6}) is positioned across the HFT terminals to flow the current. When S_{o5} (S_{o6}) is turned off, the voltage across it rises until it exceeds the output capacitor voltage C_{o4} (C_{o5}), which causes the diode D_{o7} (D_{o8}) to be forward-biased. When utilizing a bidirectional current semiconductor device (e.g., Si or SiC MOSFETs), a diode D_{o5} (D_{o6}) must be arranged in series with the switch S_{o5} (S_{o6}) to prevent any negative (positive) current from flowing back to the high-frequency transformer positive (negative) terminal. At ZVS and ZCS, switch S_{o5} can be switched ON during the negative cycle of the secondary current. Furthermore, as illustrated in Fig. 2, at ZVS and ZCS switches S_{o6} can be activated during the positive cycle of the secondary current. The primary dc-bus voltage is controlled by the primary duty cycle Dm. The output voltage and supplied power are controlled by the secondary duty cycle D_a and the phase shift between primary and secondary voltages D_{ph}. The basic phase shift that depends on the primary and secondary voltages and duty cycles is known as the high-frequency transformer turns ratio, which is denoted by the letters k and ph.

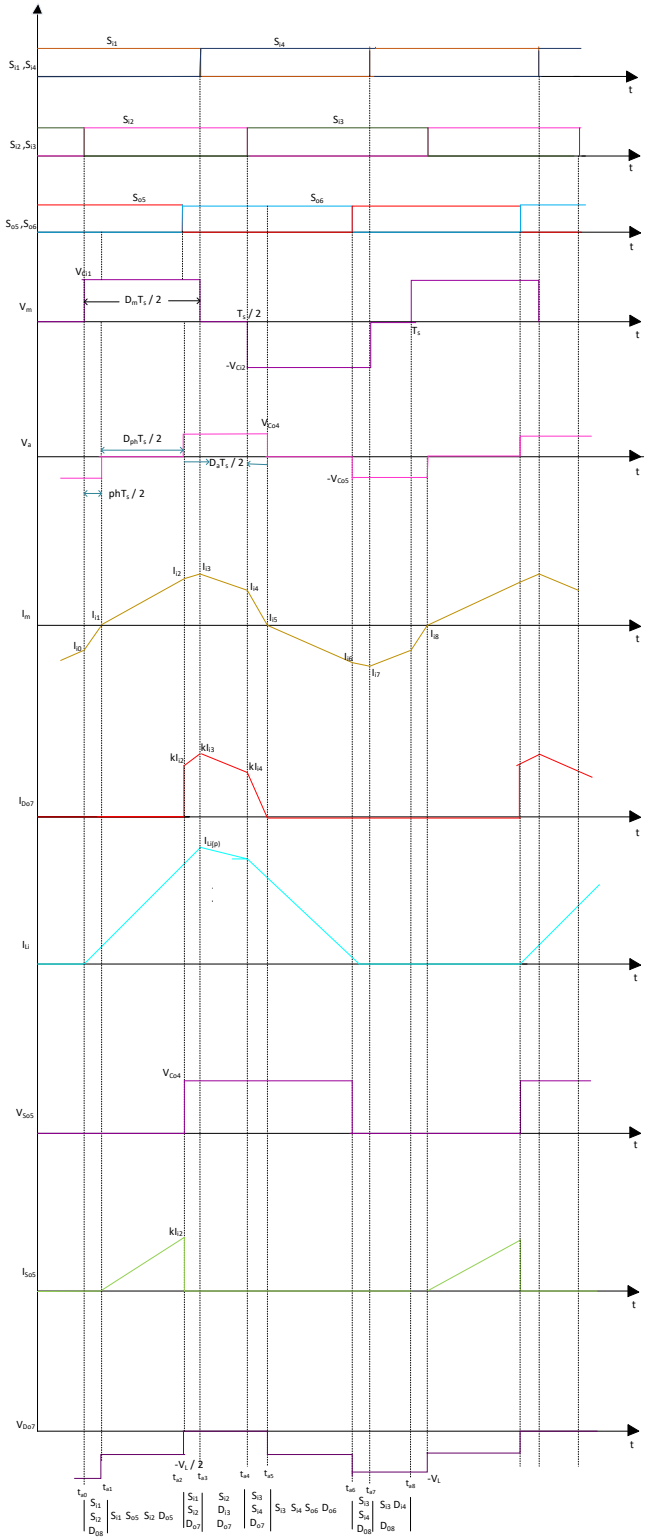


Fig. 2. Waveforms in a stable state (steady-state)

C. *Working principles*

The analogous circuit for each period is shown in Figure 3. The brown arrows indicate the HFT's primary and secondary currents, while the blue arrows indicate the input current i_i, which is the same as the boost inductor current i_{Li}.

i. Period a) [$t_a - t_b$]: Initially, the current at the primary i_m is negative and flows through the diodes which are antiparallel to each other of switches S_{i1} and S_{i2}. As indicated in Fig. 3(a),

The secondary current flows through capacitor C_{o5} and diode D_{o8}. The voltage of capacitor C_{i1} is equal to the voltage at the primary v_m, meanwhile the voltage of capacitor $C_{o5} = -V_L/2$ is equal to the voltage at the secondary v_a. The slope of the primary current is positive and grows continuously at the rate of $(V_{Co1} + kV_L/2)/L_{T1}$. When switches S_{i1} and S_{i2} are turned on, the boost inductor begins to charge at a rate of $v_{in}(t)/L_i$. This stage has the time duration of $(D_{ph} + D_a - 1)T_s/2$, and the primary current of high-frequency transformer i_m is given as:

$$i_m(t) = \frac{1}{L_{T1}}(V_{Ci1} + \frac{kV_L}{2})(t - t_a) + I_L \qquad (1)$$

The current at the primary i_m becomes zero at the end of this period. As a result, the starting state I_L of the primary current i_m is calculated as:

$$I_L = -\frac{1}{2 f_s L_{T1}}(\frac{kV_L}{2} + V_{Ci1})(D_{ph} + D_a - 1) \qquad (2)$$

ii. Period b) [$t_b - t_c$]: The current at the primary i_m, turns positive and passes via S_{i1} and S_{i2}. The current at the secondary goes through the switch S_{o5} and the series diode D_{o5}. During this time frame, Fig. 3(b) depicts the present path for the flow of the current. The voltage at the primary v_m is the same as the capacitor C_{i1} voltage whereas the voltage at the secondary v_a becomes zero. The current at the primary i_m rises at the rate of V_{Ci1}/L_{T1}. At this stage, the time duration becomes equal to $(1 - D_a)T_s/2$, and the current at the primary i_m is calculated as:

$$i_m(t) = \frac{V_{Ci1}}{L_{T1}}(t - t_b) + I_{i1} \qquad (3)$$

$I_{i1} = 0$ and $i_m(t_b) = I_{i2}$ due to this circuit setup, which may be calculated as follows:

$$I_{i2} = \frac{V_{Ci1}}{2 f_s L_{T1}}(1 - D_a) \qquad (4)$$

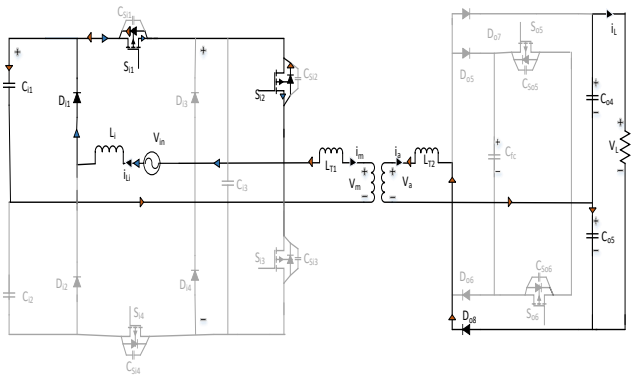
iii. Period c) [$t_c - t_d$]: The current at the secondary flows through D_{o7} and C_{o4} after switch S_{o5} is turned off. Whereas the voltage at the primary v_m is equal to the capacitor C_{i1} voltage, the voltage at the secondary v_a is equal to the capacitor C_{o4} voltage. The corresponding circuit of this period, with a time duration of $(D_m - D_{ph})T_s/2$, is shown in Fig. 3(c). The current at the primary i_m keeps flowing at the rate of $(V_{Ci1} - kV_m/2)/L_{T1}$ via C_{i1}, S_{i1}, and S_{i2}. The voltage across the leakage inductance determines the slope of i_m. Because V_{Ci1} is greater than $kv_L/2$ in the instance of Fig. 2, the slope of i_m is positive and may be calculated as:

$$i_m(t) = \frac{1}{L_{T1}}(V_{Ci1} - \frac{kV_L}{2})(t - t_c) + I_{i2} \qquad (5)$$

During period c), the peak current is calculated as:

$$I_{i3} = \frac{1}{2 f_s L_{T1}} (V_{Ci1} - \frac{kV_L}{2})(D_m - D_{ph}) + I_{i2} \qquad (6)$$

iv. Period d) [t_d – t_e]: When switch S_{i1} is turned off and switch S_{i2} is left on, the current at the primary i_m begins to flow via D_{i3} and S_{i2} and reduces at a rate of $-kV_L/(2L_{T1})$, whereas the current at the secondary flows via D_{o7} and C_{o4}. As



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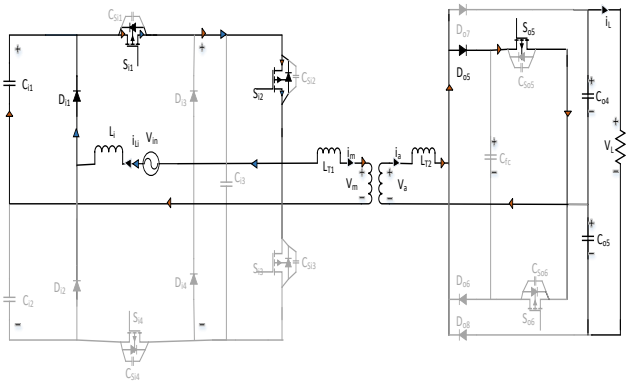

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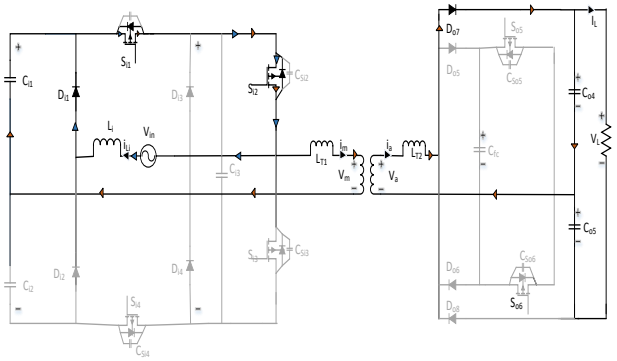

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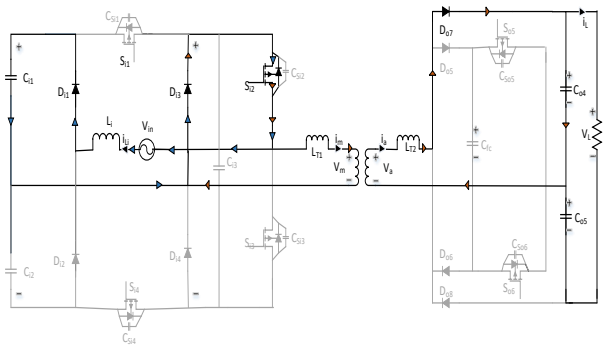

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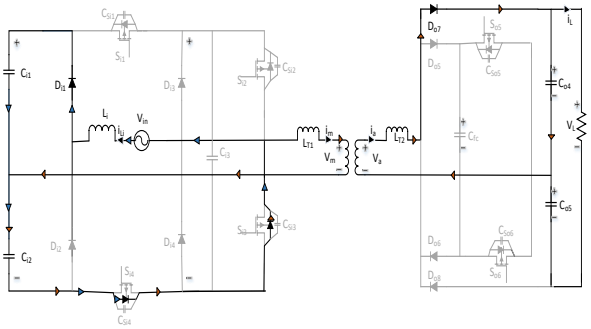

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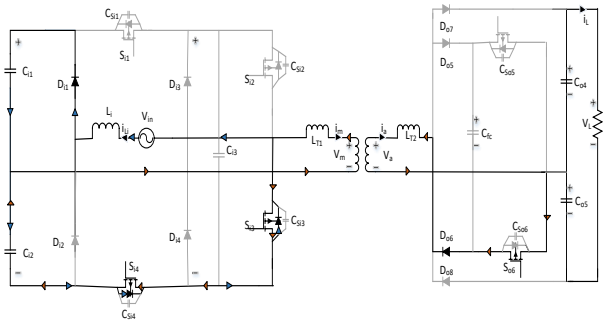

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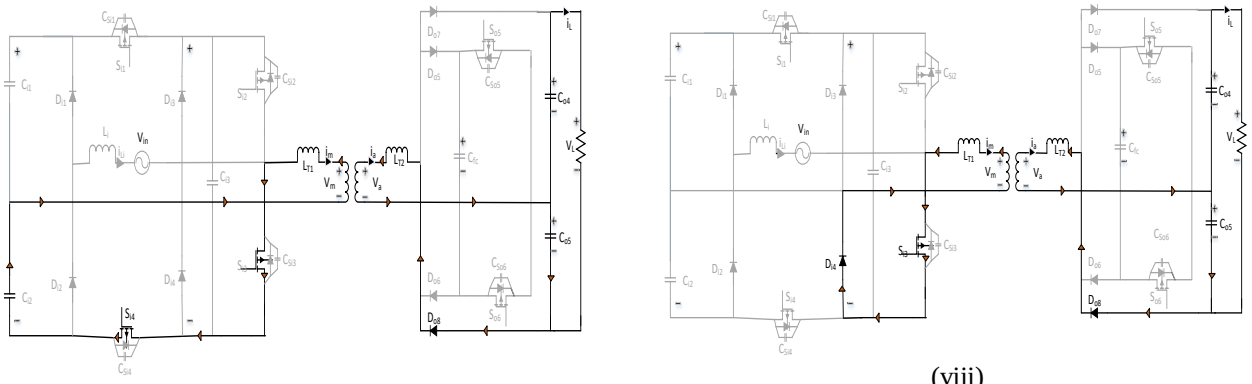


(vii) (viii)

Fig.3. Periods of steady state equivalent network of suggested methodology

illustrated in Fig. 3(d), the voltage at the primary v_m is zero, and the voltage at the secondary v_a is equal to the capacitor C_{o4} voltage, which again is equal to $V_L/2$. At this period, the time duration is $(1 - D_m)T_s/2$, and the primary current i_m is calculated by:

$$i_m(t) = -\frac{kV_L}{2L_{T1}}(t - t_d) + I_{i3} \quad (7)$$

At the end of this period d), the current is given as:

$$I_{i4} = -\frac{1}{2 f_s L_{T1}} \frac{kV_L}{2}(1 - D_m) + I_{i3} \quad (8)$$

v. Period e) $[t_e - t_f]$: The current at the primary flows via C_{i2} and the diodes which are antiparallel to S_{i3} and S_{i4}, whereas the current at the secondary continues to flow via D_{o7} after S_{i2} is turned off. I_m diminishes at a rate of $-(V_{Ci2} + kV_L/2)/L_{T1}$ because the voltage across the L_{T1} is negative. As seen in Fig. 3(e), the voltage at the primary v_m is negative and equal to the capacitor C_{i2} voltage, whereas the voltage at the secondary v_a remains positive as it was in the preceding period. The time duration of this period is the same as the period a) and the current at the primary is given as:

$$i_m(t) = -\frac{1}{L_{T1}}(V_{Ci2} + \frac{kV_L}{2})(t - t_e) + I_{i4} \quad (9)$$

The current at the primary i_m becomes zero at the end of this period and makes $I_{o5} = 0$.

vi. Period f) $[t_f - t_g]$: As seen in Fig. 3(f), the current at the primary i_m changes polarity and travels via S_{i3}, S_{i4}, and C_{i2}. To ensure lossless switching at turn ON, switch S_{o6} goes on before the primary current i_m gets negative. S_{o6} and D_{o6} now carry the current at the secondary, resulting in a voltage level of zero across the secondary winding of the high-frequency transformer. The voltage on the primary side v_m is equal to the negative voltage on capacitor C_{i2}, while the voltage on the secondary side v_a is zero. The time duration of this period is the same as period b) and the current at the primary is calculated as:

$$i_m(t) = -\frac{V_{Ci2}}{L_{T1}}(t - t_f) + I_{i5} \quad (10)$$

The starting condition of the primary current i_m is $I_{o5} = I_{i1} = 0$ at this point. By assessing equation (10) at $t = t_g$, at the end of the period, the primary current peak is I_{o6}, and at the steady-state, it equals $-I_{i2}$.

vi. Period g) $[t_g - t_h]$: Switch S_{o6} is turned off at the start of this period, and the current at the secondary conduct through C_{o5} and D_{o8}. The current at the primary i_m continues to diminish at a rate of $(kV_L/2 - V_{CI2})/L_{T1}$ as it passes via S_{i3}, S_{i4}, and C_{i2}. In the situation presented in Fig. 3(g), i_m reaches its highest negative peak value at the end of this period. The negative value of capacitor C_{i2} voltage is equal to the voltage at the primary v_m, whereas the voltage at the secondary v_a is equal to the negative value of capacitor C_{o5} voltage. The period time duration is the same as period c), and the current at the primary is given as:

$$i_m(t) = \frac{1}{L_{T1}}(\frac{kV_L}{2} - V_{Ci2})(t - t_g) + I_{i6} \quad (11)$$

vii. Period h) $[t_h - t_i]$: The main current i_m is conducted via S_{i3} and D_{i4} with a slope of positive value $kV_L/(2L_{T1})$. As illustrated in Fig. 3(h), the current at the secondary keeps flowing via C_{o5} and D_{o8}. The voltage at the primary v_m becomes zero, whereas the voltage at the secondary v_a becomes equal to the negative value of capacitor C_{o5} voltage $-V_L/2$. The period time duration is the same as period d) and the current at the primary is described as:

$$i_m(t) = \frac{kV_L}{2L_{T1}}(t - t_h) + I_{i7} \quad (12)$$

The current at the initial becomes $I_{o7} = -I_{i3}$.

From the steady-state analysis, the basic phase shift ph between the voltages of the primary and secondary can be calculated as:

$$ph = \frac{D_m}{2} - \frac{kV_L}{2V_d} D_a \quad (13)$$

Where V_d represents the dc-link voltage of the primary side. D_{ph} represents the total phase shift between the voltage of primary and secondary which is expressed in terms of primary duty cycle D_m and secondary duty cycle D_a. It is given as:

$$D_{ph} = 1 + \frac{D_m}{2} - (\frac{kV_L}{2V_d} + 1)D_a \quad (14)$$

III. LOSSLESS SWITCHING ANALYSIS

This division analyses of achieving lossless-switching at turn-on focuses solely on switch S_{i1} on the main side and switches S_{o5} and S_{o6} on the secondary side. The other switches have the same working principle and analytical techniques as the main and secondary currents, i_m and i_a, because of the uniformity of the main and secondary currents. At ZVS, all devices on both sides of the transformer are turned off.

A. *Switching devices at primary*

In comparison to the flying capacitor C_{i3}, the capacitance of the dc-bus capacitors (C_{i1}, C_{i2}) is similar and rather high. Moreover, the stray capacitance of switches (C_{Si1}, C_{Si2}, C_{Si3}, and C_{Si4}) is substantially lower than that of the capacitance of the capacitor C_{i3}. The voltages of the capacitors on the primary side are considered to be constant for simplicity, and across each semiconductor device, there is no voltage drop.

S_{i3} and S_{i4} are initially turned on, whereas S_{i1} and S_{i2} are turned off, as shown in Fig 3(g). The primary coil conducts the main current. As illustrated in Fig.3 (g) S_{i3}, S_{i4}, and C_{i2}, (brown arrows). C_{i3} and C_{Si2} are connected in parallel and C_{Si1} are connected in series with this combination. Due to this, the dc-bus capacitors' voltage must be evenly spread between C_{Si1} ($V_{CSi1} = V_{Ci1} = V_{Ci2}$) and the parallel combination of C_{i3} and C_{Si2} ($V_{CSi2}||V_{Ci3} = V_{Ci1} = V_{Ci2}$).

If $I_{o7} < 0$, the stray capacitance C_{So4} charges up to V_{Ci1} and C_{Si1} discharges to zero as fast as S_{i4} is turned off whereas S_{i3} is still turned on, and C_{i3} and C_{Si2} have constant voltage. At ZVS, S_{i1} can really be switched on throughout period (h) in Figure 3. At ZVS, switch S_{i3} off, causing C_{Si3} to charge to V_{Ci1} while C_{Si2} to discharge to zero. The current at the primary is start flowing via diodes which are connected anti-parallel to S_{i1} and S_{i2}, at ZVS fig.3 (a), C_{i1}, and L_{T1}, defining the criterion of switching on S_{i1} and S_{i2}. The following condition ensures that I_L is negative at the start of Period a):

$$D_{ph} + D_a \geq 1 \quad (15)$$

The flying capacitor C_{i3} extends the lossless-switching range for S_{i1} and S_{i4}, while the energy contained in L_{T1} allows C_{Si2} to discharge and C_{Si3} to charge.

B. *Switching devices at secondary*

The corresponding circuit at the secondary side of the transition between periods b) and c) shown in Fig. 3 is shown in Fig. 4(a). The terminals between D_{o5}, S_{o5}, and D_{o6}, S_{o6} are linked to the flying capacitor C_{fc}. C_{fc} is important because it allows the drain-source capacitance of S_{o5} and S_{o6} to be discharged, enabling ZVS to be achieved upon the switch on. As seen in Fig. 4 (a), when S_{o5} is turned off, the current at the secondary charges C_{So5} up to V_{Co4} and discharges C_{So6} to zero.

The voltage of C_{fc} is nearly constant in all working modes because its capacitance value is considered relatively higher than the stray capacitances of the switches and diodes. $I_a = kI_{i2}$ is expected to be fixed at the time S_{o5} is switched off. The following relation is produced by supposing that $C_{So5} = C_{So6} = C_{si}$:

$$kI_{i2} = C_{si}\frac{dV_{So5}}{dt} + C_{si}\frac{dV_{So6}}{dt} \quad (16)$$

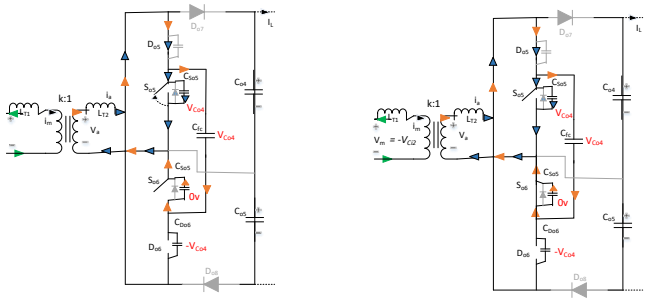
The greatest time taken to charge C_{So5} up to V_{Co4} and discharged C_{So6} up to zero can be obtained by integrating (16) on both sides:

$$t_m = \frac{4C_{Si} f_s L_{T1} V_{Co4}}{kV_{Ci1}(1 - D_a)} \quad (17)$$

Here D_a represents the duty cycle on the secondary side, which is restricted to $0 < D_a < 1$. The D_a limits are determined by the fact that $D_a = 0$ implies S_{o5} is turned on for the whole positive half cycle, while $D_a = 1$ implies S_{o5} is turned off for the full positive half cycle. The output capacitor C_{o4} is charged by the current at the secondary as fast as D_{o7} comes under the forward bias condition, as shown in Fig. 4(b) (blue arrows). As soon as $i_a > 0$ and conducts via D_{o7}, S_{o6} can be switched on at ZVS and ZCS.

The evaluation of charging C_{So6} and discharging C_{So5} follows the same pattern as before. When S_{o6} is turned off, C_{So6} is charging to V_{Co4}, and C_{So5} is discharging to zero, resulting in the change between Fig. 3(f) and Fig. 3(g). S_{o5} has the drain-source voltage which begins to reduce at a rate of $-C_{So5}dV_{So5}/dt$ till it goes to zero, while S_{o6} has the drain-source voltage which begins to grow at a rate of $C_{So6}dV_{So6}/dt$ till it goes to V_{Co4}. D_{o8} begins to conduct at this point, while S_{o5} can be switched on at ZVS and ZCS as soon as is less than 0 and passing via D_{o8}.

The gate-source signals V_{gs}, drain-source voltages V_{ds}, and drain currents i_d of S_{o5} and S_{o6} are shown in MatlabTM simulations in Fig. 5. The zero voltage and zero current switching transitions, as well as the periods when the stray capacitances C_{So5} and C_{So6} discharge, are labeled ZVS, ZCS, and discharge, respectively, in the diagram.



(a) (b)

Fig. 4. Charging and discharging C_{So5} and C_{So6} on an equivalent secondary side circuit. (a) When turning S_{o5} off, and (b) when turning S_{o6} on.

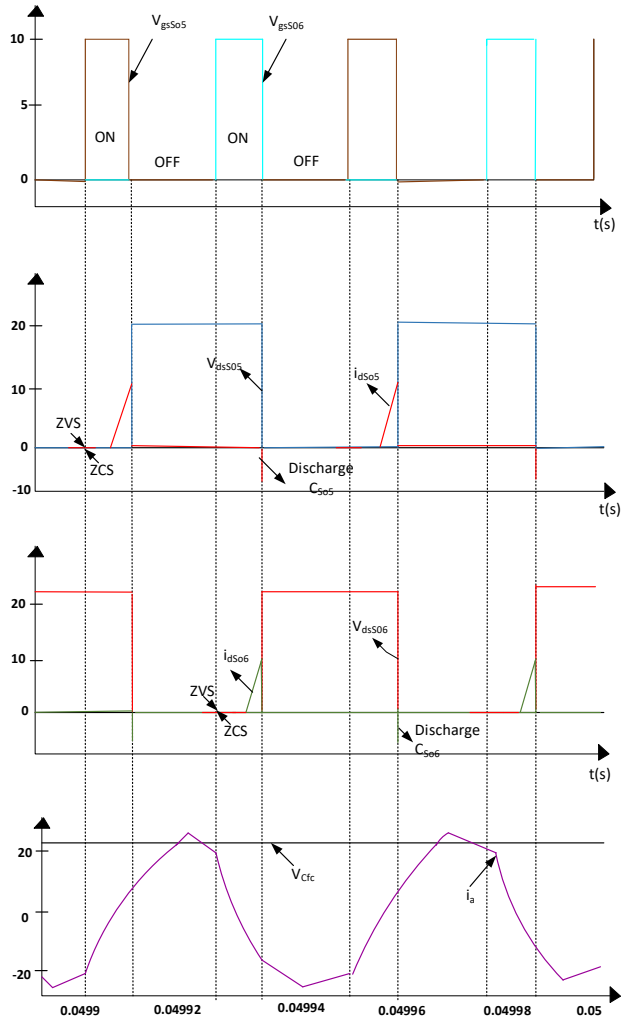


Fig. 5. Waveforms of lossless switched topology in simulation at the secondary side

IV. PROCESS FOR DESIGNING A CONVERTER

The suggested topology's design considerations are offered based on the mentioned converter standards:

V_{in} (t) = 110 Vrms (ac sinusoidal) at 60 Hz,

Power at the output, P = 900 W,

The voltage at the output, V = 200 V, and

Switching frequency, f_s = 20 kHz.

To ensure a high PF i.e. unity power factor, the primary side dc voltage V_d is chosen to be greater than double the peak input voltage V_p.

$$V_d > 2\sqrt{2}\, v_p = 312 \text{ V} \quad (18)$$

Now, on the primary side, 450 V is chosen as the dc-bus voltage. As a result, capacitors C_{i1} and C_{i2} must have a voltage rating greater than 200 volts.

A. *Designing of an Inductor*

The suggested inductor topology is designed to perform during DCM, which is ensured by meeting the following equation:

$$\frac{1}{2}\Delta i_{Li} \geq i_{Li} \quad (19)$$

Here, i_{Li} represents the peak ripple current of an inductor which is described by:

$$\Delta i_{Li} = \frac{V_d D_m T_s}{2L_i} \quad (20)$$

And

$$i_{Li} = \frac{P_m}{V_p D_m} \quad (21)$$

The critical value of the inductor to perform at DCM is obtained by adding (19), (20), and (21).

$$L_i \leq \frac{V_p{}^2 D_m{}^2}{8 f_s P_m} \quad (22)$$

L_i should be equal to or less than 160 μH and also equal to L_{T2} for 900 W and D_m = 1. To minimize exceeding the NPC devices' rating current, a value nearer to the upper range for L_i should be chosen. L_{T2} is used for smoothening the ripples of the output current. The current generated by the inductor is calculated as follows:

$$i_{Li(p)} = \frac{V_p}{2 f_s L_i} \quad (23)$$

B. *Capacitor Design for DC-Bus*

The allowable peak voltage ripple is used to build the dc-bus capacitors C_{i1} and C_{i2}. Since the inductor peak current i_{Li}(p) passes via the dc-bus capacitors, C_{i1} and C_{i2} be computed as:

$$C_{i1} = C_{i2} = \frac{P_m}{2V_p f_f \Delta v_{Ci1}} \quad (24)$$

Here, f_f represents the fundamental frequency of the ac source. The value of C_{i1} and C_{i2} are the same which is determined by using equation (24), $C_{i1} = C_{i2} > 4300$ μF.

C. *Designing of the high-frequency transformer*

Several papers have discussed the configuration of a high/medium frequency transformer, providing configuration steps [16], configuration trade-offs [17], and actual HFT solutions [16]. The needed leakage inductance turns ratio k = v_m / v_a, and magnetizing inductance L_{mg} is the most significant characteristics to evaluate. The number of turns and the design of the cores determine the value of L_{mg}. L_{mg} is

expected to be quite high in this topology, therefore it can be left out of the study. Depending on the value of k, the suggested topology can be used as a buck or boost converter. The converter functions in boost state if the voltage at the secondary v_a on the primary coil is greater than the voltage at the primary v_m; else, it runs in buck state. To run in the buck state, k should be less than 2 for v_m = 200 V and v_a = 100 V. The buck state is discussed in this study. Following the configuration approach outlined in [17] and the suggested topology's parameters, the value of flux density B_o = 0.0536 T and the number of turns on the primary N_m can be evaluated by:

$$N_m = \frac{V_m}{k_w B_o A_a f_s} \tag{25}$$

Here, k_w = 4 represents waveform factor, A_a = 7.78 cm^2 represents cross-section area of core, and, N_m = 50 represents primary turns.

Due to this, the number of turns at the secondary N_a should be less than to primary turns. The value of k is determined by the semiconductor device rating. Therefore, in respect of transformer efficiency, choosing k near 1 is the optimum option [17].

In the positive half cycle, the output power is supplied from the ac source to the load is provided by:

$$P = \frac{2}{T_s}\int_{t_a}^{0.5T_s} v_p i_{L_{T1}}(t)\,dt \tag{26}$$

$$P = \frac{v^2{}_p}{4 f_s L_{T1}}\left(\frac{kV_L}{v_m}X + Y\right) \tag{27}$$

$$X = -\frac{D_m^{\,2}}{2} - \frac{D_a^{\,2}}{2} - D_{ph}^{\,2} + D_a + D_{ph} + (D_{ph} - D_a + 1) - \frac{1}{2} \tag{28}$$

$$Y = D_m^{\,2} + 2D_m(1 - D_a - D_{ph}) \tag{29}$$

For the maximum value of power, the value of D_{ph} = 0.5, D_m = 1, D_a = 0.84, then leakage inductance L_{T1} = 146 μH.

D. *Designing of the output capacitor*

D_{o7} is forward biased when S_{o5} is turned off, and the current at the secondary is equal to:

$$i_a(t) = k i_m(t) = C_{o4}\frac{\Delta V_{Co4}}{\Delta t} + \frac{V_L}{R_L} \tag{30}$$

While i_a higher than the current at the output I_L, C_{o4} is charged, and if i_a lower than I_L, C_{o4} is discharged. This period ($\Delta t = (1 - D_a)T_s/2$) has 3 distinct slopes defined by (5), (7), and (9). C_{o4} can be determined by reordering (30) and integrating both sides as follows:

$$C_{o4} = \frac{k^2 V_L}{16 f_s^{\,2} L_{T1} \Delta V_{Co4}}\left[X_{i1} + \frac{2V_{Ci1}}{kV_L}Y_{i1} - \frac{4L_{T1} f_s D_a}{k^2 R_L}\right] \tag{31}$$

$$X_{i1} = -\frac{D^2_{\ m}}{2} - \frac{D_{ph}^{\ 2}}{2} - \frac{D^2_{\ a}}{2} + D_m D_{ph} \tag{32}$$

$$Y_{i1} = -\frac{D^2_{\ ph}}{2} - \frac{3D^2_{\ a}}{2} + 2D_a + D_{ph} + D_m D_a - 2D_{ph}D_a - \frac{1}{2} \tag{33}$$

The lowest value of the output capacitors may be obtained by equation (31) as $C_{o4} = C_{o5} > 20$ μF, for $\Delta V_{Co4} < 0.05*100$ V, D_m = 1, D_{ph} = 0.5, and D_a = 0.84.

V. SIMULATION RESULTS

In terms of electricity quality and regulation, a microgrid gives benefits to utilities and consumers. Renewable energy resources, distributed grid lines, power conversion equipment, and loads are all included in a conventional microgrid.

PARAMETER TABLE

Parameter	***Values***
Switching frequency(f_s)	20kHz
Input voltage v_{in}(t) (RMS)	690V
Output Power P	25kW
Output Voltage V_L	2kV
Output Current I_L	12.5A
Input inductor L_i	160 μH
High Side dc voltage $V_d > 2V_p$	2kV
Low side capacitor voltage V_{Co4}=V_{Co5}	1kV
Inductor at primary (L_{T1})	146μH
Inductor at secondary (L_{T2})	160 μH

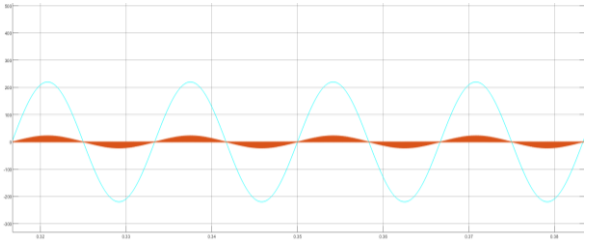


Fig.6. simulation of input current and voltage

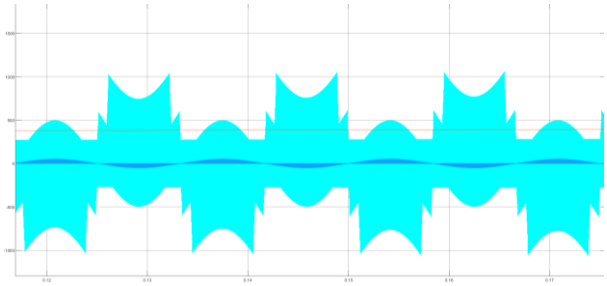


Fig.7. Simulation of V_d, v_{Li}, i_{Li}.

In Figure. 6, the current at the input is in the same phase as the voltage at the input. Figure 8 shows the voltage and current of the boost inductor, as well as the dc-bus voltage. When the boost inductor current is zero, the inductor voltage oscillates because of a resonance between the stray capacitances D_{i1}, S_{i1}, and S_{i2} and the boost inductor.

The following are the distinguishing characteristics of the suggested topology over other traditional facilities:

a) Other identical configurations involve more than six switching devices [16],[19], and we were capable of managing the dc-bus and output voltage with only six switching devices.

b) Other known topologies cannot reach identical benefits with active devices at secondary switching at ZVS and ZCS over the wide range of power [15].

c) The suggested topology has a better efficiency of 94.5 percent compared to the topology provided in [15], which estimates the highest efficiency of 93 percent.

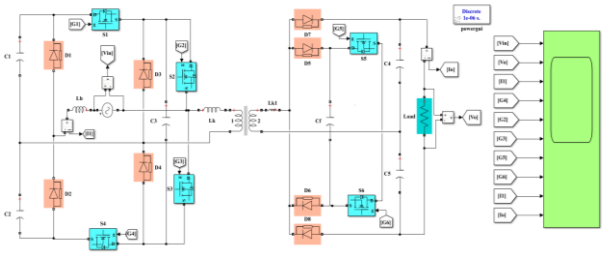


Fig.8. Simulation Diagram

VI. CONCLUSION

The purpose of this study is to develop a new low-cost ac-dc power rectifier with a higher switching frequency topology and fewer switches on the secondary side to improve power factor and total harmonic distortion. By using two switching devices and four diodes on the secondary side of the circuit, we will produce voltage waveforms. This configuration provides control on power at the input, voltage at the output, and voltage at the dc bus. This novel configuration helps to improve the input power factor and total harmonic distortion by using fewer switching devices at a higher switching frequency. Due to less number of switching devices, this novel configuration becomes more cost-efficient than the conventional one. The only disadvantage of this topology is that it only provides unidirectional power flow.in this topology, there is no requirement of external control effort. The results of the simulations for this novel topology matched the mathematical equations, steady-state analysis, and closed-loop control performance quite well.

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