INTERNATIONAL JOURNAL OF SCIENTIFIC RESEARCH IN ENGINEERING AND MANAGEMENT (IJSREM)
VOLUME: 07 ISSUE: 12 | DECEMBER - 2023 SJIF RATING: 8.176 ISSN: 2582-3930

A NOVEL LOW POWER ALU DESIGNED BY USING HYBRID STT-MTJ/CMOS CIRCUIT

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Abstract — The rise in power dissipation when the technology descends into the deep submicron zone is one of the main issues for CMOS technology due to its non-volatility, high speed, high endurance, CMOS compatibility, and primarily the low power dissipation. magnetic tunnel junction (MTJ) working on Spin transfer torque (STT). Switching mechanism is recognized as one of the most promising spintronic devices for post-CMOS era. This device can provide solutions for the issues posed by existing CMOS technology. We have put out a brand-new hybrid STT-MTJ/CMOS circuit-based logic-in-memory (LIM) P-magnetic arithmetic logic unit (P-MALU) design.. The behavior of P-MALU designs in terms of power dissipation is then studied using Monte-Carlo(MC) simulation, which incorporates process and mismatch variations for CMOS and extracted parameters of MTJ . The P-MALU circuit has also been expanded to provide 4-bit arithmetic operations. Electrical simulations are run to ensure the design's operation.

Keywords—

MTJ , Spintronics , non-volatility, Switching mechanism ,STT-MTJ, logic in memory, p-magnetic arithematic unit, monte- carlo simulation

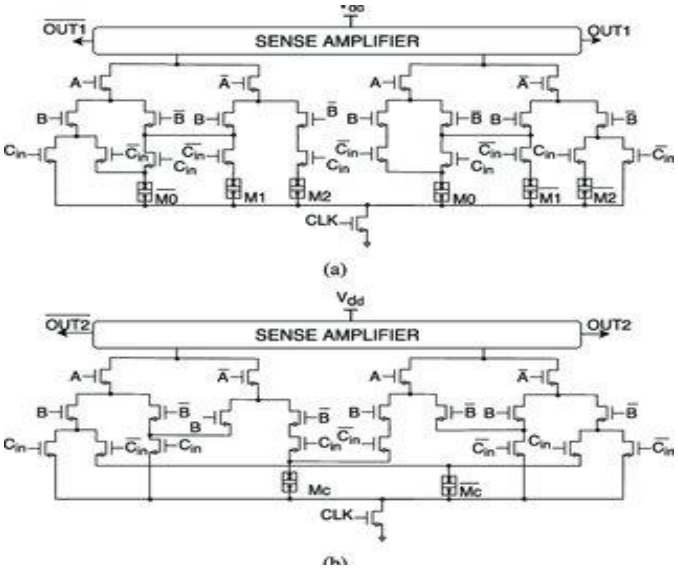
Introduction (MTJ)

Magnetic Tunnel Junctions (MTJs) are a type of solid-state device used in the field of spintronics, which combines electronics and magnetism. MTJs consist of two ferromagnetic layers separated by a thin insulating layer. The key principle behind MTJs is the phenomenon of tunnel magnetoresistance (TMR). Here's how they work: Ferromagnetic Layers: The MTJ consists of two ferromagnetic layers with different magnetization directions. These layers can be made of materials like iron, cobalt, or nickel. Insulating Layer: Between the two ferromagnetic layers, there's a very thin insulating layer, typically made of materials like aluminum oxide (Al2O3). This insulating layer is crucial because it allows for electron tunneling to occur Tunneling Effect: Electrons can "tunnel" through the insulating layer when it is thin enough. The probability of tunneling depends on the relative alignment of the magnetic moments (spins) of the two ferromagnetic layers. The ALU is designed with techniques as A quantum-dot- cellular-Automata (QCA) is used to design ALU and the executed output proved that this design is efficient in terms of cell count, place and energy

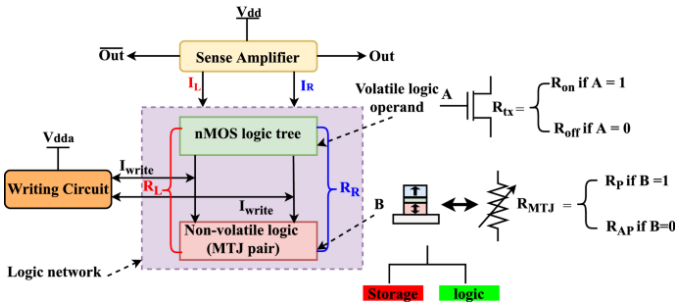
utilization. And A new structure of magnetic ALU depending on the combination of Spin-transfer-torque-magnetic-tunnel-junction/CMOS devices is proposed and concluded that they can provide low energy consumption with less transistors. The layout and utilization of ALU based on logarithmic structure is proposed and analyzed on various arithmetic functions.Finally, concluded that the designed one

I. IMPLEMENT OF ALU BY MTJ

As illustrated in the Figure, communication between the logic and memory blocks is enabled by wires and interconnects in a traditional Von-Neumann architecture. This tactic degrades the chip's overall performance. As wire length increases, a noticeable delay is introduced between these two blocks. According to ITRS, the length of global interconnects has a significant impact on latency when compared to local interconnects. Additionally, the requirement for large driver circuits on global wires results in a significant power dissipation. Furthermore, the standby power dissipation of a MOSFET increases as its channel length decreases. As a result, the total power dissipation will rise.



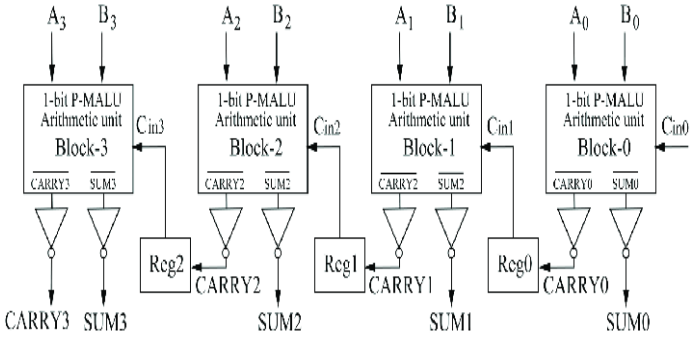
II. ALU CIRCUIT



1) Detector/Read Circuitry: This circuit configuration is a current comparator. After pull-down networks (PDNs) have finished processing inputs, sense (a) Redesigned sum sub-circuit structure for M-MALU to generate SUM, SUM in arithmetic addition and XOR, AND, and OR functions in logical mode of operation, along with their complements. (b) The carry sub-circuit for M-MALU has been modified to produce CARRY, CARRY when adding arithmetically. The output of an amplifier is given in its authentic and complementary form.

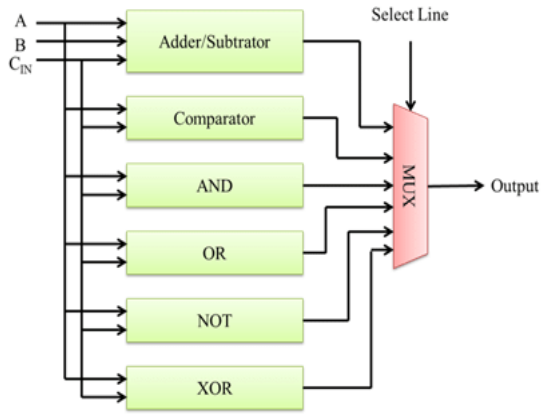
2) Pull down network: This is an MTJ and MOS logic structure combination. Here, MTJs and MOS logic both contribute to the logical operations.

3) The input data is written into the MTJ using the writing block of the LIM architecture.
An amplifier for current comparator pre-charge sense is employed in the M-MALU and P-MALU designs. On the other hand, writing circuits is derived from writing MTJ states.



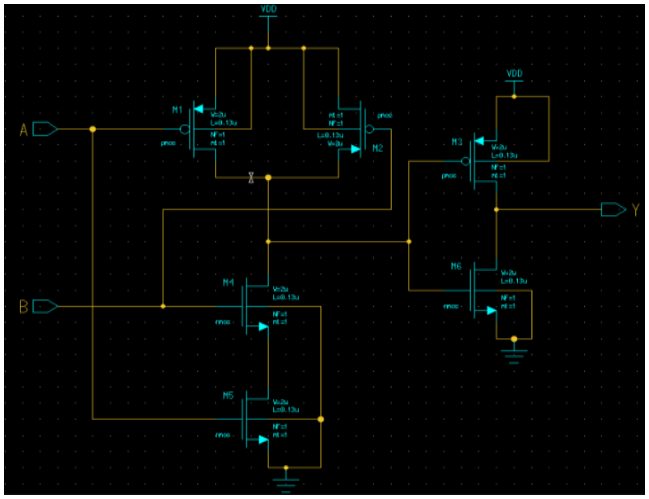
Now we study about the alu using cadence

- Typically, the ALU has direct input and output access to the processor controller, main memory (random access memory or ram in a personal computer) and input/output devices. Inputs and outputs flow along an electronic path that is called a bus.

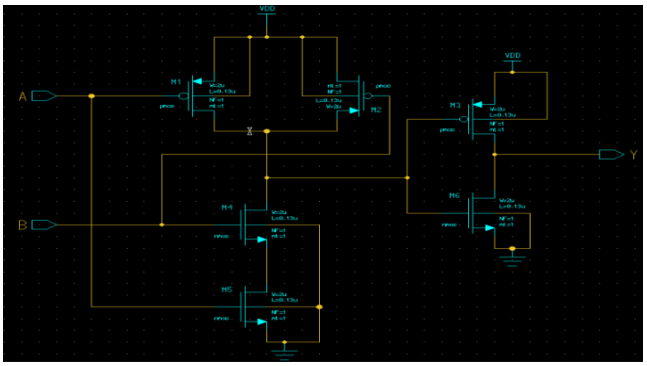


- An alu consists of too many combinational and sequential circuits they are

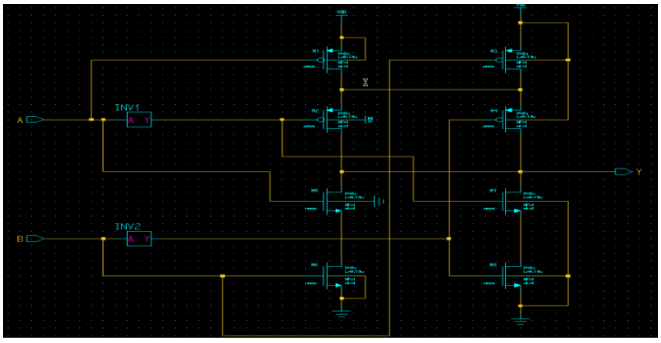
Schematic of AND gate :



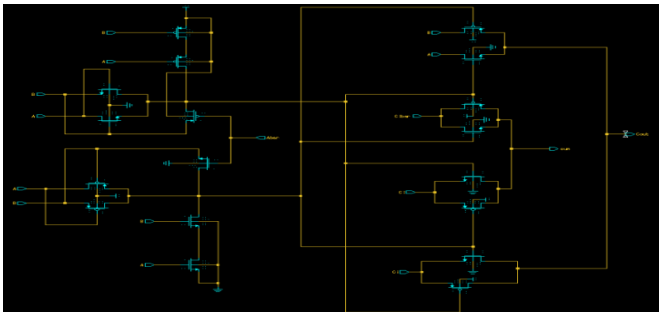
Schematic of OR gate :



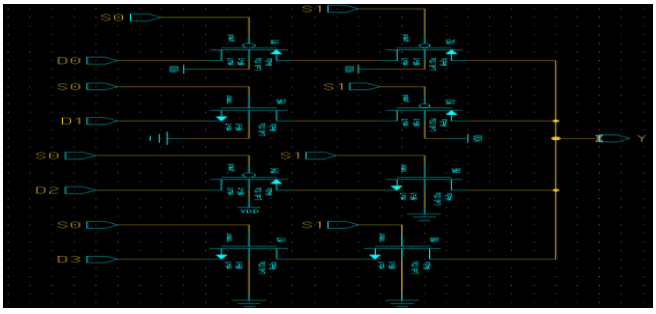
Schematic of XOR gate :



Schematic of Full Adder:

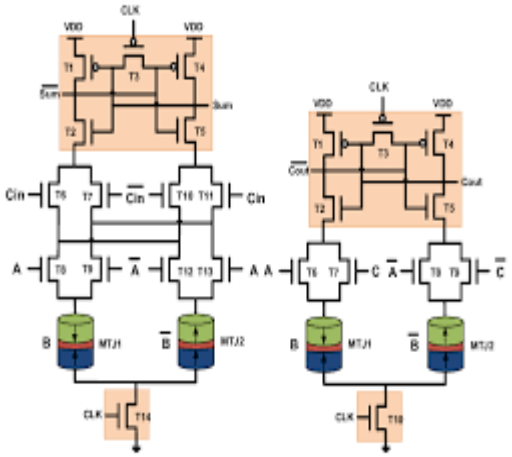


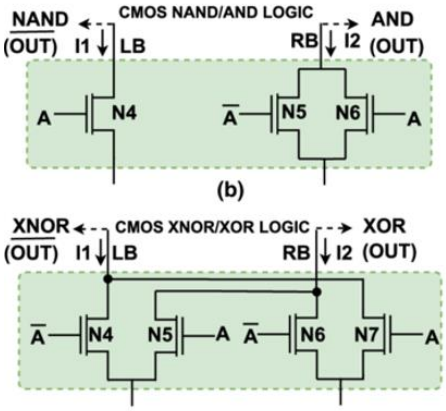
Schematic of MULTIPLEXER Design

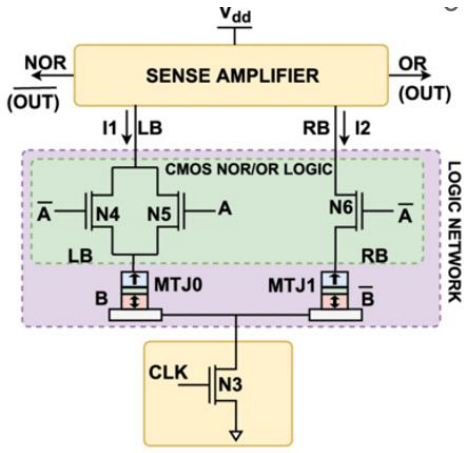


OR GATE:

The OR gate is a digital logic gate that implements logical disjunction. The OR gate outputs "true" if any of its inputs are "true"; otherwise it outputs "false". The input and output states are normally represented by different voltage levels.

- 

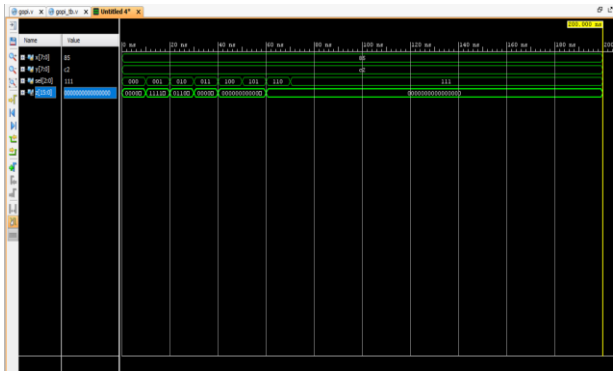
- 

- 

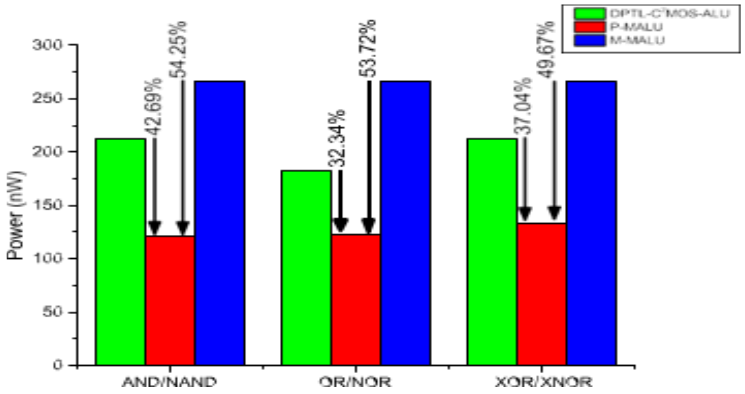
- GATE LEVEL MODELING:

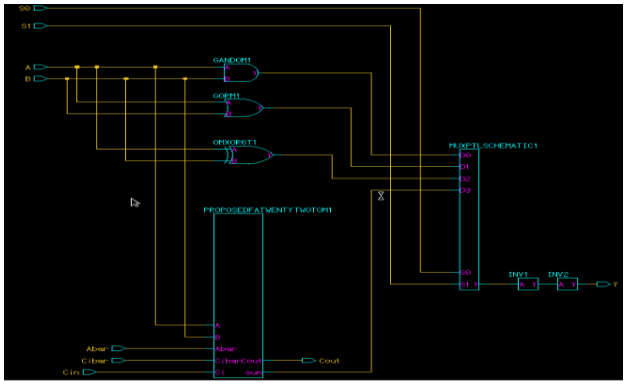
```
module PALU(x,y,sel,z);
input [7:0]x,y;
output reg [15:0]z;
input [2:0]sel;
parameter ADD=3'b000;
parameter SUB=3'b001;
parameter MUL=3'b010;
parameter DIV=3'b011;
parameter AND=3'b100;
parameter OR=3'b101;
parameter NOT1 =3'b110;
parameter NOT2 =3'b111;
always@(*)
case(sel)
ADD: z=x+y;
SUB: z=x-y;
MUL: z=x*y;
DIV: z=x/y;
AND: z=x&&y;
OR: z=x||y;
NOT1: z=!x;
NOT2: z=!y;
endcase
endmodule
```

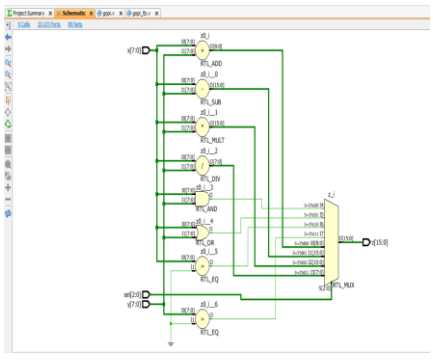
Logic	OPERATION	POWER DISSIPATION	DEVICE COUNT	NO
DPTl	XOR/XNOR/OR/NOR/NAND/AND/OR	212	36	1
MALU	XOR/XNOR/OR/NOR/NAND/AND/OR	265	41	2
P MALU	XOR/XNOR/OR/NOR/NAND/AND/OR	135	21	3



Schematic of SINGLE BIT ALU Design







CONCLUSION:

a novel P-MALU design is proposed and its power dissipation, device count, and delay are found to be better than those of DPTL-C2MOS-ALU and M-MALU designs. Because MTJs are not volatile in the slightest, when the power is turned on, the stored values are immediately usable for logic operations in addition to being stored. Because MTJ-developed hybrid circuits are non-volatile by nature, they don't require "backup" and "restore" functions and require zero static power consumption in standby mode. Compared to volatile CMOS design, hybrid circuits have this important advantage. The findings covered in this paper indicate that the suggested design uses less power and takes up less space on the silicon.Magnetic Tunnel Junctions (MTJs). An ALU is a crucial component of a computer's central processing unit (CPU), responsible for performing arithmetic and logic operations. However, MTJs are known for their use in magnetic random-access memory (MRAM), a type of non-volatile memory.

REFERENCES:

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[3] SREEVATSAN RANGAPRASAD AND VINOD KUMAR JOSHI , (Senior Member, IEEE) Received 26 September 2023, accepted 18 October 2023, date of publication 23 October 2023, date of current version 1 November 2023. Digital Object Identifier

[4] Jibin Wu , Chenglin Xu, Xiao Han, Daquan Zhou, Malu Zhang , Haizhou Li , Fellow, IEEE, and Kay Chen Tan , Fellow, IEEE