A Review of Machine Learning-Based Device Modeling and Performance Optimization for FinFETs

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***Abstract*—**The research explores the use of performance optimization strategies to further enhance FinFET device efficiency. By analyzing data from FinFets under various conditions, optimization algorithms are developed to fine-tune device parameters. This approach not only refines individual device performance but also contributes to improved circuit efficiency. The synergy between accurate models and optimization algorithms leads to faster, more energy-efficient, and reliable devices.The significance of this research extends to its potential to revolutionize design and manufacturing processes in the electronics industry. The ability to accurately model FinFET devices and optimize their performance opens new possibilities for innovation. Engineers can now design and manufacture devices with greater precision, tailoring them to specific requirements and achieving unprecedented levels of efficiency.

Moreover, the integration of ML in this context addresses the limitations of traditional approaches, particularly the computational demands associated with extensive simulations. ML-based models streamline the prediction of device behavior, significantly reducing the need for time-consuming simulations. This not only accelerates the design process but also conserves computational resources, making it a more sustainable and efficient solution.

In conclusion, this research marks a paradigm shift in semiconductor device modeling and optimization, leveraging machine learning to advance FinFET understanding and enhance performance. Beyond individual devices, it influences circuit efficiency, paving the way for a more advanced and sustainable electronics industry.

***Keywords*—** FinFET, Machine learning, Device modeling, Performance optimization, FinFET technology, ANN.

I. INTRODUCTION

Fin Field-Effect Transistors (FinFETs) have revolutionized integrated circuits, introducing a delicate balance between heightened performance and energy efficiency. These three-dimensional transistor structures, resembling tiny switches on a computer chip, redefine semiconductor devices. Yet, their intricacies and variations during manufacturing pose significant challenges. In response, machine learning emerges as a transformative force, seamlessly integrating into semiconductor engineering.

FinFETs demand a nuanced equilibrium between optimal performance and minimal power consumption, challenging traditional manufacturing processes. Machine learning acts as a sophisticated problem-solving tool, navigating the intricate web of data associated with FinFET behavior[1]. Operating in a dynamic environment influenced by multiple factors, FinFETs benefit from machine learning's unique capability to analyze multidimensional datasets.

Machine learning excels in pattern recognition, rapidly piecing together complex information, analogous to assembling puzzle pieces. In semiconductor engineering, this translates to a more comprehensive understanding of FinFET behavior. A primary challenge in FinFET manufacturing is managing process variations and device characteristics. Machine learning proves to be an empowering tool in handling these complexities, learning from historical data and real-time observations to make more accurate predictions.[2]

The collaboration between machine learning and semiconductor engineering represents a strategic approach to chip design in the data-driven era. Engineers optimize current chip designs and open new avenues for innovation in integrated circuits. Insights from machine learning can lead to novel architectures, materials, and manufacturing processes.

Embracing this synergy between human expertise and machine intelligence, the trajectory of electronic devices reaches new heights of efficiency and capability. The marriage of FinFETs and machine learning is an ongoing evolution.[3] The adaptability of machine learning algorithms ensures continuous learning, contributing to a dynamic and iterative improvement process.

Finally, the convergence of FinFETs and machine learning marks a significant paradigm shift in semiconductor technology, addressing challenges with solutions beyond traditional approaches. The future promises a semiconductor landscape where collaboration between human ingenuity and machine intelligence propels innovation, pushing the boundaries of efficiency and capability in electronic devices.[4][5]

II. REVIEW OF METHODOLOGIES

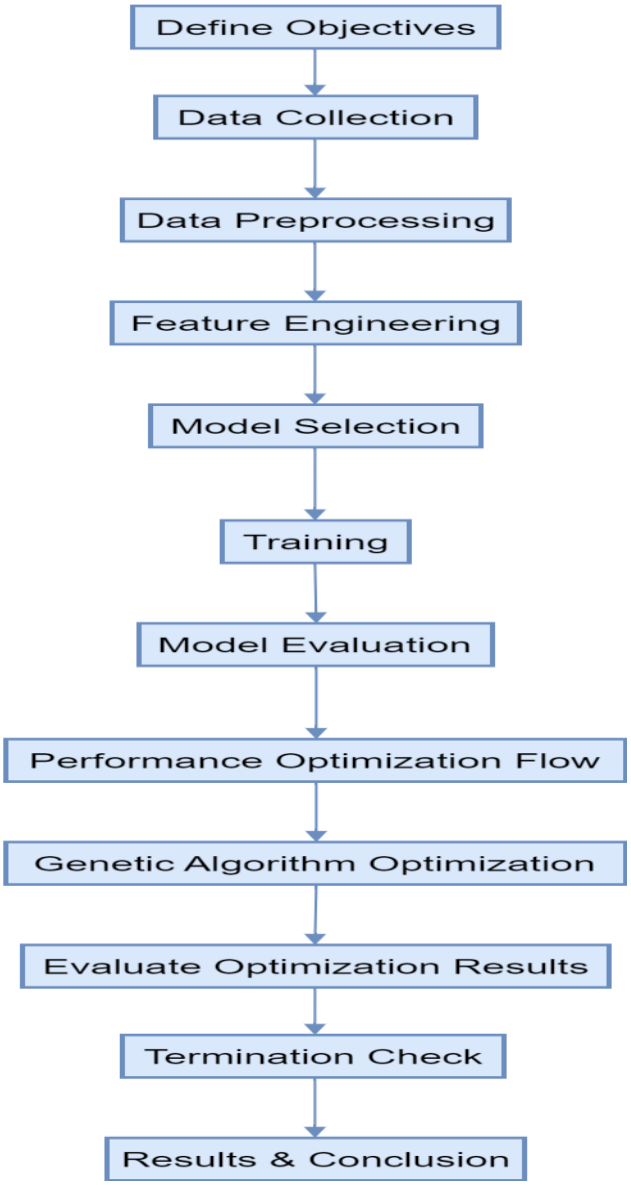

Figure 1. Flowchart of methods involved

Two-Stage Machine Learning-Based Device Modeling: The advancement of semiconductor technology, particularly in the realm of Fin Field-Effect Transistors (FinFETs), has prompted a transformative shift in integrated circuit design. The intricacies of managing device characteristics and process variations while optimizing performance and minimizing power consumption have fueled a quest for innovative methodologies. The intersection of machine learning and semiconductor engineering presents a promising avenue to address these challenges.

In the first phase of the proposed approach, Artificial Neural Network (ANN) models take center stage. These models are trained to predict discrete anchor points on the I-V (current-voltage) and C-V (capacitance-voltage) curves based on FinFET parameters. FinFETs, functioning as miniature switches on a computer chip, exhibit complex behavior influenced by factors like gate voltage and process variations. The ANN models act as intelligent translators, deciphering the relationships between these parameters and specific points on the characteristic curves. This phase serves as a foundational building block, enhancing the interpretability of the machine learning model by establishing connections between abstract device parameters and observable electrical behavior.

In the second phase, the focus shifts to achieving a more comprehensive understanding of FinFET behavior. Another ANN model is employed to fit continuous I-V and C-V curves. Unlike the discrete points predicted in the first phase, this model tackles the challenge of predicting entire continuous curves. This step is crucial for obtaining a nuanced grasp of how FinFETs respond to varying inputs and conditions. The ability to predict continuous curves enhances the model's precision, enabling it to capture the subtleties of FinFET behavior that discrete point predictions may overlook. The two-stage technique ensures that the machine learning model, trained through this comprehensive approach, can offer a holistic and accurate representation of FinFET characteristics.

Optimization Technique and Reduction in TCAD Simulations

Conventional optimization of device performance relies on extensive Technology Computer-Aided Design (TCAD) simulations. These simulations systematically analyse the influence of diverse factors on device behavior, empowering engineers to fine-tune parameters for enhanced performance. This iterative process aids in understanding and optimizing semiconductor devices through a comprehensive exploration of their operational characteristics.

To overcome computational challenges in optimizing device performance, we integrate machine learning (ML). Our approach mitigates the need for numerous TCAD simulations. The ML-based model, trained to understand FinFET parameter-electrical characteristic relationships, predicts device behavior efficiently. This reduces computational demands, making the design and optimization process more streamlined and resource-effective.

In a robust evaluation with 10,000 instances, our ML-based model efficiently predicts I-V and C-V curves, optimizing Ion/Ioff and minimizing RC. Minimal runtime enhances efficiency.

ML-Based Optimization with Genetic Algorithm Flowchart:

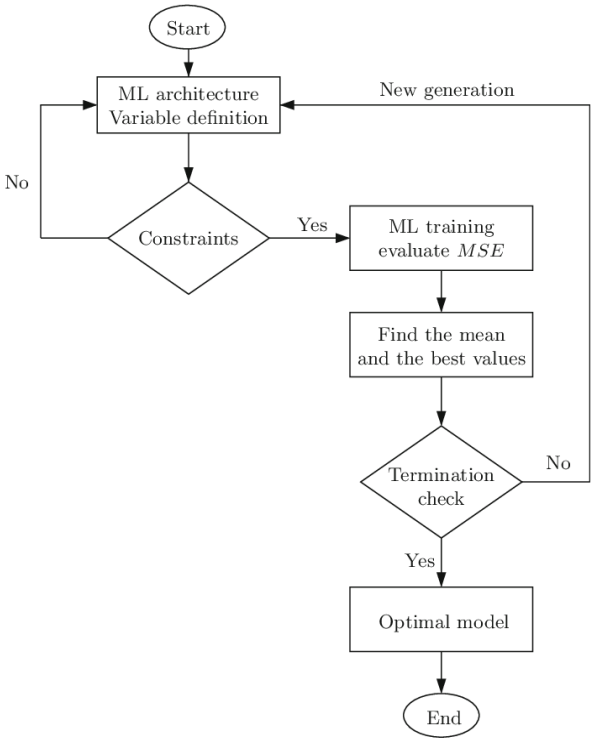

Figure 3. Flowchart explains genetic algorithm

The optimization process is further refined through the incorporation of a Genetic Algorithm (GA), an intelligent optimization technique inspired by biological evolution. GAs mimic the process of natural selection and evolution to iteratively improve solutions to complex problems. In the context of device optimization, the GA operates in conjunction with the ML-based model, guiding the search for optimal device parameter combinations. The flowchart depicting the ML-based optimization with a Genetic Algorithm outlines the step-by-step procedure of this synergistic approach. The GA begins with an initial population of potential solutions, each represented by a set of device parameters. At each iteration, the GA employs three main rules: crossover, mutation, and selection. Crossover involves combining the parameters of two parent solutions to create offspring, mimicking genetic recombination. Mutation introduces small, random changes to individual solutions, introducing diversity into the population. Selection in evolutionary algorithms retains solutions for the next generation based on performance, assessed through the Mean Squared Error (MSE) as the optimization objective function. Solutions with lower MSE are favored, guiding the algorithm towards improved performance over successive generations.

In conclusion, the proposed two-stage machine learning-based device modeling, coupled with a Genetic Algorithm for optimization, represents a comprehensive and innovative approach to semiconductor engineering. By integrating machine learning into the traditional TCAD simulation process, our

methodology reduces computational complexity and accelerates the optimization of FinFET device parameters.

Vgs	Ids_TCAD	Ids_ANN	Cgg_TCAD	Cgg_ANN
-2	0.1	0.09	0.005	0.0052
-1	0.5	0.48	0.012	0.0125
0	1.2	1.18	0.025	0.0248
1	3	2.95	0.065	0.0662
2	5	4.95	0.12	0.1198
3	8	7.95	0.2	0.2012

Table I. values for analysis using ANN and TCAD

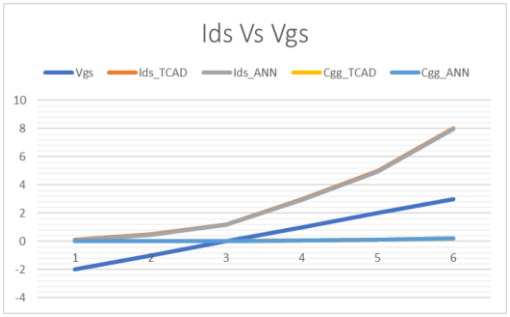

Figure 5. Graphical representation of example values

Machine learning models have emerged as indispensable tools in the realm of semiconductor design, particularly in deciphering the complex connections between FinFET parameters and device performance. The intricate relationships within FinFETs pose a formidable challenge, and machine learning's predictive prowess proves instrumental in unraveling these complexities. These models excel at predicting continuous I-V (current-voltage) and C-V (capacitance-voltage) curves, providing engineers with a deeper understanding of device behavior. Genetic Algorithms optimize FinFET parameters, leveraging evolutionary principles for systematic exploration, leading to optimal configurations and enhanced device performance.

The comprehensive understanding of intricate relationships within FinFETs, facilitated by machine learning models and Genetic Algorithms, streamlines the identification of configurations that lead to optimal device behavior. This not only accelerates the design process but also enhances the precision of semiconductor device optimization. The synergy between machine learning and Genetic Algorithms empowers researchers to navigate the intricate landscape of FinFET design with unprecedented efficiency, marking a significant advancement in semiconductor engineering. Ultimately, this collaboration contributes to the overall effectiveness and precision of semiconductor device optimization, offering invaluable tools for engineers in their quest for enhanced performance and efficiency in FinFET design.

	ON/OFF(TCAD)	ON/OFF(ANN)	RC (TCAD)	RC (ANN)
Lg	22 nm	23 nm	19 nm	19 nm
pro	3 nm	3	3 nm	3 nm
Wtop	4 nm	4 nm	4 nm	4 nm
Afin	90°	90°	90°	90°
Tspr	4 nm	4 nm	5.5 nm	5 nm
H fin	53 nm	53 nm	49 nm	48 nm
Nsd	2.5 x 10^20	2.5 x 10^20	1.9 x 10^20	2.5 x 10^20

Table II. Optimized Parameter Values with Single-Factor Analysis DOE Method

The reduction in the number of TCAD simulations, from thousands to hundreds, is a significant efficiency gain. This not only saves computational resources but also allows for a more thorough exploration of the parameter space, leading to the identification of superior candidates for device optimization. The fusion of machine learning and the Genetic Algorithm bridges the gap between theoretical predictions and real-world device performance, offering a powerful methodology for semiconductor engineers to enhance the efficiency and effectiveness of FinFET-based integrated circuits. As we navigate the ever-evolving landscape of semiconductor technology, such innovative approaches hold the key to unlocking new levels of performance and energy efficiency in electronic devices.

III. RESULTS AND DISCUSSIONS ON REVIWED WORK

We use a 2-Fin FinFET PMOS device as the example device. The device structure is labeled as 7 nm node by 2018 IRDS with 32 nm fin pitch and 54 nm poly pitch.This model accurately predicts multiple curves under different parameter combinations, bridging the gap between discrete point predictions and continuous I-V and C-V curve modeling. In contrast to earlier methods, it offers a substitute for TCAD simulation by capturing a variety of curve behaviors.

In order to further increase the inference accuracy of Ids at subthreshold region, we construct a WDE network using the following method. A practical definition for threshold voltage Vt is the Vgs at which, Id = 100 nA × $\frac{W}{L}$, since Id is proportional to $e^{q(Vgs-Vt)/\eta kt}$, it can be written

$$Id = 100\ nA \cdot \frac{Weff}{Leff} \cdot e^{q(Vgs-Vt)/\eta kt}$$

$$Ioff = 100\ nA \cdot \frac{Weff}{Leff} \cdot 10^{-Vt/SS}$$

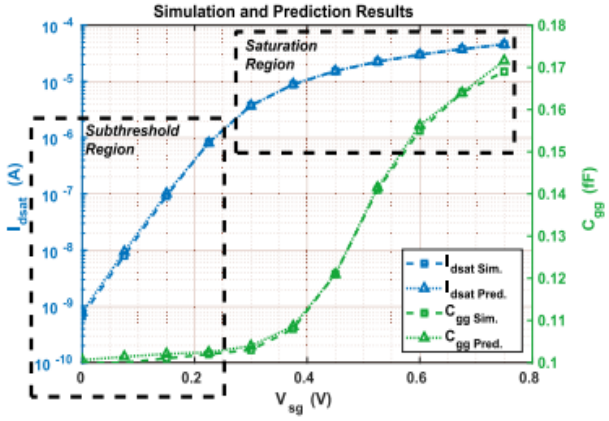

Figure 5. Prediction of different anchor points using ANN [1]

In addressing emerging semiconductor technologies, our research emphasizes the effectiveness of Machine Learning (ML) in precisely modeling FinFETs' I-V and C-V curves based on geometric parameters. This approach provides a compelling alternative to traditional TCAD simulations, especially when dealing with evolving technologies. The ML-based device model ensures accurate curve representation and opens avenues for optimizing performance across multiple objectives. Its adaptability streamlines semiconductor engineering processes, positioning ML as a powerful tool amid the dynamic semiconductor landscape. As technology advances, ML's versatility offers tailored insights for contemporary semiconductor devices, accelerating innovation. This research underscores ML's transformative potential, navigating design challenges efficiently, and contributing to the rapid evolution of semiconductor engineering. In conclusion, the integration of ML signifies a pivotal advancement, addressing modern semiconductor complexities and paving the way for broader applications, marking a significant stride toward a more efficient and dynamic era in semiconductor engineering. Combining Artificial Neural Networks (ANN) with physical knowledge and a fitting target in our study proved instrumental in accurately predicting Ids in the subthreshold region, a domain highly sensitive to geometrical parameters. The integration of ANN enhances the efficiency of predicting intricate device behaviors.

Our results highlight a substantial acceleration in data generation with our approach. This efficiency boost allows us to embark on a quest for ideal device parameter combinations, with a dual objective of minimizing RC delay and maximizing Ion/Ioff, critical metrics for device performance. The accelerated data generation enables a more extensive exploration of the solution space.

This research marks a transformative integration of ML in semiconductor engineering, underscoring its capacity to align with and contribute to ongoing technological advancements. The study positions ML as a key driver in the pursuit of precision and efficiency, paving the way for innovative solutions in semiconductor device design and optimization.

IV. CONCLUSION

Our study underscores the immense potential of Machine Learning (ML) in comprehending and optimizing semiconductor devices, with a specific focus on FinFETs and their I-V and C-V curves based on geometric parameters. The ML-based model introduced in our research emerges as a robust and reliable substitute for conventional simulation techniques, offering new avenues for forecasting and optimizing semiconductor device electrical performance. A key feature of our methodology is the integration of Design of Experiments (DOE), which not only simplifies the optimization process but also enhances predictive accuracy. This strategic integration allows for a more efficient exploration of the design space, improving the overall effectiveness of the optimization framework.

The adaptability of the ML-based model stands out as a crucial aspect, enabling the simultaneous management and optimization of multiple objectives. This characteristic proves particularly valuable when dealing with the intricate challenges associated with advanced semiconductor technologies, showcasing ML's flexibility in navigating complex design spaces.

Beyond immediate applications, our work signifies a broader shift in the paradigm of semiconductor engineering. Machine learning is portrayed as a dynamic solution capable of capturing the complex relationships within semiconductor devices. The success of our methodology suggests its potential applicability to a broader range of newly developed devices, positioning engineers and researchers at the forefront of technological advancement.

In conclusion, Machine Learning (ML) emerges as a powerful tool for accurately modeling FinFETs' I-V and C-V curves from geometric parameters, presenting a promising alternative to TCAD simulations. The ML-based device model not only streamlines performance optimization with multiple objectives but also holds promise for broader applications in the ever-evolving landscape of semiconductor technology. The adaptability and efficiency of ML make it a dynamic solution for accurate electrical performance prediction and optimization. This research lays the groundwork for a transformative integration of ML in semiconductor engineering, emphasizing its capacity to keep pace with and contribute to ongoing technological developments. The methodology's success positions ML as a versatile and indispensable tool, empowering engineers to navigate the evolving challenges of semiconductor design and contributing to the ongoing progression of technological frontiers.

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