International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 03 | March - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

A Review on Cascaded NTF Based SDM-ADC Design for VLSI Applications

Mukesh Ramani[1], Prof. (Dr.) Dolly Thankachan[2]

Abstract— Analog-to-digital converters are essential for the operation of digital circuits. Signals frequently exhibit fluctuation in response to the surrounding noise environment. Therefore, it is essential to build filters utilizing noise shaping and adaptive noise cancellation. These filters are termed adaptive filters and are utilized in applications necessitating real-time noise cancellation, such as speech processing and live video streaming. The document delineates the architecture of SDM ADCs utilizing recursive encoding. SDM ADCs are utilized to transform high bit-count, low-frequency digital impulses into lower bit-count, higher-frequency digital signals, facilitating the conversion of digital signals into analog within a digital-to-analog converter (DAC). The report examines the many methodologies employed to date, highlighting the advantages and disadvantages of each method. This paper presents the review of contemporary approaches in the domain.

Keywords— Analog to Digital Converters, Noise Estimation, Signal to Noise Ratio, Dynamic Range, Quantization Noise

I. INTRODUCTION

In order to catch up with the present day technology advancements, sigma-delta converters are used with an aim of high level of reliability and functionality with reduced chip cost [1]. It is applied in communication equipment, medical devices, automated production facilities, computers, weapons, navigation equipment, tools etc. Hence, if substantial analog signal processing (ASP) is performed, stochastic artifacts (noise) will accumulate, and the resulting signal may not represent the desired signal with the required significance needing adaptive filtering [2].

This paper focuses exclusively on the LMS algorithm and the delta-sigma modulation as chosen technique for adaptive filtering [3]. Based on the combination of oversampling and quantization error shaping techniques Delta -sigma modulator achieve a high degree of insensitivity to analog circuit imperfections, thus making them a appropriate choice to realize embedded analog-to-digital interfaces in modern systems-on-chip (SoCs) integrated in nanometer CMOS. Oversampling is inherently implemented in most sigma-delta (X-A) ADCs with integrated digital filters, where the modulator clock rate is typically 32 to 256 times the signal bandwidth, but X- *A* ADCs are limited for applications that require fast switching between input channels [4].

In medical applications multiple devices face the hurdle of SNR e.g. Electromyogram (EMG), Electrocardiogram (ECG), therefore the paper focuses on medical devices that require higher SNR to improve its performance. High-performance data-acquisition signal chains used in medical equipment require wide dynamic range and high accuracy [5].

II. WORKING

The basic structure of an adaptive noise filter can be implemented using the sigma delta modulation. A delta-sigma converter uses many samples from the modulator to produce a stream of l-bit codes. The delta- sigma ADC accomplishes this task by using an input- signal quantizer running at a high sample rate. The delta-sigma modulator takes an input and produces a stream of digital values same as other quantizers that represents the voltage of the input. The delta-sigma modulators are of two types the time and the frequency domain. An adaptive filter always has an error feedback loop often called the Sigma Delta Modulator. The modulator in Fig. l illustrates a first order sigma-delta modulator. It comprises of an integrator, a 1-bit quantizer, and a 1-bit DAC. The integrator ramps the input signals up and down. The integrator acts as the noise shaping circuit which shifts the noise from pass band to stop band. The output of the integrator is given to the comparator and then the comparator output is fed back through a 1-bit DAC to the Summing circuit. Oversampling is the process of taking more samples per second than required on the basis of the Nyquist-Shannon criterion. By changing the sampling rate the signal power and total quantization noise power is not affected. Therefore, the signal to quantization noise ratio is not changed.

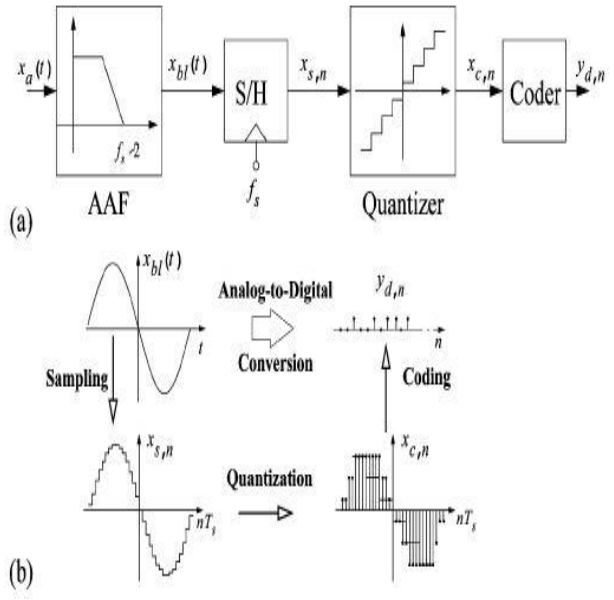

Fig.1 Basic Structure of an Adaptive Filter

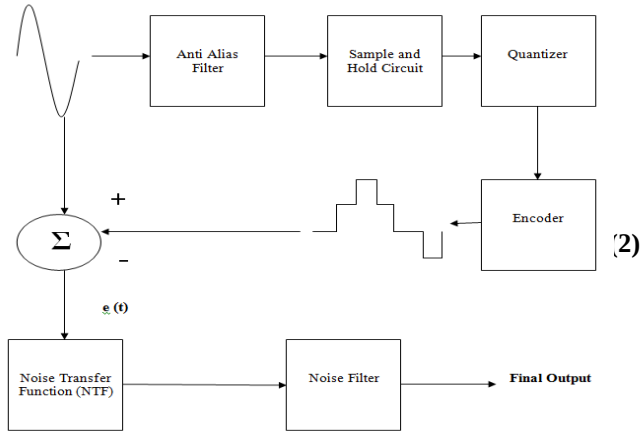

Fig.2 Structure of SDM

However, the quantization noise is spread over a larger frequency range, which reduces the spectral density of the quantization noise. The quantization noise power is reduced by 3 dB for every doubling of the oversampling ratio and the signal to quantization noise ratio is improved accordingly if the original Nyquist band is considered only. The oversampling ratio also affects the signal to noise ratio. If oversampling is increased, the signal to noise ratio is also increased exponentially.

III. PARAMETERS FOR ADAPTIVE FILTERING

(1) OVER SAMPLING RATIO:

When a significantly sampling frequency in a signal higher than the twice of bandwidth of digital samples known as Over sampling p, defined as

$$P = fs / 2B \quad (1)$$

Where fs is the sampling frequency, B is the bandwidth or highest frequency of the signal, the nyquist rate is 2B.

The theoretical limit of the SNR of Associate in Nursing ADC activity is predicated on the quantisation noise owing to the quantisation error inherent within the analog-to-digital conversion method once there's no oversampling and averaging. Since the quantisation error depends on the quantity of bits of resolution of the ADC the simplest case SNR is calculated as a perform of the Effective range of Bits

$$SNR= (6.02*ENOB) - 1.767 \quad (2)$$

for the Effective number of bits , using the measured SNDR

$$ENOB = SNDR - 1.76\ dB / 6.02dB/bit \quad (3)$$

Effective number of bits (ENOB) is simply the signal to noise-and-distortion ratio expressed in bits rather than decibels by solving the ideal SNR" equation. In the presentation of measured results, ENOB is identical to SNDR, with a change in the scaling of the vertical axis.

QUANTIZATION AND QUANTIZATION ERROR

It is bound by [-A/2 to +A/2] where A represents the amplitude of the analog signal [6].

$Qe_{(Max)} = \Delta/2$

Here Δ represents the step size.

(3) NOISE SHAPING:

The noise transfer function can be given by:

$$NTF\ (z) = (1 - z^{-1})\ L \quad (4)$$

Where L denotes the order of filter

(4) DYNAMIC RANGE:

Dynamic range is the parameter exhibiting the variation of the signal in the time domain. It is mathematically given by [7]:

$$A-(-A) = 2A \quad (5)$$

(5) FIGURE-OF-MERIT:

The figure of merit is the inverse of the signal to noise ratio and is given by

$$FOM = 1/ SNR \quad (6)$$

Comparison of the power efficiency of two AD converters that achieve identical signal conversion specifications, i.e. have the same sampling rate and realize the same SNR for every input signal, is an easy task; the one with the lowest power consumption is the best. Although the FoM of combining weight, (6) is wide used, it cannot be accustomed build honest comparisons between low resolution and high resolution AD converters. once the resolution of associate ADC is inflated, some extent is reached wherever thermal noise is limiting the SNR, so as to scale back the impact of the noise by three sound unit, capacitances have to be compelled to be doubled to extend the amount of effective bits by one, a six sound unit reduction of the noise is needed, which implies an element four increase in capacitance. Since power scales linearly with the quantity of capacitance to charge, the facility will increase with an element four. Thus, the FoM can become a minimum of an element a pair of worse once the ENOB is inflated by one.

The Error minimization gradient computed by the LMS algorithm is given by [8]:

$$\min E[z^2] = E[s^2] + \min E[(n_0 - y)^2] \quad (7)$$

IV. PREVIOUS WORK

This section puts forth the previous work in the domain and the attributes of each of the techniques used for noise shaping based Analog to Digital converter design.

Feyling at al. in [8] performed behavioral circuit simulations to compare the leapfrog control-bounded analog-to-digital converter with pertinent continuous-time sigma-delta modulators regarding nominal performance and susceptibility to component changes, clock jitter, and finite gain-bandwidth product. Simulations indicate that the nominal performance of the leapfrog is comparable to that of a continuous-time sigma-delta modulator with an identical loop filter order and the same quantization levels. Variations in components within the leapfrog's analog system will result in mistakes in the final output unless the coefficients of the reconstruction filter are adjusted correspondingly. Nonetheless, the straightforward, modular architecture, assurance of analytical stability, and single-bit quantizers render the leapfrog a compelling alternative to traditional continuous-time sigma-delta modulators.

S. Oh et al. in [9] proposed a pipelined NS-SAR ADC with 1-2 MASH structure is presented. Two-stage pipelined structure consisting of 5-bit NS-SAR and 4-bit NS-SAR ADCs shows 3 rd -order noise-shaping. To maximize power efficiency, a single operational transconductance amplifier (OTA) is reused for both an integrator for noise shaping and a residue amplifier for pipelining. The measured DR is 80dB when the sampling rate is 83.3MS/s and bandwidth is 6MHz, and power consumption is 3.5mW showing FoM s,DR of 172.3dB. The proposed ADC structure greatly relaxes design requirement of each SAR quantizer, and can achieve high resolution and wide bandwidth with good power efficiency.

Danesh et al. in [10] proposed a novel architecture for purely voltage controlled oscillator (VCO) based 1-1 MASH second-order analog-to-digital converter (ADC). Each stage of the MASH uses an open loop inverter based ring VCO. The proposed ADC uses phase information from all inverters in the VCO in both the MASH stages to perform efficient multi-bit quantization. A novel VCO quantization error extraction circuit is proposed to easily extract quantization noise of the first VCO stage. A gain calibration for the second stage of the ADC has been analyzed. Behavioral simulations have been performed to validate the proposed architecture.

P Payandehnia et al in [11] proposed a 3rd order SAR type ADC. The authors explained the concept that the practical implementation of the ADCs is done using digital filters. Higher order ADCs need to be implemented by designing higher order digital filters. The increasing order of digital filters makes the filters unstable thereby rendering instability to the ADC design. Thus there is a need for stability analysis of the ADC. A trade off between the stability and the performance of the ADC may also be observed. The stability analysis can be done using the bode plot (frequency domain analysis) or the pole zero plot in the s-plane. The authors finally resorted to a 3rd order Successive Approximation type ADC which was stable to the 3rd order.

Rudolf Ritter et al. in [12] presented a 70dB SNDR Continuous Time Delta-Sigma Modulator for industrial applications. It was explained by the authors that the removal of noise from the digitized counterpart of the original analog signal is often challenging owing to the act that the digitized form may have noise and disturbances in the same spectral band as that of the original signal. Hence it may be difficult to remove the noise and disturbances. Hence the way out is always to design a filter that would allow the digitized version of the signal and stop the noise and disturbances. This can be done by meticulous design of a filter that can be low pass, band pass or high pass based on the noise

characteristics. However, it is not necessary that the noise is completely removed from the signal. The proposed technique achieves a SNDR of 70dB which is relatively satisfactory.

S Tao et al. in [13] presented a power-efficient continuous-time incremental sigma-delta ADC. The authors mainly focused on the fact that incremental or higher order SDM based ADCs may be needed to attain high levels of signal to noise ratio. Often, a single stage SDM is not capable enough to render high values of signal to noise ratio. Hence a cascade of multi-level incremental SDMs need to be designed so as to remove the noise and disturbances in the signal with an incremental cascading approach. In this process the noise transfer function is evaluated in each of the stages and the noise shaping filter is iteratively designed in cascade. However, such a design may suffer from stability issues.

Angsuman Roy et al. in [14], designed a low power 2nd order sigma delta modulator for analog to digital conversion. In the proposed work, the authors showed that the amount of power consumption is a critical aspect for the analog to digital conversion process. The power consumptions should be as low as possible so as to practically implement the system as a system on chip (SOC) Excessive power may lead to high power dissipation and a cascading effect of increased power dissipation in the overall circuit which uses the ADC. Hence it is necessary to design the SDM with low power consumption. Hence the authors designed a passive low power SDM for analog to digital conversion.

L Hernandez at al. in [15] presented an analytical evaluation of VCO-ADC quantization noise spectrum. The authors showed that the analytical analysis of noise is necessary for the design of sigma delta modulators. The fundamental problem with the ADC design stands to be the fact that the noise creeps in due to the quantization process and the anti aliasing process. This necessitates the use of a technique to estimate the noise of the system output. This is done by using a comparator that compares the digital counterpart of the original signal and computes the difference among the two. The difference is termed as the spectral noise. Further the noise transfer function (NTF) is evaluated and then an appropriate filter is designed for the noise removal.

M De Bock et al. in [16] presented a calibration model for DAC Mismatch Errors in ADCs Based on a Sine-Wave Measurement. In the proposed work, the authors explained that there may be errors between the ADC design and the DAC design. The errors are needed to be removed since the original signal needs to be restored after the digital to analog conversion part. The errors are generally estimated first and then need to be compensated. This can be done through a dummy data training process for error estimation. The errors arise due to the process of analog to digital conversion and subsequently the signal processing in the digital to analog conversion. The authors have used a sine wave measurement technique for the purpose and have shown it to be effective for the mismatch compensation. ,

HC Tsai in [17] proposed an ADC design with Continuous-Time Modulator in 40-nm CMOS using Asynchronous SAR Quantizer and Digital Truncator. The authors explained that the fabrication level of the sigma delta modulator is also critical for the design and implementation of the ADCs. The fabrication is a main challenge with the constrains of size and dye area of the circuit affecting the performance of the overall ADC. It is often challenging to fabricate the circuit in a small technology (CMOS) technology. Increased size of the circuit dye area results in the clumsiness of the system to be a part of an system integration process. Hence the authors have fabricated the circuit on a 40nm CMOS technology.

V Srinivasan et al. in [18] proposed a 3rd-order continuous-time delta-sigma modulator clocked at 6GHz in 45nm CMOS. The authors explained that it is challenging not only to obtain a circuitry that is small in fabrication but also it should have a low response time. The main challenge is to make the system responsive enough to track fast changing analog signals. The parameter that is responsible for the determination of the speed at which the ADC responds is the clock frequency of the ADC. The higher frequency ADCs can perform quicker compared to the low frequency ADCs. In case the ADC works on low frequency, then there is always a definite chance that the ADC will miss out on the valuable and critical temporal variation of the signal and hence there will be a loss of data when the digital signal is again converted back to the analog counterpart of using the DAC process. The authors have meticulously designed the ADC on 45nm technology with a 6GHz frequency. The 6GHz frequency range is vital as it covers most of the useful physical signals.

B Jacob et al. [19] presented a multilevel inverter using the oversampling ADC. The authors showed that it is risk to sample an analog signal exactly at the Nyquist rate and it is possible that some sample may be missed or they do not render appropriate values. The

purpose then needs to be served using an oversampling ADC design and the rate at which the physical signal is sampled is more than the Nyquist rate. The factor governing the level of oversampling is the oversampling rate or oversampling ratio (OSR). Typically the value of SNR increases with increase in the OSR. The authors have implemented a multi level inverter using the oversampling rate (OSR) ADC [20].

The literature review throws light on the different challenges faced in ADC design with noise shaping and employing sigma delta modulation. The problem formulation in the next section is a derivative of the literature review.

Identified Research Gap

Based on the previous research approaches studied, the following points have been seen as gap or limitations in previous research:
1) A simultaneous or parallel analysis of OSR and SNR has not been done. The analysis is important since it gives an idea of the effect of the residual noise in the output of the ADC as the OSR keeps increasing.
2) The pole zero plot for higher order SDM based ADCs has not been analyzed. The frequency domain analysis in terms of bode plot has been done. The Pole-Zero plot gives a clear indication of exact amount of instability in the system.
3) Higher order SDM based ADCs have not been analyzed in general due to the fact that increasing the order of the digital filter renders instability to the system

V. CONCLUSION

This paper illustrates the fundamental techniques of noise shaping and noise filtering. The emphasis has been on the adaptive design parameters of filters. The essential elements of filter design and the associated parameters have been elucidated. A summary of current research in the topic has also been provided. The study is anticipated to facilitate research in the domain of adaptive filter design.

REFRENCES

[1] FanWenjie,LvQiuye,HeChong,YinLiang,Liu Xiaowei, “Architectural Design and Simulation of A Fourth-Order Sigma-Delta Modulator , International Journal, Key Engineering Materials Vols. 609-610 (2014) pp 723-727 , April 2014.

[2] Hetal Panchal, “Design and Simulation of Sigma Delta ADC Using VHDL AMS” , International Journal of Engineering Development and Research , Volume 2, Issue 1 ,pp no.548-551, 2014

[3] Liu Liang, Chen Song , He Chong, Yin Liang, Liu Xiaowei“Design of Third-order Single loop Full Feed-forward Sigma Delta Modulator”, International Journal, Key Engineering Materials Vols. 609-610 (2014) pp 1176-1180, April 2014

[4] RaminZanbaghi, Pavan Kumar Hanumolu “An 80-dB DR, 7.2-MHz Bandwidth Single OpampBiquad Based CT Modulator Dissipating 13.7-mW ”, IEEE Journal of Solid-State Circuits, Vol. 48, No. 2, pp 1 - 15, February 2013

[5] Jiandong Cheng, Guoyong Shi, and Ailin Zhang, “A Fast SNR Estimation Method for Sigma-Delta Modulator Design” , TENCON 2013, IEEE Conference, 22nd -25th October ,pp 1-4, 2013

[6] Philip M. Chopp and Anas A. Hamoui, “A 1-V 13-mWSingle-Path Frequency-Translating AZ Modulator With 55-dB SNDR and 4-MHz Bandwidth at 225 MHz” , IEEE Journal of Solid-State Circuits, Vol. 48, No. 2, pp 1-14 February 2013.

[7] T Bhatnagar, Manisha and Thankachan, Dolly. ‘Enhancing Security & QoS of Trust-enabled Wireless Networks Using Machine Learning Powered Transformable Blockchain Sharding’. DOI: 10.3233/JIFS-213482 Journal: Journal of Intelligent & Fuzzy Systems, vol. 44, issue no.-1 pp. 1-18, 2022.

[8] F. Feyling, H. Malmberg, C. Wulff, H. -. A. Loeliger and T. Ytterdal, "High-level Comparison of Control-Bounded A/D Converters and Continuous- Time Sigma-Delta Modulators, Submitted to Special Issue on IEEE Transactions on Circuits and Systems, September, 2022, pp.1-5

[9] S Oh, Y Oh, J Lee, K Kim, S Lee, J Kim, "A 80dB DR 6MHz Bandwidth Pipelined Noise-Shaping SAR ADC with 1–2 MASH structure," 2020 IEEE Custom Integrated Circuits Conference (CICC), 2020, pp. 1-4

[10] M. Danesh and A. Sanyal, "Fully Digital 1-1 MASH VCO-Based ADC Architecture," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), 2019, pp. 501-504

[11] P Payandehnia, H Mirzaie, H Maghami, J Muhlestein, “Fully passive third-order noise

shaping SAR ADC", Electronics Letters, IET Journal 2017

[12] Rudolf Ritter, John G. Kauffman, Joachim Becker, Maurits Ortmanns, "A 10 MHz Bandwidth, 70 dB SNDR Continuous Time Delta-Sigma Modulator With Digitally Improved Reconfigurable Blocker Rejection", IEEE 2016

[13] S Tao, A Rusu, "A power-efficient continuous-time incremental sigma-delta adc for neural recording systems", IEEE 2015

[14] Angsuman Roy and Jacob Baker, "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion", IEEE 2014

[15] L Hernandez, E Gutierrez, "Analytical evaluation of VCO-ADC quantization noise spectrum using pulse frequency modulation", IEEE 2014

[16] M De Bock, X Xing, L Weyten, G Gielen, "Calibration of DAC Mismatch Errors in ADCs Based on a Sine-Wave Measurement", IEEE 2013

[17] HC Tsai, CL Lo, CY Ho, YH Lin, "A 64-fJ/Conv.-Step Continuous-Time Modulator in 40-nm CMOS Using Asynchronous SAR Quantizer and Digital Truncator", IEEE 2013

[18] V Srinivasan, V Wang, P Satarzadeh, "A 20mW 61dB SNDR (60MHz BW) 1b 3rd-order continuous-time delta-sigma modulator clocked at 6GHz in 45nm CMOS", IEEE 2012

[19] B Jacob, MR Baiju, "Vector-quantized space-vector-based spread spectrum modulation scheme for multilevel inverters using the principle of oversampling ADC", IEEE 2012

[20] Yingqi Qian Changchun Zhang a, Zhongchao Liu, Leilei Liu, YurongLuan,Yuming Fang and Yufeng Guo," A High-Performance Sigma-Delta Modulator in 0.18pm CMOS Technology" International Journal, Applied Mechanics and Materials Vols. 519-520 (2014) pp 1085-1088, February 2014