A Review on FPGA-based Architectures for Noise Removal of Digital Images using High-Level Design

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Abstract— **Image corruption during the acquisition and transmission operations may be caused by a variety of disturbances. Scientists are still having trouble getting rid of the noise in the original picture. picture denoising is a technique used to improve a picture's visual quality and extract small details from a damaged image. Improving an image to make it crisper than it was originally is the aim of image restoration. The field of image processing is vast. This paper presents the results of some significant work in the subject of image denoising. It looks into image denoising using some of the most recent methods, such as SEPD (Simple Edge Preserved De-noising) and RSEPD (Reduced Simple Edge Preserved De-noising). Image corruption during the acquisition and transmission operations may be caused by a variety of disturbances. Scientists are still having trouble getting rid of the noise in the original picture. picture denoising is a technique used to improve a picture's visual quality and extract small details from a damaged image. Improving an image to make it crisper than it was originally is the aim of image restoration. The field of image processing is vast. This paper presents the results of some significant work in the subject of image denoising. It looks into image denoising using some of the most recent methods, such as SEPD (Simple Edge Preserved De-noising) and RSEPD (Reduced Simple Edge Preserved De-noising).**

Keywords— Power consumption analysis, Digital logic circuits, Ultra-low power, Subthreshold operation, Static CMOS gates

I. INTRODUCTION

In addition to storing, conveying, and expressing pictorial information for machine observation, digital image processing also improves human perception of that information, which makes it fascinating. In recent years, image processing has developed and become widespread in numerous scientific and technological domains. The primary objectives of image processing include acquisition, denoising, segmentation, feature extraction, and classification [1]. The term "image processing" describes the manipulation of digital images, which includes applying noise-filtering algorithms to eliminate aberrations and noise. During the production process or the transformation phase, the image may pick up noise or abnormalities. Removing unnecessary information from photographs, such as noise, is one of the main goals of this research. Filters are dissected at several pixel resolutions in the multi-resolution analysis. Filter components appear in various structures at different resolutions. As a result, it is feasible to separate the items in the filters. As a result, noise and flag in denoising problems can be isolated continuously, making noise removal especially easier [2]. In this study, it is suggested that denoising increases when a nonlinear flexible standard filter is used in a multi-resolution environment, first at full resolution and then at half resolution. This nonlinear handling approach is found to be useful in reducing Gaussian and Speckle noise as well as motivation disturbance. Nonlinear Flexible Averaging filters are proposed to always yield superior denoising. Furthermore, it is shown that the suggested method is also significant for denoising shading filters [3]. A novel

Flexible Averaging filter is suggested for picture de-noising through FPGA implementation. Although they have a greater execution cost, adaptive averaging filters have superior separation properties over conventional filters. High detection pixels might now be isolated once every second thanks to throughput improvements made to the recommended configuration. The flexible filter that filters distinguishable filter pixels is displayed to the best execution/value extent. Versatile filters can also be employed as detectors of debased filter pixels in addition to filtering.

Energy dissipation plays a crucial role in VLSI design, and energy consumption is given special significance by sub micrometer and nanoscale approaches. Interest in low-power goods has increased due to the growing popularity of battery-operated portable devices and the emphasis on energy conservation in embedded circuits. Knowing the power characteristics of digital logic circuits in static CMOS gates is crucial since operating these circuits at subthreshold voltages drastically lowers power usage.

This study investigates and evaluates the energy-use behavior of digital logic circuits inside static CMOS gates when they are functioning in the subthreshold range. The study intends to illustrate the efficiency and trade-offs of subthreshold logic circuits in comparison to conventional CMOS techniques by thoroughly assessing energy consumption.

VLSI engineering typically concentrates on low power consumption and little complexity. Regardless, the Simple Edge Preserved De-noising (SEP) approach produced a large area at a high power, low recurrence, and high cost. Thus, RSEPD (Reduced Simple Edge Preserved De-noising) has been introduced as a countermeasure. However, this tactic was unable to alter the enormous yield esteem. The difference in power and territory compared to SEPD was negligible. This encourages the use of the suggested approach with the assistance of CSLA (carry select adder). Compared to the current framework, this adder fundamentally focuses on recurrence while offering less territory and power. Moreover, VLSI engineering uses a variety of filters to remove driving noise from images. The purpose of the 3 x 3 sliding window is to identify pixels, regardless of whether they are quiet or noisy, in order to convey the difference between the center display and the focal pixel. In the filtering process, middle noiseless pixels are the norm rather than disturbance pixels [6]. The dim level of respect varies from 0 to 255. The numbers "0" and "255" stand for pepper and salt, respectively. VLSI engineering is responsible for the central filter, enroll bank, line support, drive finder, and choice tree. The sophisticated images cannot be prepared simply in VLSI strategy. An increase is observed in the existing de-noising strategy's execution with the aid of pipelined design.

NOISE SOURCES

Variations between the ideal signal generated by our model and the real-world signals are referred to as noise. Different detector sensitivity levels, sporadic radiation, shifting ambient conditions, and issues with transmission or digitization are only a few of the causes of noise. The number of damaged pixels affects the image's noise level. Among the main reasons why digital images contain noise are:

1. The imaging sensor is affected by environmental conditions.
2. image deterioration due to the transmission medium.
3. Low-light noise and sensor-derived temperature measurements.
4. Particles of dust on the scanning screen.
5. Blur brought on by motion, sluggish shutter rates, or miss-focusing.
6. Modes with great sensitivity and low light.

TYPES OF NOISE

Different strategies are needed to remove noise, which is a significant problem in image processing, especially in image restoration and enhancement. The primary sources of noise are the digital image acquisition and transmission operations. This article focuses on several types of noise and its sources, including:

- Impulse noise
- Gaussian noise
- Exponential noise
- Quantization noise
- Rayleigh noise
- Poisson noise (Photon Noise)

NOISE LEVEL ESTIMATION METHODS

The majority of methods for calculating noise level presume that signals are unaffected by stationary, zero-

mean white Gaussian noise. There are two categories of noise estimating methods available today:

- Block-oriented Noise Approximation
- Filter-based Estimation of Noise
- Texture-based Estimation of Noise

NOISE REMOVING FILTERS

Because of its simple mathematical structure and a number of desirable qualities, linear filters were originally the main tools used to remove noise from digital photographs. On the other hand, linear filters are not very effective when noise is not an additive problem, non-Gaussian statistics, or nonlinearities in the system. Because nonlinear digital filters perform better at removing impulse noise and preserving edges, they are extensively utilised in many different fields.

Linear Filters

Because of their strong theoretical underpinnings and computing efficiency, linear filters have gained popularity. They function best when the spectrum of the target signal can be distinguished clearly from noise. However, impulsive noise cannot be eliminated by linear filters, and they have a tendency to blur edges. The following are some instances of linear filters:

- Sobel Filter
- Gaussian Filter
- Laplacian Filter
- Unsharp Filter
- Log Filter
- Prewitt Filter
- Wiener Filter

Non-Linear Filters

The drawbacks of linear filters were addressed with the development of nonlinear filtering. Though they lack a unifying theory, nonlinear filters can be devised and implemented without the need for sophisticated optimisation techniques. Typical nonlinear filter types are as follows:

- Morphological Filter
- Homomorphic Filter
- Polynomial Filters
- Order Statistics Filters

Proposed Filters

The suggested noise removal filters distinguish between noisy and noise-free pixels using a new method. The LCEPD method with CSLA has the advantage of boosting frequency while decreasing space and power consumption. As a component of the multiresolution structure, the Flexible Average Filter (FAF) enhances common picture denoising and visual quality. When leveraging VLSI execution for image denoising, the suggested FAF structure offers reduced power consumption and takes up very little space. Performance is assessed using statistical metrics such as Mean Square Error (MSE) and Peak Signal to Noise Ratio (PSNR), which demonstrate that the suggested filter delivers greater accuracy with reduced size, power, and delay consumption.

FPGA-based Multiresolution Flexible Averaging Filter

The extensive usage of FPGAs in image processing applications is made possible by the ongoing advancements in programmable device technology. utilising an array architecture-based hardware technique, entire path planning is done utilising the binary picture of the environment. Path planning procedures are decomposed into simple local neighbourhood tasks, generating the processing element of an architecture. The array can operate at high speeds and is adaptable to hold photos of any size.

Filters in multiresolution analysis are dissected at different pixel resolutions. Filter components exhibit varying resolutions over many structures, enabling the separation of signal and noise. In a multiresolution setting, denoising is enhanced by using a nonlinear adjustable standard filter, especially for impulse, Gaussian, and speckle noise. Better denoising is achieved using nonlinear flexible averaging filters, which are especially useful for colour filter denoising. For filter denoising, a new flexible averaging filter with better qualities than current filters is suggested to be implemented on FPGA.

PERFORMANCE MEASUREMENT

Performance metrics evaluate an algorithm's compliance with requirements such as robustness and accuracy. Algorithm testing offers a comparison against similar algorithms as well as a quantitative or qualitative rating. Common performance indicators include of:

- Accuracy: the algorithm's success rate in relation to a benchmark.
- Robustness: The ability of an algorithm to tolerate different circumstances.
- Sensitivity: the algorithm's sensitivity to subtle feature changes.
- Adaptability: The technique's approach to handling image variability.
- Reliability: the extent to which an algorithm produces the same outcome when run again with the same stable data.
- Efficiency: the algorithm's (time and space) feasibility in practice.

II. RELATED WORKS

This section examines a number of well-known denoising algorithms as well as the uses, problems, and future prospects of filtering methods. It also covers VLSI systems, FPGA systems, and Carry Select Adder approaches.

In order to eliminate spatial bias, Kandemir et al. (2015) presented the Unbiased Weighted Mean Filter, which involves recalibrating the contribution figure of each clean pixel in order to remove high-density impulsive noise. Phase space reconstruction theory and Chaos theory were applied by Dahai Xia et al. (2013) to analyze electrochemical potential noise. In order to efficiently detect and eliminate impulse noise, Dawood et al. (2014) introduced the Weber's law Noise Identifier (WLNI). Self-checking carry-select adders were implemented by Dilip Vasudevan et al. (2007) for high-speed, low-cost processing. Adaptive thresholding was suggested by Chipy Ashok et al. (2015) for FPGA solutions in picture denoising. In 2015, Avinash et al. proposed a low-power DWT method for low-speed applications.

By shutting off such blocks when computations are not needed, Avinash et al. (2015) [15] suggested a solution to reduce power consumption for a valued DAA approach that employs expensive resources to perform a level-1 DWT. Because of its lower throughput, it is appropriate for low-speed applications; nonetheless, low-speed applications are typically low-cost applications. For the specified 8-bit accuracy, the maximum inaccuracy in the output is 9.58%. Keeping in mind the previous information, the level-1 DWT system can be used to generate further DWT levels iteratively. There are certain benefits to this tactic over the convolution-based method. It is very parallelizable, for instance.

S. No.	Title	Year	Methodology	Advantage	Limitation
1	An FPGA-based design for a real-time image denoising using approximated fractional integrator	2020	Approximated fractional integrator	Real-time processing capability	Complexity in implementation
2	FPGA Based Denoising Method with T-Model Mask Architecture Design for Digital Images	2020	T-Model Mask Architecture	Improved denoising accuracy	Increased hardware resources
3	A real-time video denoising algorithm with FPGA	2020	Spatiotemporal Gaussian scale mixture model	Effective noise removal in video	High computational load

	implementation for Poisson–Gaussian noise			streams	
4	An efficient FPGA based de-noising architecture for removal of high density impulse noise	2021	Median type filters	Efficient removal of high-density impulse noise	Loss of fine image details
5	Design and analysis of improved high-speed adaptive filter-based denoising architectures	2021	Adaptive filter architectures	High-speed processing	Limited to specific noise types
6	Noise Removing Filters and Its Implementation on FPGA	2021	Gaussian, Mean, and Median filters	Versatile noise removal	Susceptibility to memory bit flips
7	Design and FPGA Implementation of an Efficient Architecture for Noise Removal in Biomedical Devices	2021	Lifting-based wavelet denoising	Simplified design process	Limited to biomedical applications
8	A High-Level Synthesis Implementation and Evaluation of an Image Processing Accelerator	2022	High-Level Synthesis (HLS)	Simplified design process	Dependency on HLS compiler efficiency
9	Design and evaluation of a hardware/software FPGA-based system for fast image processing	2022	Gaussian 3×3 kernel	Fast processing speed	Limited scalability
10	An Efficient Denoising Architecture for Removal of Impulse Noise in Images	2023	Decision-tree-based impulse noise detector	Low complexity	May not handle all noise types effectively

Table 1: Showing Recent works on FGPA

III. FPGA IMPLEMENTATION OF MULTIRESOLUTION FLEXIBLE AVERAGING FILTER

For improved denoising, the suggested methodology makes use of a flexible averaging filter in a multiresolution setting. This filter's FPGA implementation offers reduced size and power consumption thanks to performance optimisation. When compared to current filters, the suggested FAF structure performs better in terms of denoising and visual quality. VLSI engineering frequently prioritises low power

consumption and a little-multifaceted nature. The SEPD (Simple Edge Preserved De-noising) approach produced only large areas, at a significant cost, with higher power and lower recurrence. Therefore, a method called RSEPD (Reduced Simple Edge Preserved De-noising) has been presented to overcome this. However, this tactic was unable to alter the enormous yield esteem. Only a few minor adjustments to power and territory were examined compared to SEPD. Central filter, enrol bank, line support, drive finder, decision tree, and other components are examples of VLSI engineering in action. The advanced images cannot be prepared directly in VLSI strategy. Increase the current de-noising strategy's execution with the aid of pipelined design.

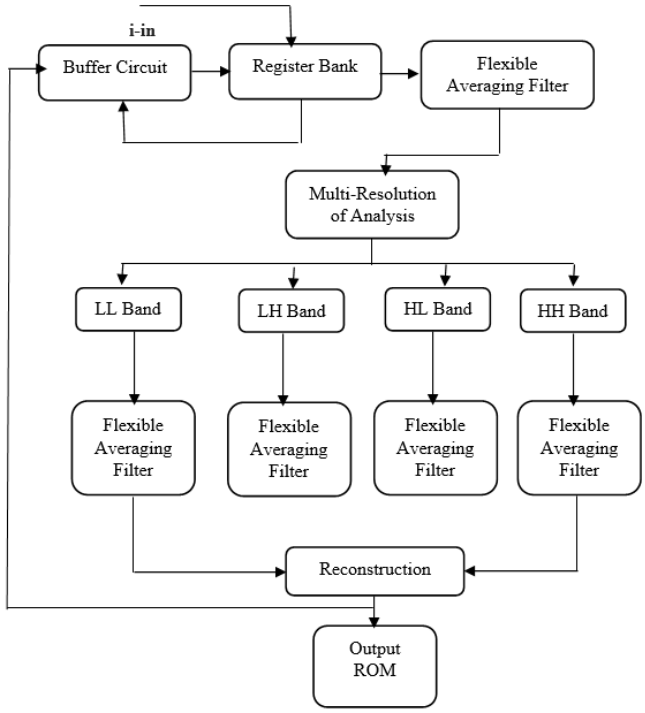

Figure 1: Flowchart of Proposed Methodology

The block diagram that displays (Figure 1) explains how to apply the recommended picture denoising computing method. The buffer circuit connects to the enrolling bank and maintains it. The enrollment bank is made up of the collection of registers. The pertinent data might be sent to a fantastic information finder in order to determine the largest and lowest value. During the denoising stage, a flexible averaging filter (FAF) is employed.

The two modules that comprise the suggested flexible average filter are the average generator (AG) and the min-ED generator. Figure 2 depicts the construction of the min-ED generator, which is used to identify the edge with the least contrast. We employ twelve |SUB|, four ADD, and four shifter units to calculate eight directional contrasts. The Min Tree unit is used in this instance to determine which is the smallest. There are several comparators that make up the Min Tree. From there, the pixels from the normal generator that make the least directional distinction (Dmin) can be obtained by taking the mean of the brightness estimations of the pixels, as seen in Figure 3.

In this diagram, all multipliers will be replaced by shifters to lower the equipment cost. We combine items b, d, e, and g into one group. The second and third values, labelled as SortFour2, SortFour3, and the final value, $\hat{f}$i,j, are produced from the condition as follows: when the recreated value fi,j received from the edge-saving filter is compared,

$$\hat{f}i,j = \begin{cases} SortFour2, & if\ (SortFour2 > \hat{f}i,j) \\ SortFour3, & if\ (SortFour3 < \hat{f}i,j) \\ \hat{f}i,j, & Otherwise \end{cases}$$

DWT Algorithm:

Step1: First, the input image is transformed from a colour image to a grayscale image [3].

Step2: The entire image is separated into chunks measuring 32 by 32 pixels.

Step3: After that, each block of 32x32 blocks is subjected to 2D-DWT, producing four details (LL, LH, HL, HH).

• LL - shows the approximate image at the nth level of decomposition, which is the outcome of both vertical and horizontal low-pass filtering.

• LH - depicts the horizontal features at the nth level of decomposition, which are acquired by applying vertical high-pass and horizontal low-pass filters.

• HL - shows the vertical details/edges that were retrieved at the nth level of decomposition using both horizontal high-pass and vertical low-pass filtering.

• HH - indicates the diagonal features gained from high-pass filtering in both directions at the nth level of decomposition.

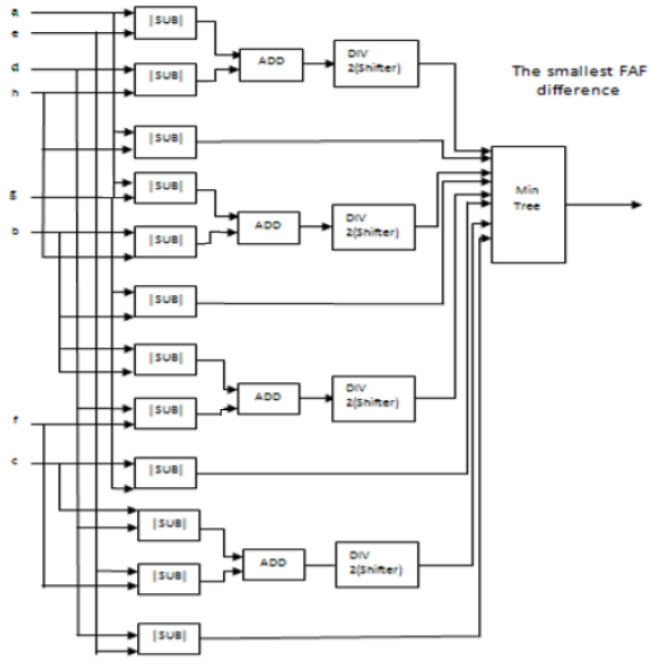

Figure 2: Architecture of Min ED Generator

Step4: After undergoing further transformation via 2DWT, the four subband details yield an additional four sub-bands of 16x16 blocks.

Step5: The 16x16 block is broken down using the steps above to create a new set of four subbands or details that are 8 by 8.

Step6: Once four 8x8 blocks have been obtained, calculate the discrete wavelet transform coefficients for each block. After quantizing these coefficients, they are sent for coding.

Step7: To create a whole image, repeat the process.

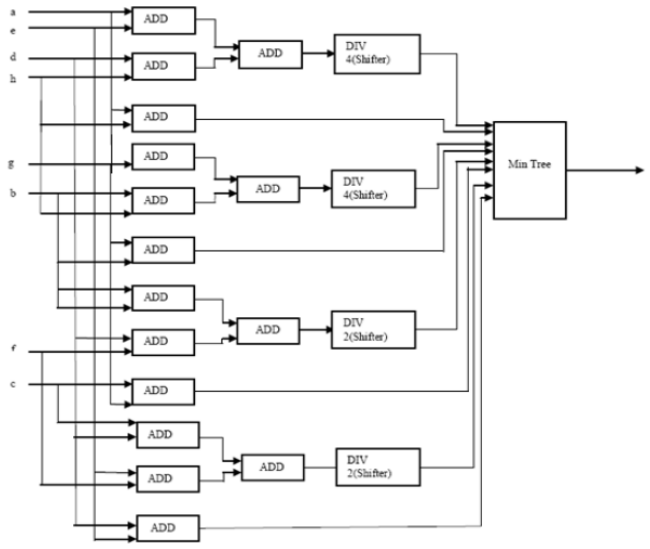

Figure 3: Architecture of Average Generator

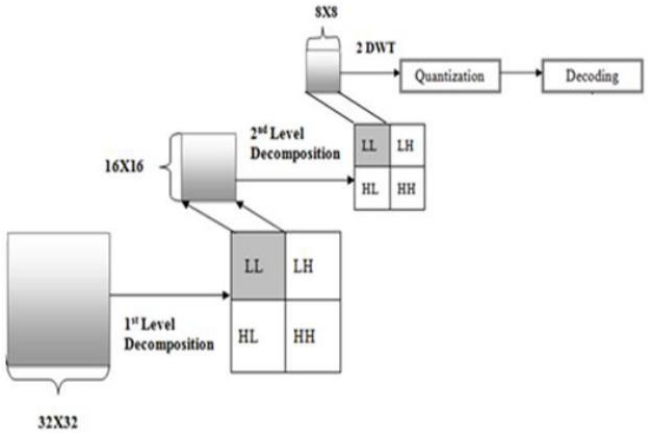

Figure 4: Methodology of DWT

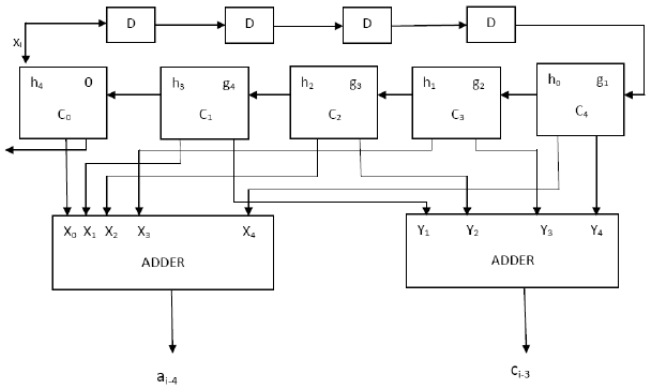

Figure 5: Multiresolution utilizing DWT Design

Wavelet transformation is not able to account for certain issues, however wavelet-based multiresolution analysis can be helpful in removing erroneous point objects and negative esteem coefficients (Figure 5). These issues motivate the creation of further multiresolution tools, such as the multiresolution analysis intermediate filter and the recommended approach going forward [16]. When used on the Sxy rectangle, this filter works well. In certain cases, this filter changes Sxy's size while it is filtering. The methodology of the proposed filter is described as follows:

$$Zmin = \min pixel\ in\ Sxy$$
$$Zmax = \max pixel\ in\ Sxy$$
$$Zmed = \text{median}\ pixel\ in\ Sxy$$
$$Smax = \max allowable\ size\ of\ Sxy$$

There are two layers to this filtering technique. Level A and Level B might be used to indicate it.

Level A:

If (Zmin < Zmed < Zmax),

Zmed is not noise to Level B for testing Zxy is noise

Else
Zmed = Noise
1. Enhance window-size
2. Repeat Level A till….
Zmed = not a Noise.

Level B:
If (Zmin < Zxy < Zmax),,
Zxy = not a Noise
Output = Zxy
Else
Zxy = A Noise
Output = Zmed

Impulse noise can originate from both positive and negative impulses; positive impulses usually have maximum values recorded, whereas negative impulses usually have minimum values. If Zmin, Zmed, and Zmax are not identified as noise, it advances to Level B. The following is the basic idea of Level B: To ascertain if Zxy is noise or not, it is evaluated. Zmed will replace it if it's a noisy [17]. In any other scenario, Zxy is not identified as a noise. After filtering, Zxy is still present in the image. Hence, unless the pixel in question has noise, the pixel value in the filtered image is comparable to that of the input image. This can stop information from being lost needlessly.

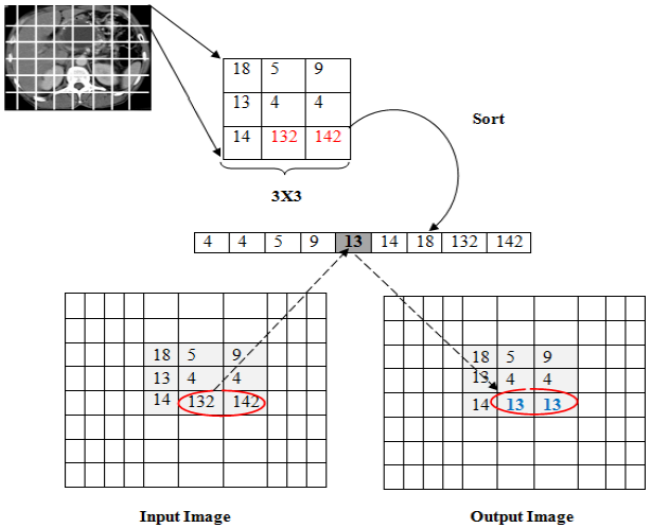

Figure 6: Proposed Methodology

The proposed filter method is depicted in Figure 6 and the hardware implementation of the multiresolution flexible averaging filter is shown in the Figure 7,

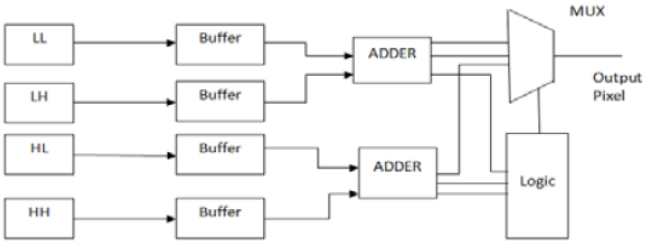

Figure 7: Hardware Implementation of the Proposed Filter

IV. RESULTS AND DISCUSSION

The Flexible Averaging filters described in VHDL were modelled using Model Sim and synthesized for the Virtex-II Pro XC2vp50-7FPGA using Xilinx ISE tools. The cost of installation is minimal. This is expressed using slices. The solutions are able to calculate 300 million times per second throughput. of the suggested approach, we can filter about 280 photos per second when we look at an image of 1024 × 1024 pixels. Figures 8 and 9 depict the original and several output images produced by different image denoising algorithms, respectively.

Table 1: PSNR of FAF

Noise Density (%)	SPED	RSPED	Proposed FAF
10	42.4	43.5	47.6
20	40.2	40.5	45.6
30	36.8	38.5	43.4
40	35.8	36.2	42.7
50	33.4	35.6	41.1
60	32.7	33.4	40.2
70	30.6	31.7	36.1
80	28.6	29.1	34.8
90	25.7	26.4	32.1

The suggested FAF method generated less space complexity than other methods, as seen by Figure 10, which compares the power consumption and area occupied by the various methods.

Table 2: MSE of FAF

Noise Density (%)	SPED	RSPED	Proposed FAF
10	0.024	0.022	0.020
20	0.039	0.037	0.032

30	0.052	0.050	0.047
40	0.065	0.062	0.060
50	0.082	0.080	0.076
60	0.098	0.094	0.088
70	0.112	0.105	0.102
80	0.125	0.120	0.112
90	0.148	0.145	0.139

It is also reported to be able to significantly reduce motivation clamour and to a manageable degree reduce Gaussian and Speckle noise. The computation performs comparably well for photos with shading and darkness. For picture de-noising using VLSI execution, the suggested FAF structure offers low power consumption and takes up less space. Tables 1 and 2, respectively, display the assessment metrics of the multiresolution averaging filter in terms of PSNR and MSE values.

V. CONCLUSION

When digital images are processed by an electronic system and sent via a communication channel, they are frequently contaminated by undesired noise components. This corruption might manifest in different ways. When images were being transferred via noisy channels, impulse noise happened. Several filters are studied in order to further increase performance.

This research introduces various unique filtering algorithms based on FPGA and VLSI that can suppress noise without compromising important image properties. It has been discovered that the multiresolution structure's use of the FAF filter results in more common image denoising and improved visual quality. For picture de-noising using VLSI execution, the suggested FAF structure offers low power consumption and takes up less space..

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