

A Review on Higher Order Continuous-Time Sigma-Delta Modulators for ADC Design

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Abstract—In this paper, the concept of adaptive filtering has been proposed. It has been shown that signals often undergo variation in the noise environment encountered. Hence it becomes mandatory to design filters based on noise shaping and adaptive noise cancellation. Such filters are called adaptive filters and are used for applications requiring real time noise cancellation such as speech processing, live video broadcasting etc. The paper presents the structure of Sigma Delta or MASH ADCs which employ recursive encoding. SDM ADCs are also used to convert high bit-count, low-frequency digital signals into lower bit-count, higher-frequency digital signals as part of the process to convert digital signals into analog as part of a digital-to-analog converter (DAC). The paper focuses on the various approaches used thus far for the purpose, citing the pros and cons of each approach.

Keywords— Adaptive Filter Design, Noise Filtering, Sigma Delta Modulator (SDM), MASH, Signal to Noise Ratio.

I. INTRODUCTION

In order to catch up with the present day technology advancements, sigma-delta converters are used with an aim of high level of reliability and functionality with reduced chip cost. It is applied in communication equipment, medical devices, automated production facilities, computers, weapons, navigation equipment, tools etc. Hence, if substantial analog signal processing (ASP) is performed, stochastic artifacts (noise) will accumulate, and the resulting signal may not represent the desired signal with the required significance.[1] needing adaptive filtering.

This paper focuses exclusively on the LMS algorithm and the delta-sigma modulation as chosen technique for adaptive filtering. Based on the combination of oversampling and quantization error shaping techniques Delta -sigma modulator achieve a high degree of insensitivity to analog circuit imperfections, thus making them a appropriate choice to realize embedded

analog-to-digital interfaces in modern systems-on-chip (SoCs) integrated in nanometer CMOS. Oversampling is inherently implemented in most sigma-delta (X-A) ADCs with integrated digital filters, where the modulator clock rate is typically 32 to 256 times the signal bandwidth, but X- A ADCs are limited for applications that require fast switching between input channels.

In medical applications multiple devices face the hurdle of SNR e.g. Electromyogram (EMG), Electrocardiogram (ECG), therefore the paper focuses on medical devices that require higher SNR to improve its performance. High-performance data-acquisition signal chains used in medical equipment require wide dynamic range and high accuracy.

II. WORKING

The basic structure of an adaptive noise filter can be implemented using the sigma delta modulation. A delta-sigma converter uses many samples from the modulator to produce a stream of 1-bit codes. The delta- sigma ADC accomplishes this task by using an input- signal quantizer running at a high sample rate. The delta-sigma modulator takes an input and produces a stream of digital values same as other quantizers that represents the voltage of the input. The delta-sigma modulators are of two types the time and the frequency domain. An adaptive filter always has an error feedback loop often called the Sigma Delta Modulator. The modulator in Fig. 1 illustrates a first order sigma-delta modulator. It comprises of an integrator, a 1-bit quantizer, and a 1-bit DAC. The integrator ramps the input signals up and down. The integrator acts as the noise shaping circuit which shifts the noise from pass band to stop band. The output of the integrator is given to the comparator and then the comparator output is fed back through a 1-bit DAC to the Summing circuit. Oversampling is the process of taking more samples per second than required on the basis of the Nyquist-Shannon criterion. By changing the sampling rate the signal power and total quantization noise power is not affected. Therefore, the signal to quantization noise ratio is not changed.

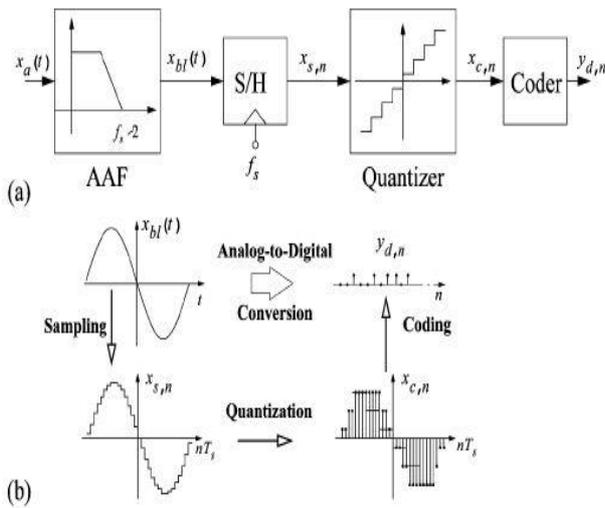


Fig.1 Basic Structure of an Adaptive Filter

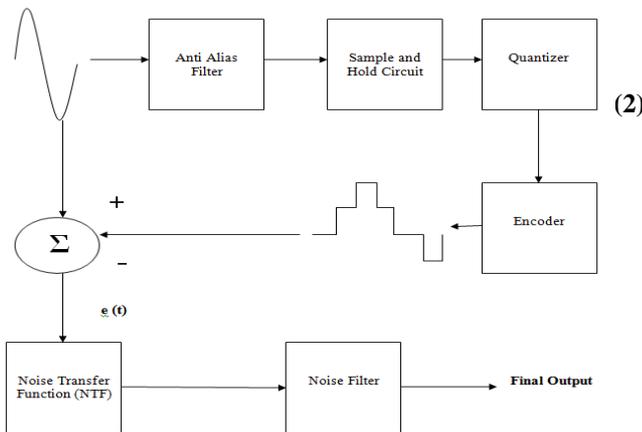


Fig.2 Structure of SDM

However, the quantization noise is spread over a larger frequency range, which reduces the spectral density of the quantization noise. The quantization noise power is reduced by 3 dB for every doubling of the oversampling ratio and the signal to quantization noise ratio is improved accordingly if the original Nyquist band is considered only. The oversampling ratio also affects the signal to noise ratio. If oversampling is increased, the signal to noise ratio is also increased exponentially.

III. PARAMETERS FOR ADAPTIVE FILTERING

(1) OVER SAMPLING RATIO:

When a significantly sampling frequency in a signal higher than the twice of bandwidth of digital samples known as Over sampling p, defined as

$$P = f_s / 2B \tag{1}$$

Where f_s is the sampling frequency, B is the bandwidth or highest frequency of the signal, the nyquist rate is $2B$. [2]

The theoretical limit of the SNR of Associate in Nursing ADC activity is predicated on the quantisation noise owing to the quantisation error inherent within the analog-to-digital conversion method once there's no oversampling and averaging. Since the quantisation error depends on the quantity of bits of resolution of the ADC the simplest case SNR is calculated as a perform of the Effective range of Bits

$$SNR = (6.02 * ENOB) - 1.767 \tag{2}$$

for the Effective number of bits, using the measured SNDR

$$ENOB = SNDR - 1.76 \text{ dB} / 6.02 \text{ dB/bit} \tag{3}$$

Effective number of bits (ENOB) is simply the signal to noise-and-distortion ratio expressed in bits rather than decibels by solving the ideal SNR" equation [7] In the presentation of measured results, ENOB is identical to SNDR, with a change in the scaling of the vertical axis.

QUANTIZATION AND QUANTIZATION ERROR

It is bound by $[-A/2 \text{ to } +A/2]$ where A represents the amplitude of the analog signal.

$$Q_{e(\text{Max})} = \Delta/2$$

Here Δ represents the step size.

(3) NOISE SHAPING:

The noise transfer function can be given by:

$$NTF(z) = (1 - z^{-1})^L \tag{4}$$

Where L denotes the order of filter

(4) DYNAMIC RANGE:

Dynamic range is the parameter exhibiting the variation of the signal in the time domain. It is mathematically given by:

$$A - (-A) = 2A \tag{5}$$

(5) FIGURE-OF-MERIT:

The figure of merit is the inverse of the signal to noise ratio and is given by

$$FOM = 1 / SNR \tag{6}$$

Comparison of the power efficiency of two AD converters that achieve identical signal conversion specifications, i.e. have the same sampling rate and realize the same SNR for every input signal, is an easy task; the one with the lowest power consumption is the best. Although the FoM of combining weight, (6) is wide used, it cannot be accustomed build honest

comparisons between low resolution and high resolution AD converters. once the resolution of associate ADC is inflated, some extent is reached wherever thermal noise is limiting the SNR, so as to scale back the impact of the noise by three sound unit, capacitances have to be compelled to be doubled to extend the amount of effective bits by one, a six sound unit reduction of the noise is needed, which implies an element four increase in capacitance. Since power scales linearly with the quantity of capacitance to charge, the facility will increase with an element four. Thus, the FoM can become a minimum of an element a pair of worse once the ENOB is inflated by one.

The Error minimization gradient computed by the LMS algorithm is given by:

$$\min E[z^2] = E[s^2] + \min E[(n_0 - y)^2] \quad (7)$$

IV. PREVIOUS WORK

This section puts forth the previous work in the domain and the attributes of each of the techniques used for noise shaping based Analog to Digital converter design.

Feyling et al. presented the behavioural circuit simulations used to compare the leapfrog control-bounded analog-to-digital converter to relevant continuous-time sigma-delta modulators in terms of nominal performance and sensitivity to component variations, clock jitter and finite gain-bandwidth product. Simulations show that the nominal performance of the leapfrog is similar to that of a continuous-time sigma-delta modulator of the same loop filter order and with the same number of quantization levels. Component variations in the leapfrog's analog system will introduce errors in the final output, unless the coefficients of the reconstruction filter are modified accordingly. Nevertheless, the simple, modular structure, analytical stability guarantee and single-bit quantizers make the leapfrog an interesting alternative to conventional continuous-time sigma-delta modulators.

Vardhini et al. proposed that various signal processing applications incorporated sigma delta ADC among different analog to digital converters because of its digital dominant architecture. This paper presents the design of a low pass continuous time sigma delta analog to digital converter on-chip architecture with a very few passive components connected externally to FPGA suitable for signal processing applications, wireless application, sonar and radar beamforming. Schematic level architecture of high speed comparator working at a differential swing which is not allowed by FPGA standard differential pads is designed. Analysis illustrates that proposed on-chip continuous-time

sigma-delta analog to digital converter exhibits a sampling rate of 400 MHz designed with high speed comparator with varied differential swing. Output data rate of 1 MHz with a dynamic range of 72 dB is achieved with less bill of material that suites for signal processing applications.

S. Oh et al. proposed a pipelined NS-SAR ADC with 1-2 MASH structure is presented. Two-stage pipelined structure consisting of 5-bit NS-SAR and 4-bit NS-SAR ADCs shows 3rd -order noise-shaping. To maximize power efficiency, a single operational transconductance amplifier (OTA) is reused for both an integrator for noise shaping and a residue amplifier for pipelining. The measured DR is 80dB when the sampling rate is 83.3MS/s and bandwidth is 6MHz, and power consumption is 3.5mW showing FoM s,DR of 172.3dB. The proposed ADC structure greatly relaxes design requirement of each SAR quantizer, and can achieve high resolution and wide bandwidth with good power efficiency.

Danesh et al. proposed a novel architecture for purely voltage controlled oscillator (VCO) based 1-1 MASH second-order analog-to-digital converter (ADC). Each stage of the MASH uses an open loop inverter based ring VCO. The proposed ADC uses phase information from all inverters in the VCO in both the MASH stages to perform efficient multi-bit quantization. A novel VCO quantization error extraction circuit is proposed to easily extract quantization noise of the first VCO stage. A gain calibration for the second stage of the ADC has been analyzed. Behavioral simulations have been performed to validate the proposed architecture.

Eric Gutierrez et al. proposed a Pulse Frequency Modulation Interpretation of VCOs. The authors used the concept of noise shaping. The authors explained that in the process of analog to digital conversion, there are various steps involved such as sampling, quantization and encoding. The processes render certain amount of noise and error effects in the output of the analog to digital converter (ADC). The overall effect in the output of the analog to digital converter's response can be marred by noise and disturbance effects which may tend to reduce the signal to noise ratio of the ADC overall. The effect would be a less reliable digitized counterpart of the analog signal. Hence, it is necessary to employ extended noise shaping in the circuit level implementation.

P Payandehnia et al. proposed a 3rd order SAR type ADC. The authors explained the concept that the practical implementation of the ADCs is done using digital filters. Higher order ADCs need to be implemented by designing higher order digital filters.

The increasing order of digital filters makes the filters unstable thereby rendering instability to the ADC design. Thus there is a need for stability analysis of the ADC. A trade off between the stability and the performance of the ADC may also be observed. The stability analysis can be done using the bode plot (frequency domain analysis) or the pole zero plot in the s-plane. The authors finally resorted to a 3rd order Successive Approximation type ADC which was stable to the 3rd order.

Rudolf Ritter et al. presented a 70dB SNDR Continuous Time Delta-Sigma Modulator for industrial applications. It was explained by the authors that the removal of noise from the digitized counterpart of the original analog signal is often challenging owing to the fact that the digitized form may have noise and disturbances in the same spectral band as that of the original signal. Hence it may be difficult to remove the noise and disturbances. Hence the way out is always to design a filter that would allow the digitized version of the signal and stop the noise and disturbances. This can be done by meticulous design of a filter that can be low pass, band pass or high pass based on the noise characteristics. However, it is not necessary that the noise is completely removed from the signal. The proposed technique achieves a SNDR of 70dB which is relatively satisfactory.

S Tao et al. presented a power-efficient continuous-time incremental sigma-delta ADC. The authors mainly focused on the fact that incremental or higher order SDM based ADCs may be needed to attain high levels of signal to noise ratio. Often, a single stage SDM is not capable enough to render high values of signal to noise ratio. Hence a cascade of multi-level incremental SDMs need to be designed so as to remove the noise and disturbances in the signal with an incremental cascading approach. In this process the noise transfer function is evaluated in each of the stages and the noise shaping filter is iteratively designed in cascade. However, such a design may suffer from stability issues.

Roy et al. designed a low power 2nd order sigma delta modulator for analog to digital conversion. In the proposed work, the authors showed that the amount of power consumption is a critical aspect for the analog to digital conversion process. The power consumptions should be as low as possible so as to practically implement the system as a system on chip (SOC) Excessive power may lead to high power dissipation and a cascading effect of increased power dissipation in the overall circuit which uses the ADC. Hence it is necessary to design the SDM with low power consumption. Hence the authors designed a passive low power SDM for analog to digital conversion.

L Hernandez et al presented an analytical evaluation of VCO-ADC quantization noise spectrum. The authors showed that the analytical analysis of noise is necessary for the design of sigma delta modulators. The fundamental problem with the ADC design stands to be the fact that the noise creeps in due to the quantization process and the anti aliasing process. This necessitates the use of a technique to estimate the noise of the system output. This is done by using a comparator that compares the digital counterpart of the original signal and computes the difference among the two. The difference is termed as the spectral noise. Further the noise transfer function (NTF) is evaluated and then an appropriate filter is designed for the noise removal.

M De Bock et al. presented a calibration model for DAC Mismatch Errors in ADCs Based on a Sine-Wave Measurement. In the proposed work, the authors explained that there may be errors between the ADC design and the DAC design. The errors are needed to be removed since the original signal needs to be restored after the digital to analog conversion part. The errors are generally estimated first and then need to be compensated. This can be done through a dummy data training process for error estimation. The errors arise due to the process of analog to digital conversion and subsequently the signal processing in the digital to analog conversion. The authors have used a sine wave measurement technique for the purpose and have shown it to be effective for the mismatch compensation. ,

HC Tsai et al. proposed an ADC design with Continuous-Time Modulator in 40-nm CMOS using Asynchronous SAR Quantizer and Digital Truncator. The authors explained that the fabrication level of the sigma delta modulator is also critical for the design and implementation of the ADCs. The fabrication is a main challenge with the constraints of size and dye area of the circuit affecting the performance of the overall ADC. It is often challenging to fabricate the circuit in a small technology (CMOS) technology. Increased size of the circuit dye area results in the clumsiness of the system to be a part of a system integration process. Hence the authors have fabricated the circuit on a 40nm CMOS technology.

The literature review throws light on the different challenges faced in ADC design with noise shaping and employing sigma delta modulation. The problem formulation in the next section is a derivative of the literature review.

Identified Research Gap

Based on the previous research approaches studied, the following points have been seen as gap or limitations in previous research:

- 1) A simultaneous or parallel analysis of OSR and SNR has not been done. The analysis is important since it gives an idea of the effect of the residual noise in the output of the ADC as the OSR keeps increasing.
- 2) The pole zero plot for higher order SDM based ADCs has not been analyzed. The frequency domain analysis in terms of bode plot has been done. The Pole-Zero plot gives a clear indication of exact amount of instability in the system.
- 3) Higher order SDM based ADCs have not been analyzed in general due to the fact that increasing the order of the digital filter renders instability to the system

V. CONCLUSION

In this paper the basic approach of noise shaping and noise filtering have been illustrated. Focus has been on the adaptive design parameters of filters. The critical aspects of filter design along with the relevant parameters have been explained. A summary of contemporary work in the field has also been explained. It is expected that the paper would pave the path for research in the relevant field of adaptive filter design.

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