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A Review on VLSI Aspects of Error Detection and Correction on SOCs

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Abstract :- **The implementation of error detection and correction codes on system on chip (SOC) is one of the key challenges in VLSI design owing to the fact that SOCs are often limited in terms of computation power and memory. Turbo codes is a category of error detection and correction codes which have moderate complexity but exhibit a steep descent in the error floor. The name is derived from the fact that two decoders try to simultaneously decode the encoded sequence of bits synonymous with the turbo engines. This paper presents a VLSI perspective and comprehensive review on need of error detection and correction. The emphasis has been laid on the error detection and correction employing the turbo encoding mechanism. The turbo encoding mechanism has been chosen as the baseline technique as it shows adherence to the Shannon's limit while exhibiting a steep plummet in the error rate, in the error rate even at low SNR values. The important features of the turbo encoding-decoding process has been cited with explanations. A review of the various categories of turbo codes and similar approaches has been presented. Salient features of contemporary work have been cited.**

Keywords: Very Large Scale Integration (VLSI), Error Detection and Correction, Trustworthiness, Turbo Codes, Shannon's Limit.

I. INTRODUCTION

Error detection and correction are fundamental concepts in digital systems, especially in VLSI design where numerous components are densely integrated on a single chip [1]. The goal is to identify and rectify errors that may arise due to various factors, including electromagnetic interference, manufacturing defects, or radiation-induced faults [2]. Implementing robust error detection and correction mechanisms is crucial for the overall reliability and performance of VLSI circuits [3]. VLSI circuits can be susceptible to different types of errors, such as single-bit errors, multiple-bit errors, and intermittent faults [4]. Single-bit errors involve the corruption of a single binary digit, while multiple-bit errors affect more than one bit simultaneously [5]. Intermittent faults are transient and may occur sporadically due to external factors. Understanding the nature of these errors is essential for selecting appropriate error detection and correction techniques [6].

Error detection and correction (EDC) in VLSI (Very Large Scale Integration) implementations is a critical aspect of designing reliable digital systems. EDC techniques are employed to ensure that data integrity is maintained in the presence of transient or permanent errors that can occur during data transmission or storage [7].

II. VLSI IMPLEMENTATION OF ERROR DETECTION AND CORRECTION CODES

Error correction techniques go a step further by not only detecting errors but also correcting them. Hamming codes, Reed-Solomon codes, and Bose-Chaudhuri-Hocquenghem (BCH) codes are examples of error correction codes used in VLSI designs. These codes introduce redundancy into the data, allowing for the identification and correction of errors. The choice of a specific error correction code depends on factors such as the desired level of error correction and the available resources on the VLSI chips [8].

Error detection techniques aim to identify the presence of errors within the system. Common methods include parity checking, cyclic redundancy check (CRC), and checksums. Parity checking involves adding an extra bit to each data word, ensuring that the total number of set bits is either even (even parity) or odd (odd parity). CRC involves generating a polynomial code based on the data, and checksums involve calculating a sum or checksum value to verify data integrity. [9]

One of the ways to do the same is the design of error detection and correction codes which are able to pick up the errors in the received data at

the receiving end and also able to correct them. Of several mechanisms to correct the errors, one of the most potent coding techniques is the turbo encoding mechanism [8]. The turbo encoding mechanism exhibits extremely good error plummeting performance in the waterfall region of the error rate curve analysis with steep fall in the error rates even for low value of signal to noise ratio. This is typically useful for IoT and Fog frameworks as the devices are often constrained in terms of the processing power leading to limited encoding options and also as the media is unguided, the path loss factor results in the reduction in the signal strength resulting in the low value of signal to noise ratio. The double whammy exists in the case of high noise and disturbance effects in the channel leading to distortions in the received SNR values. Thus a fall in the error rate for lower values of SNR in the case of turbo decoding is extremely useful and makes the technique feasible for application in real time applications [10].

Without loss of generality, it can be stated that Turbo Codes are very close to Shannon's limit mathematically defined as [11]:

$$C = Blog_2(1 + \frac{S}{N}) \quad (1)$$

Here,
C is channel capacity
S is signal power
N is noise power
B is bandwidth

The Shannon's limit is BER of almost 10^{-5} (ideally 0) for $\frac{E_b}{N_0}$ = 0 dB for binary modulation.

A typical example where the turbo encoder and decoder are used is depicted in the Fig.1:

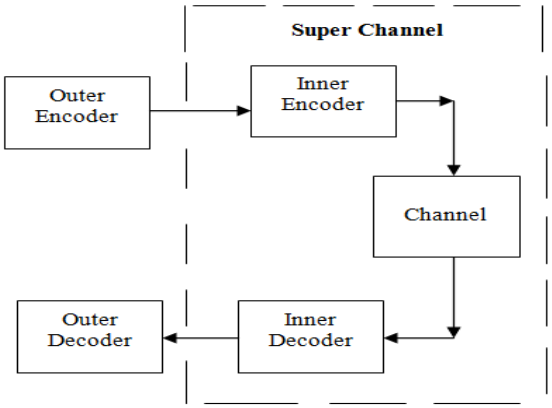

Fig.1 Encoder-Decoder Structure

a. Turbo Encoding

The turbo encoding can be thought of as a two-step process comprising of the inner encoder and the outer encoder.The inner encoder, channel and outer encoder is often termed as the super channel. Fig.2 exhibits the structure of the coding mechanism. The above limit corresponds to a binary rate R=1/2 convolution encoder which has a constraint length K and memory M=K-1.

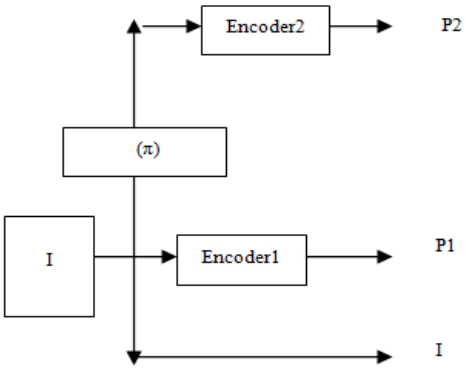

Fig.2 Structure of Turbo Code Encoder

The turbo encoding can be thought of as a two-step process comprising of the inner encoder and the outer encoder.[12]. The inner encoder, channel and outer encoder is often termed as the super channel. The encoder may have to identical encoding blocks which result in the system being termed as a symmetric encoding structure [13]. The essence of the encoding approach lies in the fact that there are two encoders generating two parallel parity bit streams. Additionally, the unaltered bit stream which is the actual data is also

transmitted. The parity bits P1 is the output of the encoder 1 while the parity bit P2 is the output of the encoder 2. The interleaver is responsible for the re-arrangement of the bits (information bits) prior to feeding the encoder 2. Thus three parallel bit streams are generated which passes through the channel and the decoder has the job of identifying the actual bit stream with an accurate guess so as to manage low values of error rate at the decoding end and this would lead to high trustworthiness in the system [14].
Assuming that the bit d_k is the input to the encoder at time k, we have the codeword C_k which is binary coupled:[2]

$$X_k = \sum_0^{k-1} g1_i d_{k-1} \mod 2\ g1_i = 0,1 \quad (2)$$

$$X_k = \sum_0^{k-1} g2_i d_{k-1} \mod 2\ g2_i = 0,1 \quad (3)$$

Where,

$$G_1 : \{g_{1i}\} \quad (4)$$
$$G_2 : \{g_{2i}\} \quad (5)$$

G1, G2 are two code generators generally expressed in the octal form.
The Convolutional encoders are used in a parallel structure with an interleaver to introduce randomness [15].

b. Turbo Decoding
The turbo decoded comprises of two decoders, akin to the encoder to perform the exactly reverse operation. The interleaver is represented by (π) and the de-interleaver is represented by (Dπ) [16]

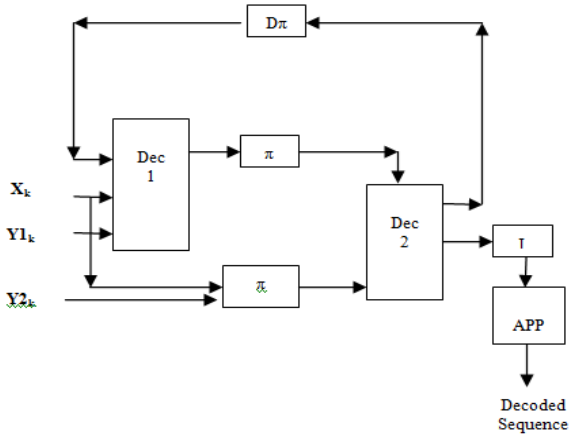

Fig.3 Structure of Turbo Decoder

The different blocks used in the decoding mechanism are:
1) Decoding block 1.
2) Decoding block 2.
3) Interleaver.
4) De-Interleaver.
5) Aposteriori probability estimator.
6) Probability threshold block.
7) Information bits.
8) Parity bits.

For a random channel, the turbo decoder is made up of the random variables x_k and y_k defined mathematically as [17]:

$$x_k = (2d_k - 1) + i_k \quad (6)$$
$$y_k = (2Y - 1) + q_k \quad (7)$$

Here,
k is the time index
i_k and q_k are independent noises in the channel with noise variance σ^2

III. PREVIOUS WORK
This section presents the salient features of the previous work done in the domain.

Mahdavi et al. proposed that spatially coupled serially concatenated codes (SC-SCCs) are constructed by coupling several classical turbo-like component codes. The resulting spatially coupled codes provide a close-to-capacity performance and low error floor. Authors present VLSI architectural templates and explore them based on building blocks linking architectural templates with the new algorithms.

Zhao et al. proposed a Markov based method with superposition. This would yield the parity generation with recursion (PrBMST-LDPC). The approach was to reduce the complexity of the recursive approach to generate the parity and non-parity bits so as to make it feasible for low complexity implementation.

Chen et al. presented about the Polar Codes attracting concern and attention in the recent times. Especially in the forthcoming 5G wireless networks their adoption and use has been garnering attention.

Moloudi et al. proposed coding techniques with spatial connection. The codes are concatenated codes with the information bits spatially connected. This is shown to reduce the error rate in the waterfall region.

Cai et al. put forth the block Markov superposition transmission of BCH (BMST-BCH) codes, that can be made to get a very low and reduced error floor measure.

Liva et al. enunciated the block codes design for the brief data blocks i.e. for less than thousand data bits. It is a problem that has been an active research area that has garnered importance due to latest technical developments in the wireless communication networks.

Arıkan et al. explained the "turbo revolution" could be considered as successors to the low density parity check (LDPC). The channel coding area has seen a lot of modernization and technical advancements in the recent couple of years. made significant improvement.

Boulat et al. proposed a mechanism on encryption based security types. It is useful as it can secure against decoding that is unauthorized. But lesser possibility of interception is mainly ensured by strong communication. model that showed good results.

Babar et al. discussed the area of high detection intricacy that has been the chief challenge in the nearby future. The Gigabit frameworks have to be strongly handled and improvised in order work in tandem with other structures and types of domain. Here a quantum based detector can go a long in getting the outcomes right on time. It can detect signals in the range of hundreds attributing to its parallel working feature.

IV PROBLEM IDENTIFICATION

Designers often face trade-offs between the level of error correction, hardware complexity, and performance. Optimization strategies involve choosing the most suitable error detection and correction techniques based on the specific application's requirements. Trade-offs may include sacrificing a degree of error correction for reduced hardware complexity or vice versa. Advanced optimization techniques, such as parallel processing and pipelining, can also be employed to enhance the efficiency of error detection and correction in VLSI implementations.

Implementing error detection and correction in VLSI poses challenges such as limited space, power constraints, and the need for real-time processing. Designers must strike a balance between the complexity of error correction codes and the available resources. Additionally, the choice of coding scheme may vary based on the specific application requirements, as different applications may prioritize low latency, low power consumption, or high reliability differently.

Conclusion: This paper presents a comprehensive review on the need for trustworthiness in IoT and Fog networks. The introduction to error detection and correction pertaining to the trustworthiness of large scale wireless networks and IoT networks has been presented. Moreover, it has been shown that due to the effectiveness of Turbo Codes and their adherence to Shannon's limit, they are the most suitable for high data rate networks. Previous work and their significant contribution have been cited and explained. This paper paves the path for future advancements in the domain of design of turbo codes for wireless IoT and Fog networks.

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