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A Spatially Coupled Structure of Turbo codes for VLSI-SoC Applications

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Abstract: The chip level implementation of error detection and correction codes is a challenging aspect for VLSI systems as the system complexity often makes it infeasible for systems to be implemented within the constraints of memory and processing speed. One of the most effective techniques for error detection and correction happen to be the turbo codes. The turbo codes have two encoders and two decoders working in synchronization to perform the error detection and correction mechanism. In this paper, a cascading and sharing of bits is proposed to implement error detection and correction in systems which can be implemented on system on ship (SoC). It has been shown that the proposed system attains lesser error rate at moderate iterations as compared to exiting research work.

Keywords: SoC, Error Detection and Correction, VLSI, iterations, cascaded bits.

I. INTRODUCTION

All communications work on binary transmission in the present world. Hence devising mechanisms for error detection and correction is necessary to enhance the reliability of data transfer. Moreover, over the last decade, the upsurge of internet of things (IoT) has led to investigation of systems which can render high reliability. Over the last few years, the vision of the Internet of Things (IoT) has become a reality:

all over the world, billions of wireless sensors gather and transmit data about all facets of our lives [1], from Smart City applications such as live road traffic and parking spot mapping to industrial ones such as the structural monitoring of buildings and bridges, or even environmental ones such as weather and pollution measurement. In this context, the traditional Internet packet structure can become inefficient: the short length of the packet payload makes the overhead from protocol headers become more significant [2], and channel codes need to be designed for the short packet regime [3]. However, IoT sensors have some common features that can be exploited to increase transmission efficiency: as the processes they monitor are often slow-varying and highly correlated in time [4], [5], they can be represented with Hidden Markov Models (HMMs) [6]. The overall objective of this work is to show how learnable features of the source can decrease the communication requirements as learning progresses and a Markov source is one of the simplest ways to show this effect. The standard approach to exploit some regularities in the source data is is source compression [7]: as packets are highly correlated in time, the sensed data can be compressed using previously transmitted data as a reference, reducing the amount of data sent with no loss of accuracy [8]. However, compression-based schemes have two drawbacks: firstly, they need to be shared by both endpoints of the communication. . Unlike narrowband IoT (NB-IoT) standard where the whole data block will be retransmitted repeatedly until the data are recovered successfully, the proposed TLRCM works in a rateless manner and can achieve a smooth rate adaptation to channel variations, reducing the number of symbols to be retransmitted. Thus, TLRCM can significantly reduce the power consumption of IoT device and improve transmission throughput [9]. To reduce computational complexity, a 1-b subtraction and memory reading algorithm, which can be easily implemented in limited computing capability IoT devices, is proposed for the generation of TLRCM symbols.

II. TURBO ENCODING

The encoding structure is based on the cascaded encoders which the turbo encoding mechanism employs. The structure comprises of two cascaded convolution encoders shown in figure 1.

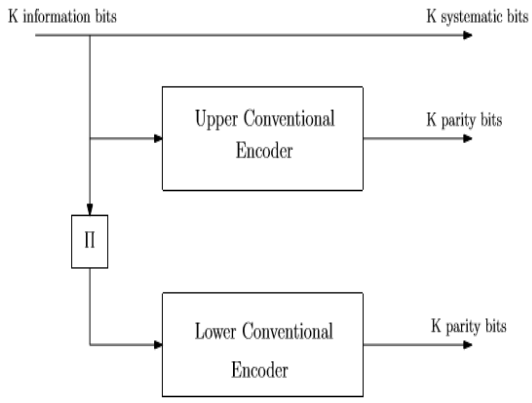

Fig.1 Turbo Encoder

The system comprises of the upper and lower encoders with an interleaver between them. The interleaver is used to reduce the chances of burst error between the transmission and receiving ends.

The interleaver structure is depicted in figure number 2. The block interleaver shown in figure 2 is row wise write and column wise read interleaver.

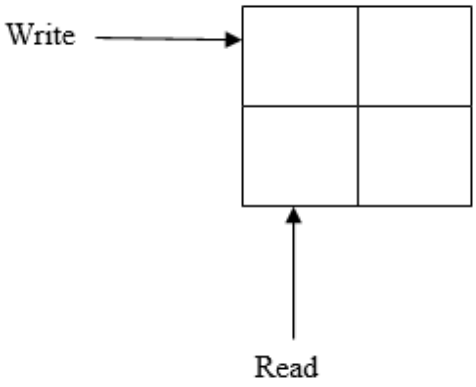

Fig.2 Block Interleaver structure

III. TURBO DECODING

The decoder can also be adapted to exploit information from previous packets, obtaining the Maximum A Posteriori (MAP) decoding: the optimal Low Density Parity Check (LDPC) decoder for Markovian sources was derived in [9]. In the case of variable length encoding [10], the source-aware decoder becomes more efficient in the case of long symbol sequences, as its does not increase the size of the decoding trellis. If the Markov model is not known at the beginning, the authors of [11] propose an implementation of Irregular Repeat Accumulate (IRA) codes that can take into account its learned transition probability in the message passing process. In this work, we take a similar approach: by modeling the temporally correlated source as an HMM, we can gradually learn the statistics of the underlying process at the receiver side, allowing a MAP decoding of messages sent over a noisy channel. Instead of compressing messages to remove redundant information (i.e., the correlation between subsequent packets), we exploit it at the receiver side to improve decoding, and puncture short Bose-Chaudhuri-Hocquenghem (BCH) codes [12] to increase efficiency. BCH is a practical explicit coding scheme, which can give better results with compression schemes than the short packet coding bounds, which are not associated with a practical code construction. Recent forecast estimates that the number Internet of Things (IoT) connections will reach 22 billions worldwide, including cellular IoT as well as short range IoT. The latter one are nowadays most common and use local area network techniques such as Wifi, Zigbee or Bluetooth to connect to an access point (typically a smartphone or a box) to access the wider network. Over the past few years, new approaches often referred as Low Power Wide Area (LPWA) networking technologies have emerged from the shadow to provide direct connectivity between the objects and the Network. Proprietary solutions were defined such as Sigfox, LoRa or other [13] while the cellular industry mandated the 3GPP to define optimized solutions for IoT. As a result, the LTE category 1 specifications were frozen offering a low-end LTE category for machine type communication (MTC), and two main lower categories were standardized in context of Release 13: LTEM and Narrow Band IoT (NB-IoT). These two categories were defined with aggressive objectives in terms of battery life, cost, extended coverage, while maintaining the benefits of cellular systems, such as security, coverage, quality of service or mobility [14]. The decoding structure is based on the recursive SOVA algorithm. For each step or iteration ‘k’. the following steps are implemented.

$$P(0) = P(1): apriori\ at\ k = 1 \quad (1)$$

Here,
P denotes the probability
Apriori is the probability of occurrence of bit to be 0 or 1 initially.
For each iteration beyond 1,

$$O_{D1} \overset{over\ k}{\longleftrightarrow} O_{D2} \forall K = k \geq 1 \qquad (2)$$

Here,
O_{D1} denotes output of decoder 1.
O_{D2} denotes output of decoder 2.
k are the iterations.

The decoder structure is depicted in figure 3.

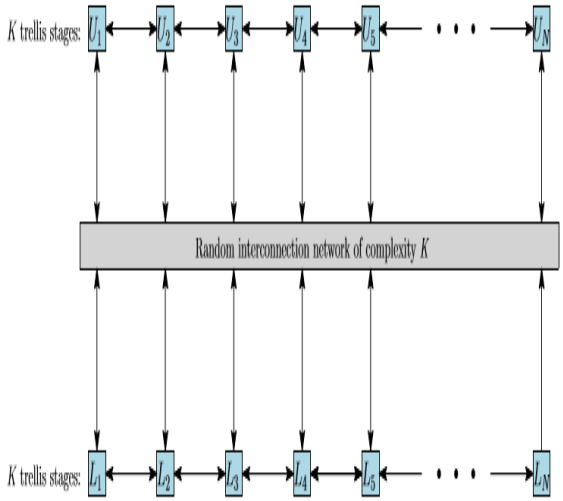

Fig.3 The turbo decoder structure.

To reduce the transmission rate, the concept of puncturing is employed, in which either of the parity bits are suppressed so as to reduce the bits which need to be sent [15].

Bit	TX (Y/N)	TX (Y/N)	TX (Y/N)
I	Y	Y	Y
P1	Y	N	Y
P2	N	Y	N
	Time=t1	Time=t2	Time=t3

Fig.4 Puncturing

The proposed system needs to implement the multiple blocks of codes which are to be employed over the entire bit stream. The proposed system for a stream of bits is depicted in figure 5.

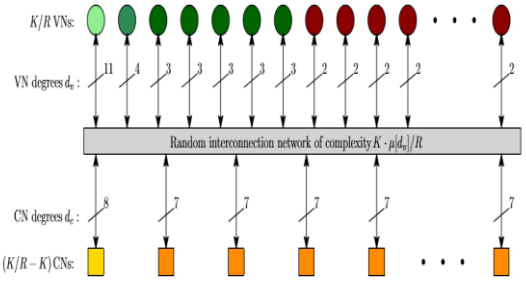

Fig.5 Bit Stream Structure for decoder.

The proposed system has a cascade structure for the bits in which the parity and information bits are cascaded as:

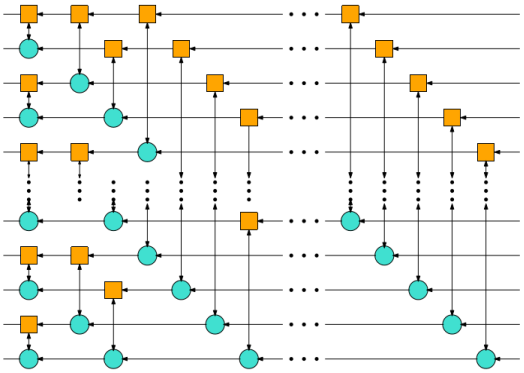

Fig.6 Cascading bit stream.

The adjacent bit streams are cascaded in this case. The cascade of the bit streams form a transport block. The cascade of non-adjacent blocks makes the system complexity lesser compared to the cascade of adjacent blocks.

IV RESULTS AND DISCUSSIONS

The system designed starts off with generation of random binary data stream of 1s and 0s. To emulate a practical situation, noise has been added to the bit stream.

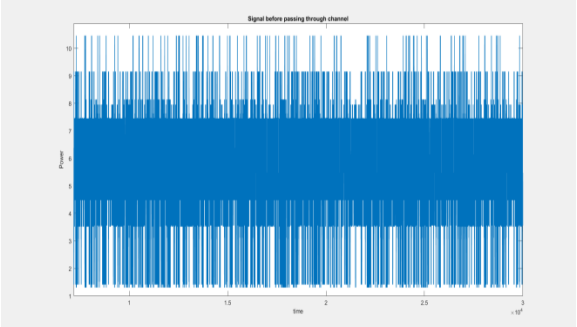

Fig.7 Binary Data

Figure 7 depicts the binary data generated and to be transmitted.

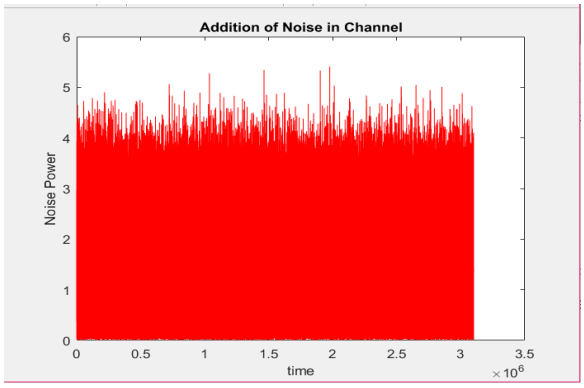

Fig.8 Noise added to bit stream

Figure 8 depicts the noise added to the binary data stream.

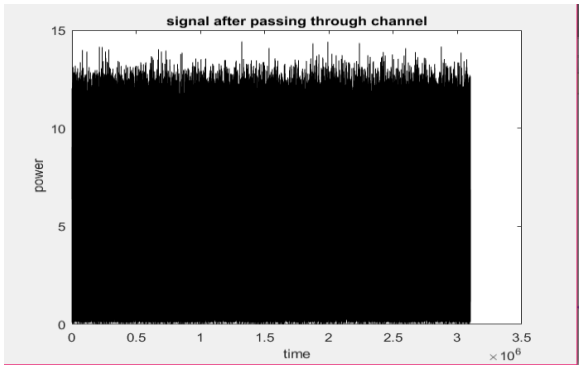

Fig.9 Bit Stream after noise

Figure 9 depicts the data stream after noise addition.

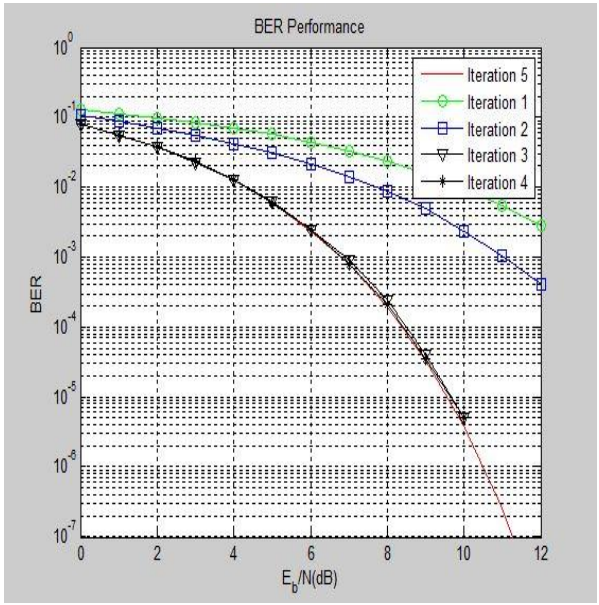

Fig.10 Error rate of system

Figure 10 depicts the error performance of the proposed system, as a function of iterations.

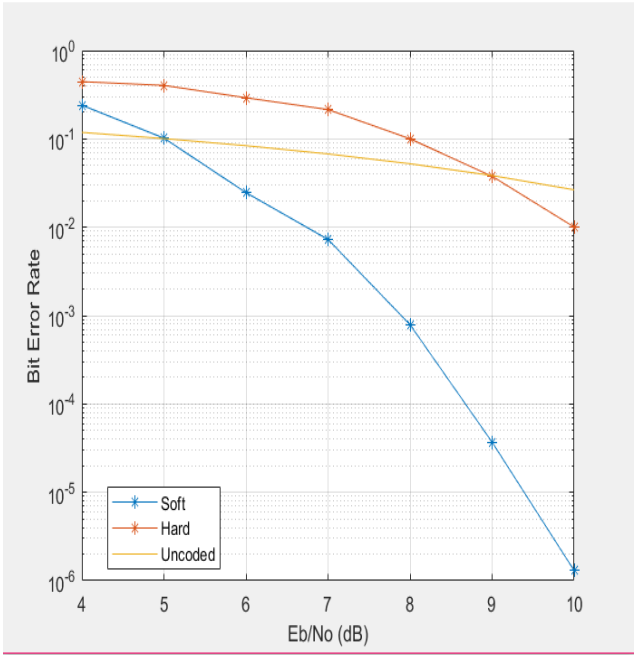

Fig.12 Error rate comparison

Figure 12 depicts the conditions of error rate with no, soft and hard coding techniques employed.

It can be observed that the soft coded SOVA algorithm performs better than the uncoded and hard coded versions.

Conclusion:

This paper presents a SoC based implementation mechanism for the error detection and correction of turbo codes with moderate number of iterations and low error rates. The cascaded structure of the system allows adjacent blocks to be coupled with each other so as to share information among the sub-code blocks of the transport blocks. The error rate of the system is used to evaluate the performance of the proposed system. It can be observed that the proposed system outperforms the hard coded and the un-coded version of the bit streams for the on chip implementation. The low or moderate number of iterations signify that the system complexity is less to be implemented as a VLSI-SoC model.

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