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A Study of Boundary Scan Testing

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Abstract –

With the rise of integration density at chip level, the controllability and observability of defects become difficult, leading to restricted physical probe access to I/O pins. It is impractical to test all the input pins and capture outputs from output pins on a chip among a computer circuit board (PCB). Boundary scan may be a useful methodology to test with reduced physical probe access to IC pins on complicated PCBs.

This paper gives the detailed study of boundary scan testing and its functions associated with Test Access Port (TAP). It also explains the boundary scan instructions and the signals through the TAP controller. Supports the applications of testing the devices on various factor using JTAG standard.

***Key Words*: JTAG, TAP, Boundary Scan, Device Under Test.**

1.INTRODUCTION

Testing of a circuit has been part of VLSI technology from the terribly starting. From the first style to the final production of a VLSI device, faults and errors might happen in each stage. several testing ways are fictitious, aimed at the rising new VLSI technology throughout the past few decades.

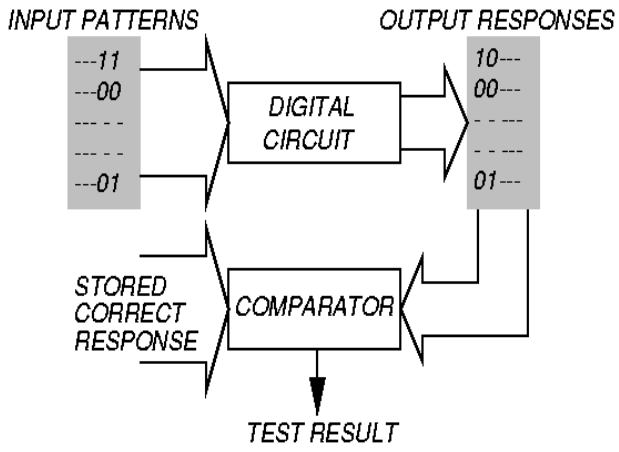

Fig -1: Testing Principle

Figure 1 explains the VLSI testing principle. The DUT has both inputs and outputs. The test vectors are applied to the DUT's inputs, and then the outputs are captured. The captured outputs are compared to the expected outputs; if they match, that DUT is functions correctly; if not, that DUT is faulty.

To make VLSI testing the following Design for testability (DFT) techniques are involved. DFT refers to those design techniques that make test generation and test application cost-effective.

DFT methods for digital circuits:

- Ad-hoc methods

  Structured methods:
- Scan - Partial Scan
- Built-in self-test (BIST)
- Boundary scan

  DFT method for mixed-signal circuits:
- Analog test bus

2. BOUNDARY SCAN TESTING

Joint Test Action Group (JTAG) for the purpose of developing a standard to resolve the issues of traditional testing techniques ad developed by IEEE Standard Boards, as IEEE 1149.1. Boundary-scan provides the suggests that to test product a lot of with efficiency, while maintaining or increasing the desired fault coverage to confirm smart quality.

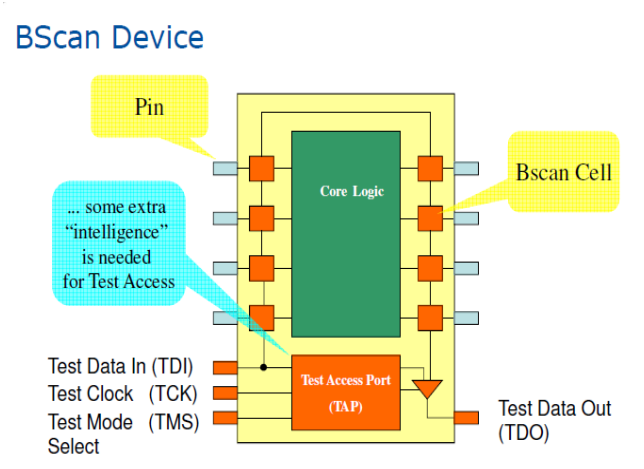

Fig -2: Boundary Scan Device

The boundary scan needs four pins, to regulate and observe the device under test (DUT) [7]. First, the test Clock (TCK) and test Mode choose (TMS) are 2 input pins needed to drive boundary-scan. Test Reset (TRST), is elective, since the state machine is place into a reset state once TMS is control high for 5 TCK cycles.

The other two pins, test data in (TDI) and test data Out (TDO) enable data to be shifted serially in to and out. All four or 5 pins form the Test Access Port (TAP), which an solely be used for boundary-scan performs and will not be shared with the other function

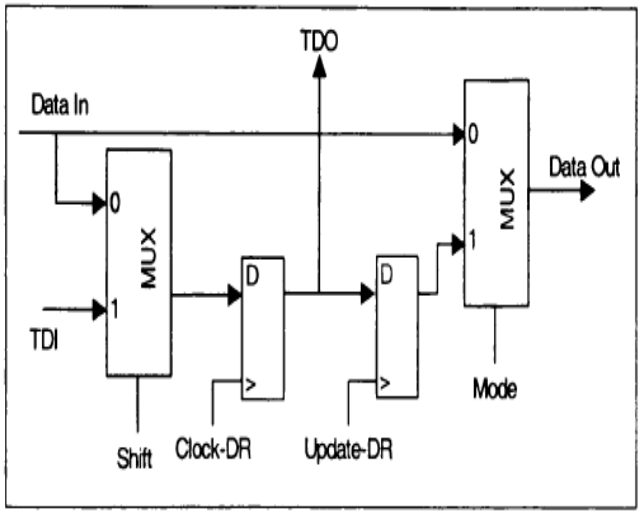

Fig -2: Boundary Scan Cell

In different instructions and TAP controller states, the control signals are also different, which cause four different functional operations of the BSC. Figure 2 shows the operations of boundary scan cell.

(1) Normal: when the control signal Mode is 0, at the output mux, data transfer from PI to PO.

(2) Scan: when the Shift DR is 1, at the input mux, data transfer from SI to shift register and Clock DR pulses.

(3) Capture: when the Shift DR is 0, at the input mux data transfer from PI to shift register and Clock DR pulses.

(4) Update: when Update DR pulses data transfer from shift register to parallel output register

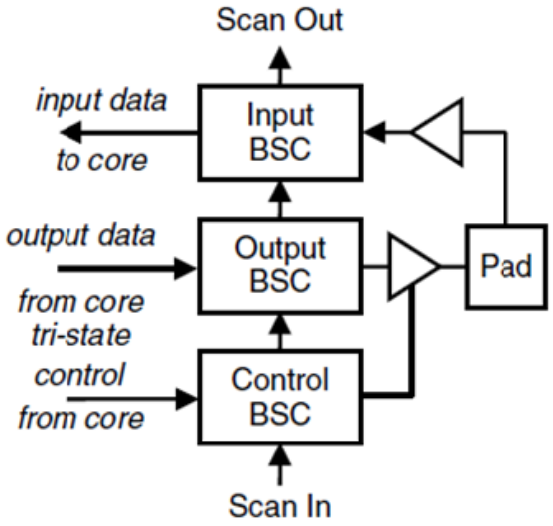

Fig -4: Bidirectional Buffer with multiple Boundary Scan cell

The number of boundary scan cells relies on the particular device However, for a duplex i/o buffer, as in associate degree FPGA, for example, associate degree i/o pin might have 3 boundary scan cells as shown in figure.4 , with one boundary scan cell for input data, one for output information, and one for tristate buffer management.

Some pins are duplex i/os, every of that has 3 boundary scan cells: input boundary scan cell, output boundary scan cell and management boundary scan cell. Some i/os are input solely, associate degreed solely have an input boundary scan cell. Besides the boundary scan cells connected to i/os, there are also some uncontrollable and unperceivable internal boundary scan cells

2.1. BOUNDARY SCAN Instructions

The JTAG normal denes directions that may be loaded into IR serially throughout an instruction-register scan cycle, then decoded and dead to regulate test operations. Instructions are often classified into mandatory instructions and optional instructions.

Table -1: Instruction for JTAG

Instruction	Status
BYPASS	Mandatory
CLAMP	Optional
EXTEST	Mandatory
HIGHZ	Optional
IDCODE	Optional
INTEST	Optional
RUNBIST	Optional
SAMPLE/PRELOAD	Mandatory
USERCODE	Optional

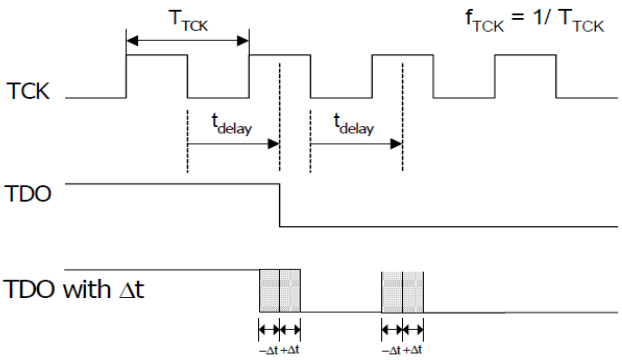

Fig -5: Timing Diagram for TAP Signals

The delay time (tdelay) to be entered is the time between the falling TCK edge at the controller's connector until the respective TDO signal edge from the UUT arrives at the controller's connector.

♦ tdelay includes the delay of **Distance POD** and/or testbus cable and UUT.
♦ Δt is the delay time tolerance. It is used to compensate inaccuracies of delay time and TCK frequency.

♦ If the exact value of tdelay is known, a value of 5 ns should be entered as Δt.

♦ The higher the desired test frequency is, the more accurately Δt has to be defined. The TCK frequency is set by the software according to the condition: **FTCK <= 1/ (4 x (Δt + 2 ns))**

Figure 5 shows that +Δt and −Δt form an undefined area where TDO is not exactly predicted.
However, it is important for the Boundary Scan technique that a rising edge of TCK may only occur after
this undefined area to ensure a safe value for TDO. The distance between two undefined areas has to
be at least as wide as an undefined area to achieve independence of the delay time.

3. CONCLUSIONS

In these paper the functions and operations of boundary scan has been studied with the JTAG instructions associated with the TAP controller and functions with device under test.

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