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A Study of Machine Learning Algorithms for VLSI Design

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Abstract:

Very Large Scale Integrated (VLSI) circuits have been a vast field in the semiconductor world and to make the machines behave as humans the popular technology used is Artificial Intelligence. Machine learning is the subset of AI, is the study of various algorithms and model which allows one to learn the machine from past data and train the machine to explicit the present. This paper, a brief review of various machine learning algorithms supports all the stages of VLSI IC Fabrication.

Keywords: VLSI, Machine Learning, SVM, KNN, and CNN.

Introduction:

The creation of millions of component interconnections on a chip using a standard set of manufacturing procedures on a flat surface is known as Very Large Scale Integration (VLSI). As the circuit size has greatly risen, the design and test development of VLSI chips have become expensive affairs to a great extent.

VLSI Design of a chip includes mainly the Front end and back-end Design. The front-end process includes the Logic design which in turn comprises digital specification, architectural design, and behavioral design. Back-end design includes process such as logic synthesis, physical design, and fabrication. Fig1 shows the VLSI Design flow.

Artificial intelligence (AI) has offered notable answers to numerous issues in a variety of sectors. A machine can readily imitate human intellect and carry out tasks of various complexity thanks to the AI principle, which is based on human intelligence. AI includes the field of machine learning (ML). There are countless uses for AI/ML algorithms given their many benefits. In the past ten years, VLSI design and technology have made substantial use of AI/ML techniques.

There is various Machine learning algorithm such as supervised learning, unsupervised learning, and reinforcement learning. Fig 2. Shows the classification of algorithms.

Supervised: Using test input-output pairs, supervised learning is the process by which a machine learns a function that translates an input to an output. It makes use of a collection of training data that has been labeled.

Unsupervised: Data-driven unsupervised learning analyses unlabeled datasets without the requirement for human intervention [1]. This is frequently employed for the extraction of generative features, the discovery of significant patterns and structures, the grouping of data, and exploratory reasons.

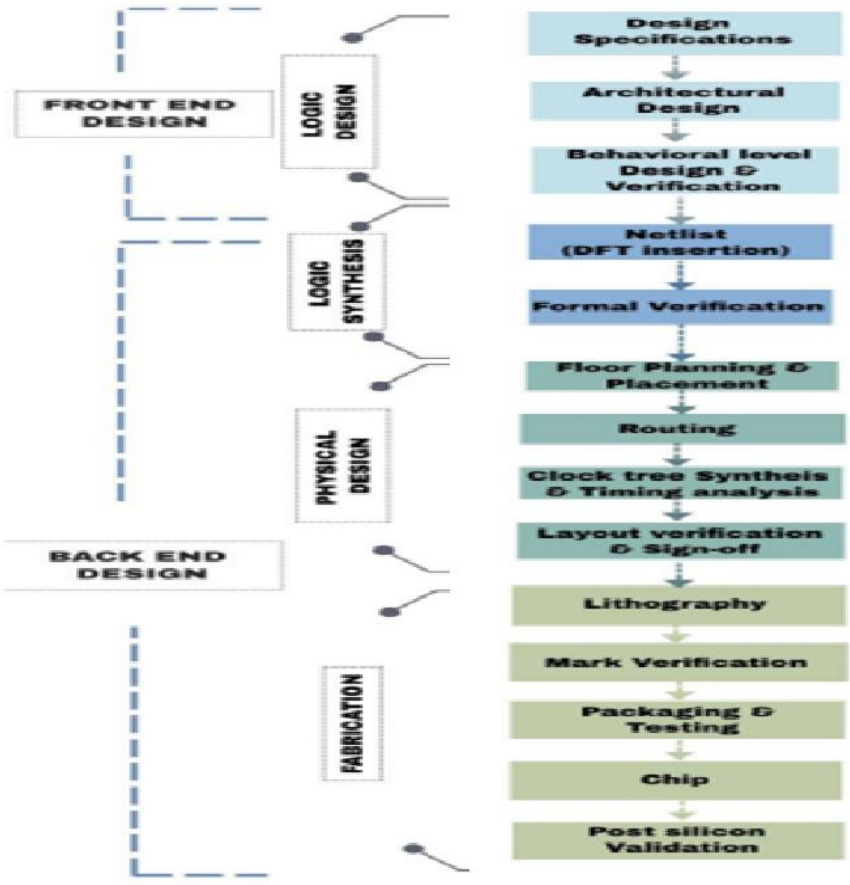

Fig 1: VLSI Design Flow

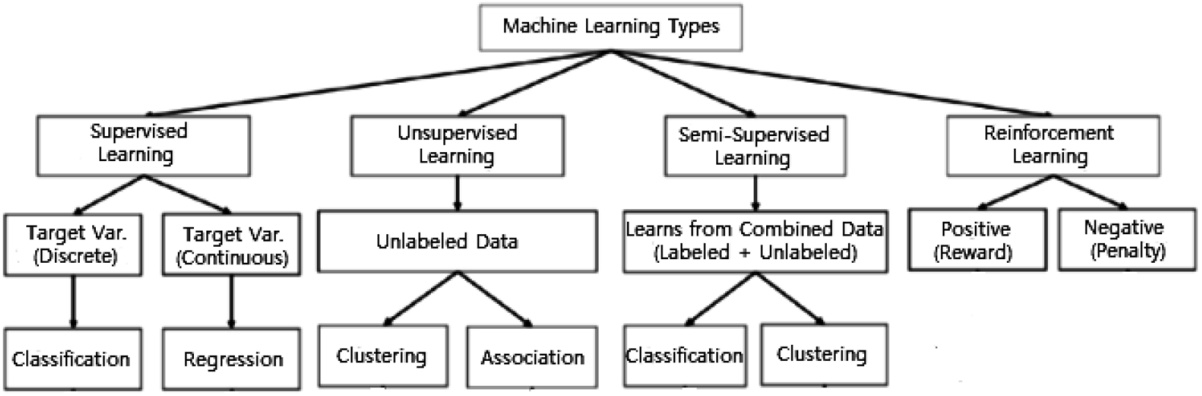

Fig 2: Classification of ML Algorithms

Semi-supervised: Because it uses labeled and unlabeled data, semi-supervised learning combines the supervised and unsupervised approaches outlined above [1, 3].

Reinforcement: Reinforcement learning is a form of machine learning technique that permits software agents and machines to automatically assess the best behavior in a specific context or environment to increase its effectiveness [2],

ML in Architectures

In order to give the authors an overview and a sense of the scope of research in VLSI designs for ML, this study presents a thorough review of VLSI architectural alterations at the memory and systolic array levels in this section, and at the SoC level in the following section.

Author [4] proposed a dependable, deep-in-memory ML classifier based on an on-chip trainer utilizing a typical 16 kB 6T-SRAM bit-cell array. With the use of memory devices arranged in an array, in-memory computing technology may carry out MAC operations. [5]

A parallel digital VLSI architecture for SVM training and classification was discussed by the author [6]. A multi-layer system bus and several distributed memories make full use of parallelism in this parallel architecture.

One of the popular and readily available programmable logic devices is the FPGA (Field Programmable Gate Array) [6, 7], which can speed up the processing capability of AI on hardware.

For the purpose of assessing the performance of SoCs, numerous ML, and deep learning applications have been described in the past. [8]

ML in Physical design

At various stages of physical design, machine learning, and pattern-matching approaches offer a reasonably good abstraction and quality of outcomes. To achieve early design closure, they serve as a link between each step and offer insightful input.

Partitioning, floor planning, placement & clock tree synthesis, and routing are the four general steps of physical design

[9] presents a deep-learning model (CNN-based) to estimate the routability of a location in order to quickly assess the level of routing difficulties that the detailed router would experience. A CNN-based RL model with optimal routability for the existing Placement is suggested in [10] for detailed Placement.

One of the critical phases of the VLSI physical design is clock tree synthesis. It is used to lessen insertion latency and clock skew. ML-based parameter tweaking in multi-source CTS is used by Ray et al. [11] to quickly construct a high-performance clock network.

ML in Fabrication

An IC is made using a variety of procedures, such as wafer preparation, epitaxy, oxidation, diffusion, ion implantation, lithography, etching, and metallization [246]. The entire process is carried out in very sophisticated fabrication units under continuous human supervision. To guard against external/environmental damage, the manufactured ICs are placed in appropriate packaging.

In order to identify pinching and bridging hotspots during the transfer of the mask to the wafer, Park et al. [12] present an SVM model trained on lithographic data. To achieve an accurate decision function to classify them into four categories—horizontal bridging (HB), vertical bridging (VB), horizontal pinching (HP), and vertical pinching (VP)—they further included corporate domain knowledge of lithographic information in the SVM kernel.

ML in Testing

After an IC has been manufactured, possible faults are found through a procedure known as VLSI testing. In the VLSI design flow, it is the most important step. VLSI testing takes up around 70% of the design development time and resources. Different testing techniques are used at different stages of the design cycle. Functional verification testing, acceptability testing, manufacturing testing, wafer level testing, packaging level testing, and so on are generally distinct layers of testing [13].

ML is being used to forecast the ideal test set in order to get the most fault coverage with the fewest test vectors. The fault coverage was increased in [14] by using the nearest neighbor technique to produce effective test pattern creation for BIST (built-in self-test). This program generates test patterns targeted at defects that are resistant to random patterns and finds them.

In VLSI circuits that are being designed for testing, scan chain architectures are frequently used. By improving the controllability and observability of the digital circuit logic, they broaden fault coverage and improve diagnosability.

A methodology for unsupervised learning using a Bayesian diagnosis model was proposed [15]. The model received the failing probabilities of each scan cell as input and divided the scan cells into various clusters.

Conclusion:

This paper illustrates the overview of applications of various machine learning algorithms implemented in each and every stage of VLSI Design. Supervised algorithms such as KNN and SVM are mostly implemented in all stages. Clustering is an Unsupervised algorithm which is also been used and neural network algorithms such as CNN, and RNN are also implemented in most stages of design.

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