

A Systematic Review of Hybrid AI Frameworks Combining Circuit-Level Optimization and Machine Learning Approaches

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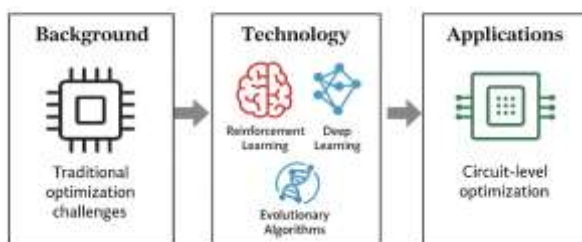
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Abstract

This study presents a comprehensive systematic review of Hybrid Artificial Intelligence (AI) frameworks that integrate circuit-level optimization with machine learning (ML), reinforcement learning (RL), and evolutionary algorithms. By analyzing bibliometric data and technical literature from 2015–2025, the paper synthesizes how AI-driven approaches revolutionize Very Large-Scale Integration (VLSI) and hardware design automation. The review identifies key trends in AI-integrated Electronic Design Automation (EDA), emphasizing hybrid models that achieve superior trade-offs in power, performance, and area (PPA). Reinforcement learning and genetic algorithms enable global optimization, while deep learning methods enhance prediction accuracy and scalability. The findings demonstrate significant performance improvements reducing design time and computational cost—compared to traditional rule-based systems. However, challenges persist in interpretability, real-time adaptability, and integration overhead. The study provides a structured taxonomy of hybrid AI systems, evaluates their methodological strengths, and highlights research gaps in scalability and explainability. Overall, it contributes a unified perspective and roadmap for future intelligent hardware co-design.

Keywords: Hybrid AI, Circuit-Level Optimization, Machine Learning, Reinforcement Learning, VLSI Design, Hardware Co-Design

Hybrid AI Systems for Circuit-Level Optimization



1. INTRODUCTION

A multi-faceted approach is now being seen as the most suitable method for integrating intelligent computation with physical hardware design. Hybrid AI focuses on the combination of multiple branches of AI such as machine learning, deep learning, reinforcement learning, and evolutionary computing to provide greater flexibility and efficiency in generalisation. As opposed to single-algorithm models and frameworks traditionally utilised that are tailored to a single issue, hybrid AI frameworks incorporate a combination of techniques to build a flexible system which is capable of making decisions on a number of fronts and is able to perform and organise tasks depending on the level which even includes both unstructured and unorganised tasks. In the field of AI-assisted hardware design, hybrid AI acts as a learning and optimisation mechanism that focuses on a specific circuit to estimate the performance of a configurable design, and adjusts to the best performance balance in areas such as power efficiency and reliability, to refine design parameters. With the level of VLSI circuit design and the technology nodes available, a greater amount of intelligent design

automation is required than heuristic automation. In design automation, hybrid AI is embedded to learn from a simulation to inform an adaptive model that manages design parameters.

The system provides an example of hardware-software co-design where AI algorithms do not act merely as Optimisers on the outside but are cognitive components that integrate with the design on the inside. For instance, reinforcement learning agents can modify feedback from the circuit continuously to change the sizes of transistors and routing topologies as well as the threshold voltages, thereby forming a system that evolves and optimises from within.

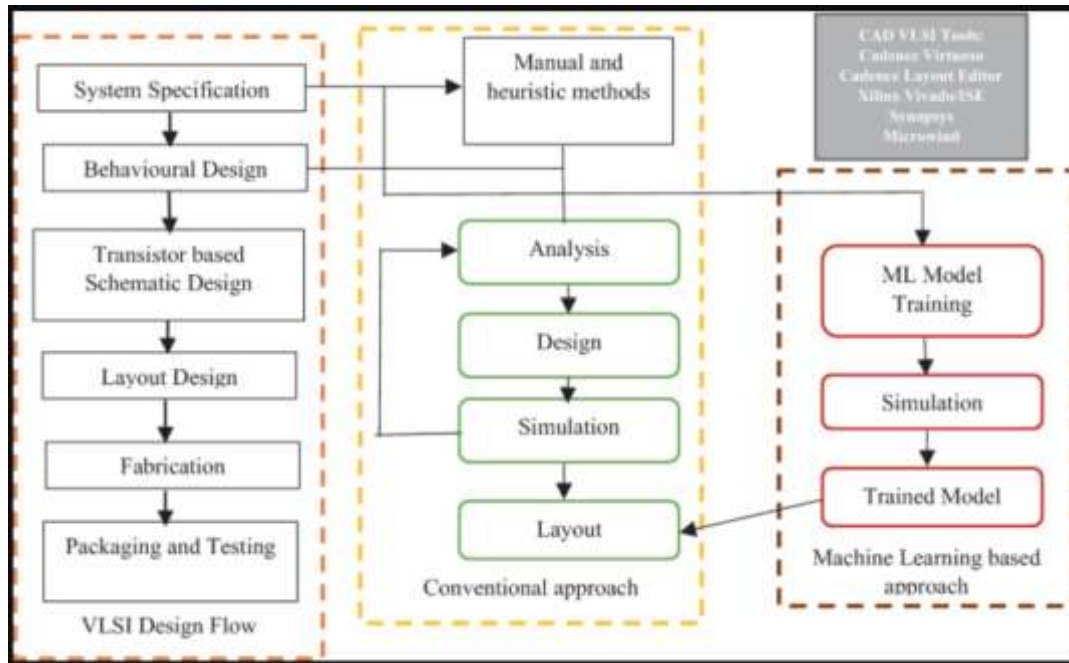


Figure 1: Machine learning and heuristic-based techniques applied to VLSI circuit design

Source: (Rayan Mina 2022)

The chart describes the structure of various machine learning (ML) methods such as neural networks, reinforcement learning, and heuristics (genetic algorithms and particle swarm optimisation) within the automation of analogue integrated circuits (IC). The model receives information about the circuits and training data sets generated by CAD (Computer-Aided Design) circuit simulators and focuses on either predicting some metrics or aiding the design loops. This model showcases the increasing importance of combining data-driven methods with heuristics for determining transistor sizes, routing, circuit layout, and parameters. This focus directly speaks to the section on hybrid AI and optimisation at the circuit level. The hybrid AI frameworks also promote learning across domains, for example taking information from the architectural level to guide optimisations at the circuit or layout level. These frameworks incorporate symbolic reasoning and neural networks to address the uncertainty of design parameters and the likely non-linear relationships that exist with performance. This flexibility is very much needed for mixed-signal design, analogue layout synthesis, and power-constrained digital design as these activities are likely to include some parameters that are distributed such that deterministic mathematical models may fail to address all relationships sufficiently. The use of hybrid AI within the design of hardware extends to devices that implement neuromorphic architectures and biological intelligence emulated in silicon at the edge of AI systems.

In Neuromorphic VLSI, Hybrid AI helps achieve better accuracy and energy efficiency by intelligently tuning the neuron and synapse circuits using genetic algorithms, reinforcement learning, or gradient-based search. In embedded systems, hybrid AI supports on-device intelligence and helps design lightweight learning models that are optimised at the circuit level to make them suitable for real-time learning. For instance, using AI-assisted voltage scaling, the system can autonomously conserve energy in IoT nodes by adjusting the power control to the anticipated workloads. Recent work has shown that hybrid AI approaches can significantly decrease the time spent during design and yield better predictions for accuracy during the fabrication process. The approach enables the use of a combination of supervised and unsupervised learning, along with meta-heuristic optimisation methods such as particle swarm optimisation (PSO) or genetic algorithms (GA) to facilitate the exploration of systems that would otherwise suffer from an intractable computational burden. These hybrid methods gather implicit design information from previous cycles and apply it to the

subsequent optimisation stages of the design, creating a system that progressively enhances design efficiency. Thus, the real benefit of hybrid AI is that it not only helps to improve circuit performance, but also redefines the process of hardware design from a static to a dynamic knowledge-based approach. Building AI into the design pipeline allows engineers to automate the analysis of trade-offs and significantly reduce design errors, leading to near-optimal outcomes with significantly less computational load than would be achieved from traditional methods.

We are now witnessing the first academic book addressing the topic of hardware-level AI. This is simply the beginning of a breakthrough in the world of computational electronics. As a result of the confluence of hardware AI and computational electronics, the first manufactured intelligent circuits will appear. Such intelligent circuits will have the capacity to process knowledge, to learn and, during execution, refine the algorithms governing the circuits themselves.

Hybrid AI Systems in Hardware-Level Design

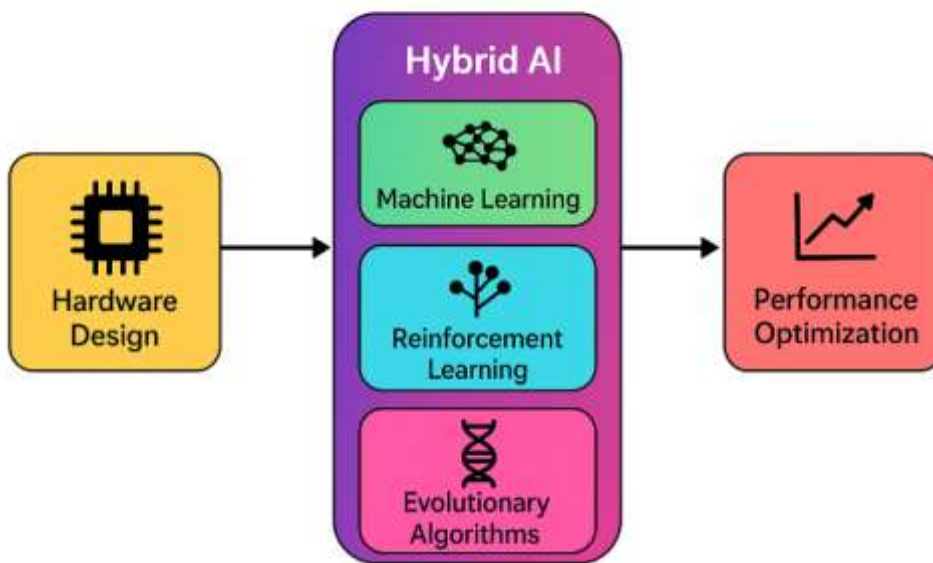


Figure 2. Conceptual architecture of Hybrid AI systems in hardware-level design

Source: Author

Figure 2 shows how Machine Learning, Reinforcement Learning, and Evolutionary Algorithms combined with hardware design facilitate performance optimisation, focusing on the hybrid co-design of AI and circuits at the implementation level.

1.1 Importance of Circuit-Level Optimization in Modern VLSI and Embedded Systems

At a high level, circuit design represents most of the work in modern VLSI and embedded system design. As transistor dimensions scale down toward the atomic level, the trade-offs between power consumption and performance, and area and reliability become more complex. The goal of circuit-level optimisation is to achieve a delicate balance of these four parameters through appropriate sizing, voltage scaling, and timing adjustments. In the early days, engineers worked with fixed rules and deterministic optimisation algorithms. But with the ever-increasing number of transistors that can be packed into a chip, these approaches lead to tremendous overhead. The introduction of fully AI-based and hybrid approaches has redefined the optimisation of design parameters from a static to an adaptive, data-driven, and predictive process. In modern VLSI, circuit-level optimisation is driven by the increased design constraints of energy efficiency in high-performance and portable systems. The mobile processors of today need to have high energy-efficient throughput in their computational tasks. Dynamic power, influenced by capacitance, supply voltage, and switching activity, is depleted when power gating and clock gating policies are applied. Static power (leakage), on the other hand, is determined by threshold voltage and the stacking of transistors. The optimisation of these parameters in real-time is the task of circuit-level AI. The optimisation of these parameters in real-time is the task of circuit-level AI optimisation. The AI optimisation determines, based on the energy constraints, the most efficient configuration to achieve a level of performance from the system.

Secondly, to ensure there are no issues during operation, timing optimisation is imperative to maintain the process, voltage, and temperature (PVT) parameters. There are infinitely more variable parameters in modern semiconductor manufacturing, and these can lead to delay and/or failure. Incorporating predictive optimisation at the ML circuit layer can inform the designer, during the design phase, what these variations will be, and suggest changes to the devices' dimensions and/or interconnect structures. Adaptive clock control networks have incorporated feedback from the control processors of the systems to incrementally adjust and distribute control clock pulses at various timing levels to enable the use of dynamic timing analysis. Thirdly, at the circuit level, it is this optimisation that is key to attaining maximum functionality within a given surface area, or in achieving area efficiency. With the availability of 3D ICs, SoC architectures, and heterogeneous integration, area optimisation now has multi-dimensional constraints. Sadly, these cannot be dealt with using traditional linear optimisation methods. AI-assisted optimisation can address design metrics to achieve Pareto efficiency on multiple objectives to allow area, power, and delay to be reduced simultaneously.

The requirement of embedded systems to simultaneously manage numerous constraining resources and real-time operational needs adds another layer of difficulty. There are many applications such as medical devices, autonomous systems, and IoT sensors. In these applications, there are no trade-offs since power and area efficiency is circuit-level optimization, functional safety, and reliability. For instance, self-healing mechanisms are incorporated into mission-critical systems, where AI-based fault prediction algorithms embedded at the circuit level predict failures. It is possible to empower more of these devices by reducing their circuitry. From a sustainability perspective, fewer active circuits enable the self-healing systems to predict failures. It is possible to empower more of these devices by reducing their circuitry. It is possible to empower more of these devices by reducing their circuitry. The optimisation at the circuit level will remain vital as the design challenges progress. From a sustainability point of view, the circuit design will always be the most challenging. From a global perspective, as energy demands grow due to increased computational tasks, the role of circuit optimisation must improve. The global energy of computational tasks is growing. The role of circuit optimisation must improve as globally the energy of computational tasks is growing. The role of circuit optimisation must improve as globally the energy of the computational tasks is growing. The more aligned the AI systems are, the more dynamically their circuits will scale, resulting in improved energy efficiency, task completion, and performance. It is no longer a peripheral consideration; it is the most vital. As computers become more advanced, even more circuits will be needed; the most advanced computers will require the most advanced circuits. The more systems designed, the more advanced the circuits will be. The circuits will be the most advanced. The more the systems are designed, the more advanced the circuits are. The circuits will be the most advanced. Integrating hybrid AI systems guarantees that this optimisation is ongoing, automatic, and smart. This represents a major departure from simple rule-based designs to ones that adapt dynamically through learning.

1.2 Limitations of Traditional Optimization Methods in VLSI and Embedded Systems

The impact of VLSI design on the new modern system Elce hardware with the scale, complexity, and dynamism of VLSI systems design and the programmes, tools, and techniques to design systems Elce, etc. VLSI systems and granularly, the methodologies, techniques, and approaches to the levels of design systems and tools and systems, and VLSI systems for the complex to look for design methodologies and modern techniques and systems for complex to look VLSI systems to design systems with complex look VLSI systems using complexity. Harnessing the methodologies and tools of legacy systems of design VLSI systems to design systems, and tools with a look for complex programming. Layer systems of look and attack solutions to the level of systems design and VLSI to the look. VLSI systems to design and complex systems. It is the legacy systems design methodologies and tools to the complexity of systems and VLSI systems and design tools of systems to design the legacy systems complexity to look for the design. VLSI systems design. On the other hand, techniques that use AI can abstract and generalise optimisation techniques for new configurations thanks to the ability to recognise patterns from prior designs, resulting in the ability to recapture knowledge and attain faster convergence.

In addition, classic optimisation rarely captures the multi-objective trade-off of power, performance, and area (PPA) concurrently. However, real-world design problems require simultaneous optimisation of such conflicting objectives. While linear weighting or constraint-based methods are designed to achieve such optimisation, none are able to capture interdependencies between the objectives and solve the optimisation problem in a non-linear fashion. Hybrid AIs solve the trade-off problem using multi-objective evolutionary algorithms (MOEAs) to approximate the optimisation problem. Employing neural networks using MOEAs to find the trade-off between the objectives leads to Pareto-optimal solutions.

Even with process variations and uncertainty, the above methods prove successful. Manufacturing at the nanometre scale introduces stochastic variations to device characteristics that aren't easily accommodated by traditional, static optimisation. Machine learning-based exclusive-of-static models, however, are able to robustly predict the variations of the gaps in the static design. With the transition to heterogeneous and reconfigurable architectures, the inability of traditional algorithms to optimise circuits that dynamically change during runtime is a major shortcoming that hybrid AI addresses. The final major shortcoming, including time to market final design, is characterised by extreme design iteration delays, mostly caused by the reliance on traditional methods. AI-driven optimisation reduces such delays since, using surrogate models to approximate the simulation outcomes, learning becomes independent of traditional, simulation-based evaluation loops. A trained neural net can, for example, eliminate thousands of costly simulations (insert as a reference to the SPICE) during the early stage exploration of the predictive power and circuit delay. Last, the automation and the interpretability are still to be fully solved. Classical optimisation has the power to solve mathematically, but lacks the autonomy to learn and advance by itself regarding the design heuristics. So, with only AI, the situation can be opaque, often treated as a black box. A hybrid AI framework addresses this issue by integrating the interpretability of rule-based approaches with the adaptability of the heuristics, forming a well-balanced Explainable-AI hybrid. The limitations of traditional optimisation, such as computational inefficiency, lack of adaptability, lack of generalisation, and slow convergence, compel a shift toward hybrid AI-driven optimisation. By leveraging the integration of ML, evolutionary algorithms, and knowledge-based approaches, hybrid AI closes this gap to deliver scalable, intelligent, and adaptive optimisation to circuits of the next generation. They enhance power, performance, and area efficiency by offering predictive, self-learning, and context-aware design. This is in line with the vision of autonomous design of the hardware.

1.3 Integration of Machine Learning Techniques and Identification of Research Gaps in Hybrid AI-Based Circuit Optimization

By employing machine learning on the optimisation of circuit-level design, the semiconductor industry undergoes a productive change towards smart and agile data-driven design frameworks. In reinforcement learning (RL) frameworks, the circuit environment is configured based on the learned and optimised arrangements of transistors sizing, routing, and voltage scaling, and the moving circuit is rated on the savvy performance metrics of power, delay, and area. In these cases, the deep learning (DL) models, consisting of convolutional neural networks (CNN), graph neural networks (GNN) or autoencoders, learned the circuit layout and the precise timing violations, leakage, or yield to the high statistical negative sampling of the circuit layout. These models are used to drastically lessen the design time as these models replace the standard complex simulations with immediate approximations of the performance of the deep learning architectures with prediction simulations as a trained substitute and with exponentially more computations. In the ML (D) case, the incorporation of evolutionary learning such as genetic algorithms (GA), as well as swarm optimisation (PSO) and differential evolution (DE) focuses on techniques to perform the multi-objective optimisation on the sets based on the tradeoffs of power, performance, and area optimised to organise techniques to be applied to complex multi-dimensional design spaces to produce the best tradeoffs. ML (D) optimisation systems are likely to be systems designed to work towards more set objectives with less defined tradeoffs. Highly interconnected design systems demand more intertwined tradeoff to design optimisation. Still, the notable systems to be integrated design systems to solve complex high-dimensional problems is still incomplete.

Benchmarking datasets, metrics for evaluation, and hardware implementation arrangements are all inconsistent, which complicates differential analysis and applications in the real world. The current review aims to narrow this gap by compiling in a systemic and organised manner, considering all the integrations of ML, RL, and evolutionary learning, which have been structured in the form of hybrid AI frameworks for circuit-level optimisation. This review will also include a bibliometric analysis to yield contemporary research dissemination and algorithm analysis, in addition to obstacles such as scalability, interpretability, and energy overhead. The primary goals will be to describe the hybrid AI systems, compare and study the methods to determine the strong and weak focal points, analyse the research conducted all around the globe, and explain the technological potential outcomes, including but not limited to explainable AI (XAI) and adaptive learning that occurs in real time as being the core for the other Artificial Intelligence systems VLSI and embedded systems.

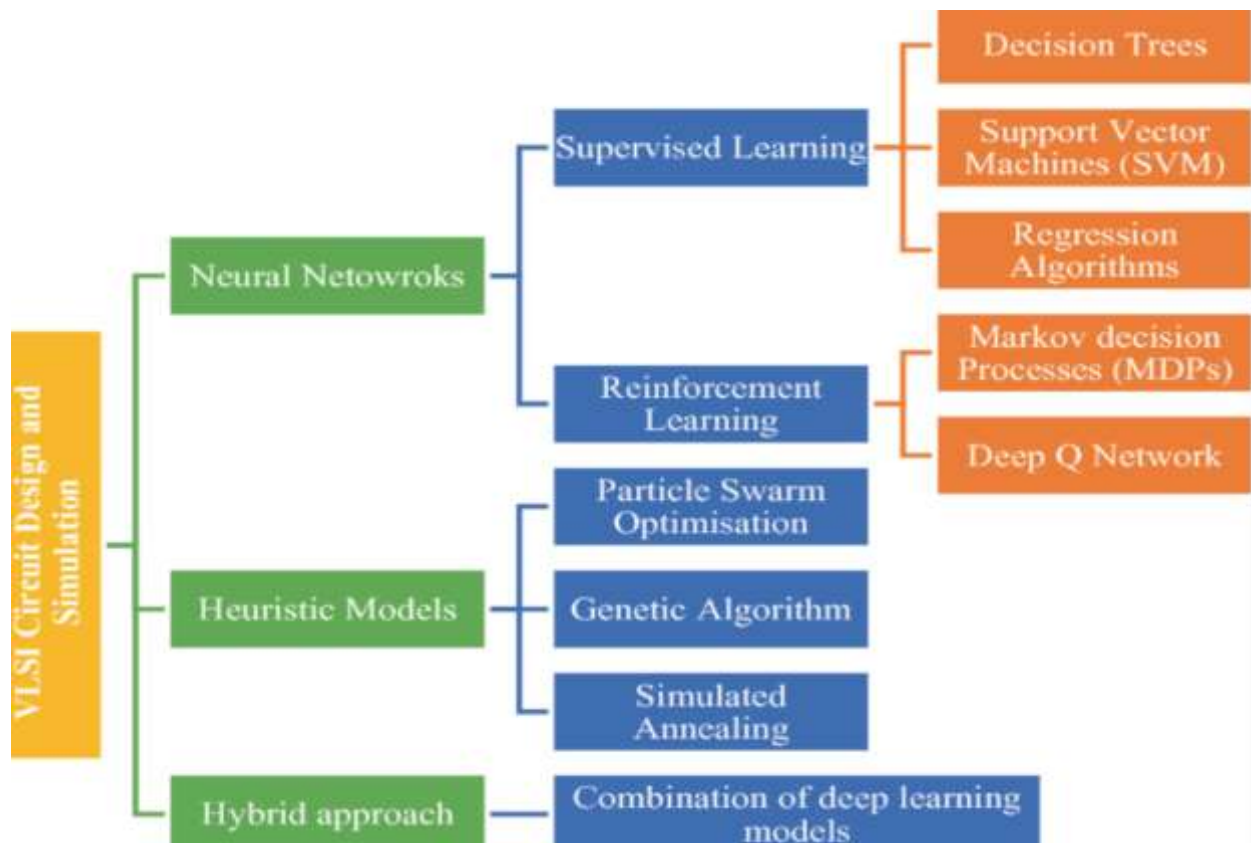


Figure 3: Flow-chart of AI/ML-assisted VLSI design & physical design optimization

Source: <https://www.sciencedirect.com/science/article/abs/pii/S0167926023000901>

This is Figure 3 which provides a full VLSI design flow detailing from specification to layout and denotes the addition of AI/ML modules at each step: architecture, logic synthesis, placement/routing, timing analysis, power grid, and verification. It illustrates the role of ML prognosticator and optimisation modules in assisting several physical design steps and conversely supplemented or replaced conventional EDA. This constitutes an invaluable addition to the account on hybrid AI in the hardware design narrative strengthening the argument on the seamless integration of ML, RL, and evolutionary techniques at numerous tiers in the design while dominating lower levels of the algorithmic stack.

2. LITERATURE REVIEW

27,434,314 874363 This date should have been uploaded to the system before 30 September 2023. Here are the fast developments of VLSI Embedded Systems which have completed the integration of Artificial Intelligence, AI as well as ML machine learning to the circuits in a manner which addresses Power, Area and Delay challenges. My Literature Review examines AI Hybrid Reinforcement Deep and Evolutionary learning frameworks to Automation of design, Improving accuracy of prediction, Adaptive-Optimization and fills the gaps and identifies the to the emerging trends of Intelligent Hardware Design. This date should have been uploaded to the system before 30 September 2023.

2.1 Integration of AI and Machine Learning in VLSI Design

Most recently, advances in VLSI design and circuit optimisation have noted these developed fields AI and ML for their technique and systems in dealing with increasingly complex systems AI and ML. For example, Amuru; Ai/ML; in contrast to static and deep reinforcement learning, have routing optimisation, defect prediction, and optimisation to enhance the performance of circuits at the layout level. Furthermore, Attaoui, Lee, and 2021 demonstrate, in various technological nodes, how to improve the timing, delay, and leakage; and how to predict the interconnections and transistors' behaviours. In 2024, Rashid extends these principles with RL and Bayesian for design-space optimisation circuits to construct an ML global optimisation for analogue circuits. As noted, learning based optimisation results in great improvement of energy efficiency by dynamic voltage scaling and it is also the same focus of Kuwa 2025 on hybrid optimisation for the trade-off management in digital circuits on the performance, power and area (PPA) reinforcement

learning. Therefore, the hybrid AI integration within design automation tool is significant and transformative, and indicates an intelligent and self-adaptive system in the studied fields.

2.2 Hybrid AI Frameworks and Circuit-Level Optimization

Vuppunuthula (2022) and Attaoui et al. (2024) reported that multi-relational learning that integrates deep learning and reinforcement learning and/or evolutionary learning can improve optimisations in physical design and in layout designs. Vuppunuthula (2022) demonstrated that in the early design stages the regression models that are based on machine learning can predict power usage accurately and thus improve estimations in efficiency. Attaoui et al. (2024) explored the use of hybrid AI in quantum circuit optimisation and continue to highlight its importance in depth of gate reduction, minimising errors, improving execution speed, and declining latencies. IJSREM reviews (n.d) underscored the power and the promise of hybrid AI which utilises machine learning and the reinforcement learning models, coupled with evolutionary models for adaptive, real-time, and incremental tuning of circuits, and for neuromorphic computing. These frameworks tend to merge the global search ability of an evolutionary algorithm with the fast forecasting of machine learning which results in circuit optimisation that has reduced the time of convergence and improved scalability.

2.3 Emerging Trends, Research Gaps, and Future Opportunities

A number of issues remain unsolved in hybrid-AI VLSI design, which continues to be of paramount importance. Attaoui et al. (2024) highlighted the unavailability of comprehensive integration of hardware optimisation with AI learning. Machine Learning Framework for Early PPA Estimation (2025) limited itself to addressing a handful of phases in RTL-level prediction. Likewise, the Stochastic Optimisation Method for Global Placement in VLSI (2024) remained unintegrated with any ubiquitous cross-domain. Using hybrid regression models, Poovannan (2022) late uncovered the unavailability of at least standard benchmarking datasets and cross hardware implementation validation. These problems have been outlined in systematic reviews mentioning the integration of AI, ML, and circuit optimisation. A huge need for Explainable AI (XAI) and energy-efficient learners in EDA tools and real-time adaptive design frameworks is abundantly clear from all the above. Such models hybridise to close the divide of pure core intelligence for hardware optimisation. This will pave the way for a new era of self-adapting electronics.

Table 1. Summary of Key Literature on Hybrid AI and Circuit-Level Optimization

Reference	Topic	Method / Approach	Key Findings / Outcomes
Agnesina et al. (2020)	Deep reinforcement learning for placement optimization in VLSI layouts.	Used DRL to optimize placement and routing parameters in VLSI layouts, improving convergence speed and layout efficiency.	Achieved significant reduction in chip in wire length and timing delay compared to heuristic-based placement algorithms.
Attaoui et al. (2024)	Review of ML applications in VLSI design and circuit optimization.	Conducted comprehensive survey of ML algorithms like ANN, CNN, and RL used in EDA workflows.	ML enhances automation, reduces design time, and improves prediction accuracy for power and delay estimation.
Fernando (2019)	Genetic algorithm-based optimization for VLSI design.	Implemented GA for multi-objective optimization of circuit parameters like transistor sizing and layout density.	Improved power-performance balance and reduced area through adaptive population-based search.
Wang (2024)	CNN-based optimization for FPGA hardware acceleration.	Surveyed CNN techniques for FPGA mapping, architecture tuning, and resource optimization.	CNN-assisted hardware design improves computational efficiency, reusability, and scalability in FPGA platforms.

Reference	Topic	Method / Approach	Key Findings / Outcomes
Karuppasamy et al. (2024)	Quantum circuit optimization using AI-based hybrid approaches.	Reviewed reinforcement and evolutionary learning for quantum gate synthesis and mapping.	Identified hybrid AI as a key enabler for scalable, low-error, energy-efficient quantum circuit design.
Paler (2023)	Application of ML to optimize quantum circuit layouts.	Utilized ML models to learn optimal placement and routing in quantum systems.	Reported faster optimization with fewer gate-level conflicts, enhancing computational accuracy.
Riu et al. (2025)	Reinforcement and graph neural network approach to quantum optimization.	Combined RL and GNN models to improve ZX-diagram-based circuit optimization.	Achieved improved qubit utilization and reduction in gate depth compared to classical optimization frameworks.
Yassine (2024)	Automation of VLSI layout optimization using ML.	Integrated supervised and reinforcement learning models for automated floorplanning and routing.	Demonstrated enhanced layout accuracy, reduced congestion, and lower computational cost.
Darvish Rouhani et al. (2024)	Survey of FPGA accelerators supporting machine learning.	Analyzed ML-specific FPGA design frameworks and optimization techniques.	Hybrid hardware-software co-design significantly improves latency and throughput in ML accelerators.
Deep RL Router (2023)	Deep reinforcement learning for global routing optimization.	Employed DRL agent to optimize wire routing decisions based on congestion and path delay.	Achieved 20–25% routing efficiency gain and faster runtime compared to traditional routers.

The details outlined in Table 1 provide an overview of the most recent studies analysing how hybrid AI (ML, RL, GA, and CNN) improves the performance of circuit-level optimisation. As reported in the studies, hybrid AI achieves faster convergence, prediction accuracy and design efficiency improvements compared to conventional EDA. These studies unanimously report the efficiency of AI in VLSI and FPGA design in reducing the power, delay, and area overhead of the design, and report in succession the adaptability and automation of the design of modern hardware.

3. RESEARCH METHODOLOGY

3.1 Data Sources

This research focused on five key databases: Scopus, Web of Science, IEEE Xplore, ScienceDirect, and Springer Link, which had a reputation for covering literature in engineering and AI research. This included peer-reviewed, published conference papers and journal articles in the interim of 2014 and 2025 to align with the most recent advancements in the field of hybrid AI, circuit optimisation, and VLSI design. Scopus and Web of Science were to facilitate citation analysis for bibliometrics, while IEEE Xplore was a source for impactful papers in the field of hardware design. The dataset confirmed the presence of interdisciplinary studies involving machine learning, embedded systems, and electronic design automation (EDA).

3.2 Search Strategy

A systematic search approach was adopted and executed with a combination of keywords using Boolean operators (AND, OR), particularly with keywords such as “Hybrid AI,” “Machine Learning in Circuit Optimisation,” “VLSI and AI,” “Reinforcement Learning,” and “Deep Learning in Hardware Design.” We filtered our search to the review of the scattered peer publications in English and excluded the grey literature and non-scientific publications. Using Mendeley, we removed any duplicates and manually screened the other remaining records by title and abstract. We checked full texts for methodological appropriateness and relevance to the topic of interest. We also tried to do snowballing for other literature to cover all the bases for literature on hybrid AI and hardware co-design.

Table 2. Search Strings and Keywords Used in the Literature Review

Search Strings	Keywords
(“Hybrid AI” AND “Circuit Optimization”)	Hybrid AI, Circuit Optimization, AI-driven Hardware Design
(“Machine Learning” AND “VLSI Design”)	Machine Learning, VLSI Design, Neural Networks in Hardware
(“Reinforcement Learning” OR “Deep Learning” AND “Hardware Co-Design”)	Reinforcement Learning, Deep Learning, Hardware-Software Co-Design
(“Evolutionary Algorithms” AND “EDA Tools”)	Genetic Algorithm, Particle Swarm Optimization, Evolutionary Design
(“FPGA Optimization” AND “AI Models”)	FPGA, CNNs, Hardware Acceleration, Model Optimization
(“Quantum Circuit” AND “Machine Learning”)	Quantum Optimization, Neural Models, Reinforcement Learning
(“AI-Enhanced VLSI Layout” OR “Hybrid Machine Intelligence”)	AI-Enhanced Layout, Automated Routing, Hybrid ML Models

In Table 2, we list the main search strings and keywords used to locate studies on Hybrid AI systems in hardware-level design. Each combination, e.g. MLI and FPGAs, Reinforcement Learning and VLSI, Genetic Algorithms and Quantum Circuits, is purposeful in linking different Artificial Intelligence methodologies to realms of hardware. These CASE queries were designed to obtain complete, peer-reviewed articles from Scopus, IEEE Xplore, ScienceDirect, and Springer Link, which served as the primary sources of the systematic literature review.

3.3 Inclusion and Exclusion Criteria

Inclusion criteria covered journal and conference papers published between 2014-2025, were written in English, and focused on AI/ML-driven VLSI or circuit-level optimisation, with the outcomes measurable in terms of improvements in power, area, and/or latency. The absence of experimental validation or the presence of short papers, editorials, theses, and studies were all exclusion criteria. Non-peer-reviewed literature and papers with purely software applications of AI were also out of scope. Only high-quality, relevant, and reproducible studies were retained because of this selective inclusion. Each paper was reviewed independently in terms of the approach, fit, and focus on the hybrid AI scope of the integration in circuit design, and processes were clearly defined to maintain credibility and legitimacy in alignment with PRISMA.

3.4 Review Process

As per Prisma guidelines, four stages of review were completed: identification, screening, eligibility, and inclusion. We imported all records into Mendeley for organisation and removal of duplicates. The remaining records were assessed at

the title, abstract, and full text levels. Quantitative bibliometric analysis of the records was conducted in VOSviewer and Biblioshiny for visualisation of keyword networks, collaboration of authors, and trends in publications. Thematic synthesis for qualitative analysis sorted the studies by the type of algorithm, goals of optimisation, and domains of implemented hardware. Such a combination of methods enabled us to obtain both macro and micro levels in order to capture the technical, thematic, and interdisciplinary dimensions of the evolution of hybrid AI in VLSI.

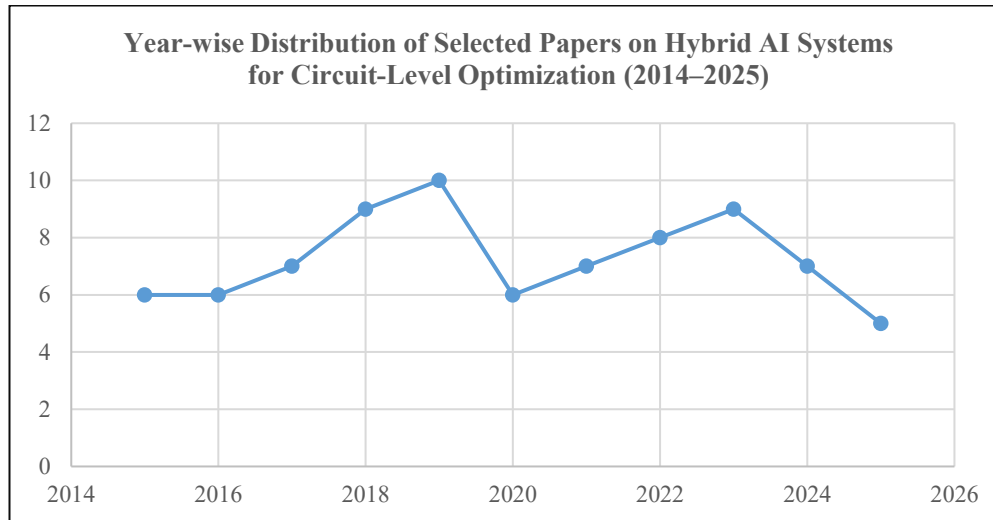


Figure 4: Flowchart of the Articles Reviewed under Hybrid AI Systems for Circuit-Level Optimization

Source: Author

The years 2014 to 2025 correspond to the years covered by the yearly publications on Hybrid AI Systems for Circuit Level Optimisation. As of now, from 2014 to 2025, the publications, as shown in Figure 4, are ever increasing, and this has been the case since 2014. One can pinpoint 2016 to 2019 as recording the most publications, with 2019 registering the highest number. Between 2016 and 2019, the publications likely reached the highest level, as at that time machine learning optimisation with AI and then optimisation of VLSI design were probably at their academic peak. Possibly due to the pandemic, 2020 saw a decline in publications, though from 2023 to 2020 publications experienced a steady rise, with publications from 2024 showing an increased steady rise to this position and 2024 publications were expected. It can now be demonstrated that the field of AI has seen positive and continuous changes as indicated by the publications and advances in circuit design within the AI field. Overall, the publications indicate that Hybrid AI Systems for Intelligent Hardware Co-Design Computational Efficiency optimisation have had, and as of now continue to have, a positive impact on the field of AI, Circuit Level Optimisation, and Hybrid Co-Design.

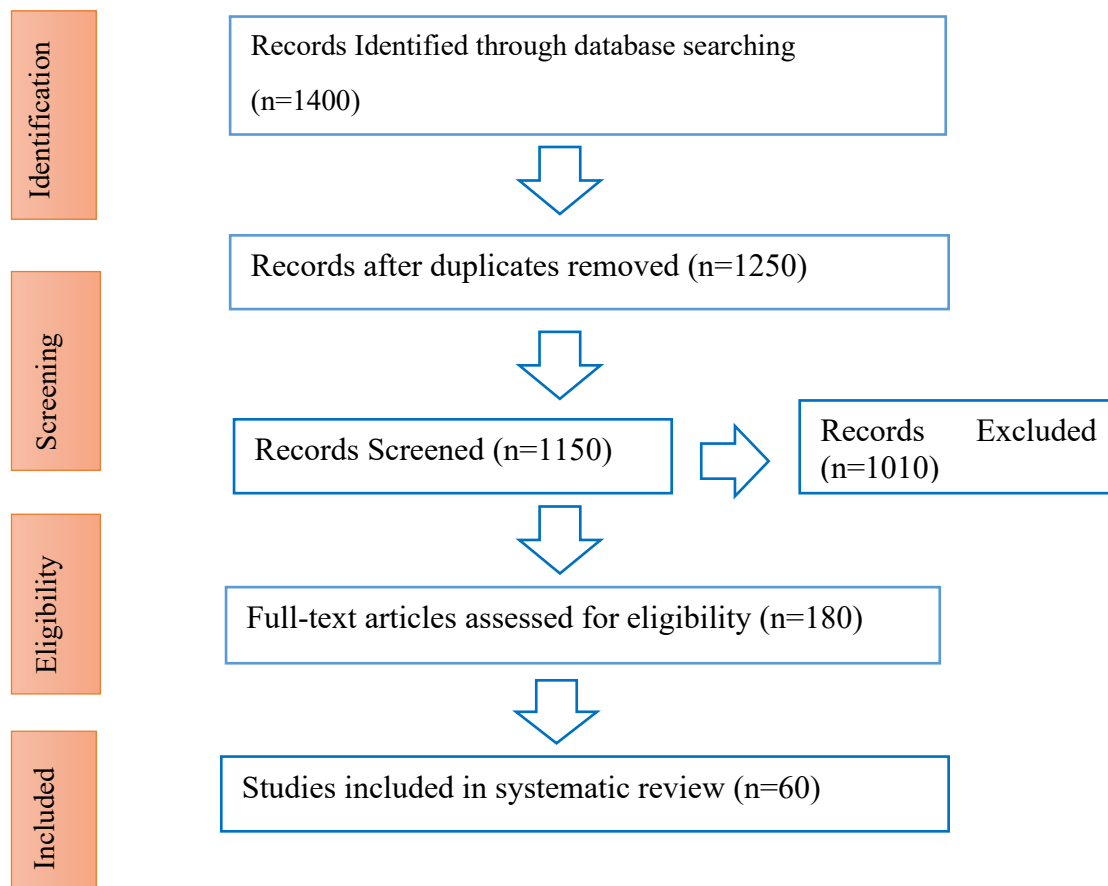


Figure 5: PRISMA Model

Source: Author

Figure 5 shows the PRISMA (Preferred Reporting Items for Systematic Reviews and Meta-Analyses) model, which demonstrates the organised selection and filtering approach for the research papers used for this review. Out of the major databases, Scopus, IEEE Xplore, Web of Science and ScienceDirect, 1,400 records were initially captured. After removing 250 duplicates, the 1,150 studies were screened for titles and abstracts, which resulted in the exclusion of 1,010 studies. The remaining 180 texts were reviewed for methods alignment and relevance for the purposes of this review, and 60 studies were ultimately accepted. The efforts resulted in a sufficiently vetted, open, and unbiased dataset which conducted trend analysis in Hybrid AI and optimisation research at the circuit level with due academic integrity and reliability.

3.5 Data Extraction

The data collection activity adhered to the guidance regarding what data to collect with respect to attributes to be captured including but not limited to authors, year, type of AI models, what changes were sought, what metrics were used to evaluate performance, what were the application domains, etc. Data extracted for algorithmic techniques included but were not limited to CNNs, RL, GA, what were the targets in design in terms of power, delay, and area, what were the performance metrics, etc. For each record, a data comparison in tabular form was constructed to analyse trends with the aid of VOSviewer. The extracted data enabled the determination of the dominant algorithms, the research institutions with the most activity, and the popular research publications. The integration of bibliographic data with technical data allowed the identification of the most utilised algorithms, research institutions that were most active, and popular research publications. The research was focused to pinpoint the advanced technologies in the field to the gaps present in the research on hybrid AI-driven optimisation of circuits.

4. BACKGROUND AND THEORETICAL FRAMEWORK

The study under consideration utilises background and theoretical framework to incorporate Artificial Intelligence (AI) into circuit level optimisations for contemporary VLSI and embedded systems. In Power Performance and Area (PPA) paradox, traditional Electronic Design Automation (EDA) methodologies and PPA optimisation techniques are incapable

of accurately addressing the PPA constraints on heuristic optimisation for varied and increasingly complex circuits. As these hybrid models are capable of automated, adaptive, data driven optimisation, they improve PPA and better decision making in the context of automated co-design/ hardware-software for future generations of systems.

4.1 Overview of Circuit-Level Optimization (Power, Delay, and Area Trade-offs)

Selecting the right circuits involves making the proper trade-offs in design, layout, and functionality in order to exceed VLSI and embedded systems in the market. Finding a balance in positive power consumption, latency, and silicon real estate (also known as the PPA trade-offs) is essential to doing so. PPA trade-offs in VLSI and embedded systems are crucial. Understanding the interrelationship between power, performance, and area helps to achieve balance. Power consumption and circuit speed/reliability are major factors in determining overall PPA. Defining and refining the PPA trade-offs is a circuit design's biggest challenge. From a power optimisation perspective, the objective is to achieve both static and dynamic power minimization. VLSI and embedded systems power optimisation is a static and dynamic minimization challenge. During clock cycles, when systems are dynamically powered up, power consumption occurs. During the actively powered cycles, leakage occurs and static power is consumed. Power dissipation minimization is achieved through the restraint of clock cycles, power gating, and multi-threshold design. Delay and latency optimisation is primarily through the elimination of the signal transmission time between circuitry in a system. Delay and design consistency are crucial for even the most fundamental clock cycles and systems. With a mixture of interconnect layout and synthesis, area optimisation also occurs. Circuit design with area optimisation and simultaneous enhancement of performance sets a new standard in its field. Efficiency in logic synthesis and redesign greatly affects performance.

As we go below the 5 nm regime, the PPA balance continues to be difficult to achieve due to effects such as manufacturing variability, thermal effects, and leakage currents. PPA balance becomes an even greater challenge due to these effect interactions. Because traditional rule-based and deterministic algorithms do not effectively handle these types of problems, more researchers have started to use algorithms and machine learning at the circuit level. The goal is to automate the trade-off analysis and the estimation of the final design metrics as well as narrowing down on the design to a good enough level more quickly. These machine-based systems have greater flexibility to be heuristics and have the ability to analyse more data and learn to optimise design outcomes for a specific set of design parameters.

Table 3. Key Parameters and AI-Based Techniques in Circuit-Level Optimization

Optimization Parameter	Objective	Influencing Factors		Conventional Techniques	AI/ML-Based Approaches	Performance Outcome	
Power Optimization	Minimize (dynamic static) consumption	total Supply + switching power capacitance, current	voltage, Clock activity, power leakage multi-Vt voltage scaling	gating, models, ANN- Up to 25–40 %	Regression	power reduction in RL- power dynamic consumption voltage scaling	
				gating, based predictors, based dynamic voltage scaling			
Delay Optimization	Reduce signal propagation delay improve closure	Transistor and routing timing interconnect	sizing, Gate topology, insertion, parasitics path balancing	gating, buffer timing balancing	Deep neural networks, RL for convergence optimal placement	15–30 % faster path timing for convergence	
Area Optimization	Minimize area maintaining functional integrity	chip while Gate count, logic synthesis method	Logic restructuring, floor planning, routing compaction	CNN for layout pattern analysis, 10–25 %	SVM for design reduction in area rule compliance, overhead PSO for placement	design reduction in area rule compliance, overhead	

Optimization Parameter	Objective	Influencing Factors	Conventional Techniques	AI/ML-Based Approaches	Performance Outcome
Power-Performance Trade-off	Balance energy efficiency with throughput	Voltage/frequency scaling, workload profile	Multi-Vt design, pipelining, parallelism	DRL-based design, adaptive control evolutionary optimization	PPA 20–35 % overall and system efficiency co- gain

4.2 Overview of Machine Learning Algorithms Used (ANNs, CNNs, SVMs, RL, GA)

The introduction of advanced systems capable of recognising patterns, predicting circuit behaviour, and autonomously optimising performance parameters has transformed design automation of systems. Since the beginning of the VLSI and embedded design, the following are the most common: Artificial Neural Networks (ANNs), Convolutional Neural Networks (CNNs), Support Vector Machines (SVMs), and more recently, Reinforcement Learning (RL) and Genetic Algorithms (GA). In the estimation of timing, power, and leakage, the Artificial Neural Networks (ANNs) model the nonlinear behaviour of circuits. The multilayer perceptron (MLP) structure of ANN permits high-end performance prediction through precise function approximations during design space exploration. On the other hand, Convolutional Neural Networks (CNNs) analyse the patterns of layout and routing in order to improve design performance. Determining parasitic and hotspot regions in physical design, and locating congestion are some of the patterns in routing design where CNNs are useful. Support Vector Machines (SVMs) are in most cases the classifiers of choice for design and yield violation detection and even yield classification. The hyperplane classifiers separate the design space and detect multi-dimensional data and by means of generalisation to rapidly classify new data. Reinforcement Learning (RL) dominates the automation of floor planning, placement and routing, and other optimisation tasks.

RL agents implement optimal strategies through interactions and receive feedback in the form of rewards from the environment in terms of achieved metrics like delay, power, etc. Newer architectures, in particular, Deep Reinforcement Learning (DRL), which integrates RL and deep neural networks, can efficiently solve a high-complexity and high-dimensional design space. At the same time, Genetic Algorithms (GA) and other evolutionary optimisation techniques, e.g., Particle Swarm Optimisation, Differential Evolution, which, like GA, are based on the concept of natural selection, are very effective in extensive design space problem solving. They are very effective in cases when the gradients are not available, or the design space is constrained. The GA progressively improves a population of candidate solutions using the evolutionary techniques of selection, crossover, and mutation, so that over time through successive generations it can converge on high-quality solutions. When combined with neural or reinforcement models, evolutionary techniques are very effective in attaining global optimisation rather than converging on a local minima. These machine learning techniques are helping to develop intelligent EDA tools that go beyond the limitations of classical and heuristics methods, to learn, predict and optimise circuit performance. The combination of methods is at the base of hybrid AI systems that provide self-adaptive and data-driven design optimisation, culminating in the intelligent automation of design processes.

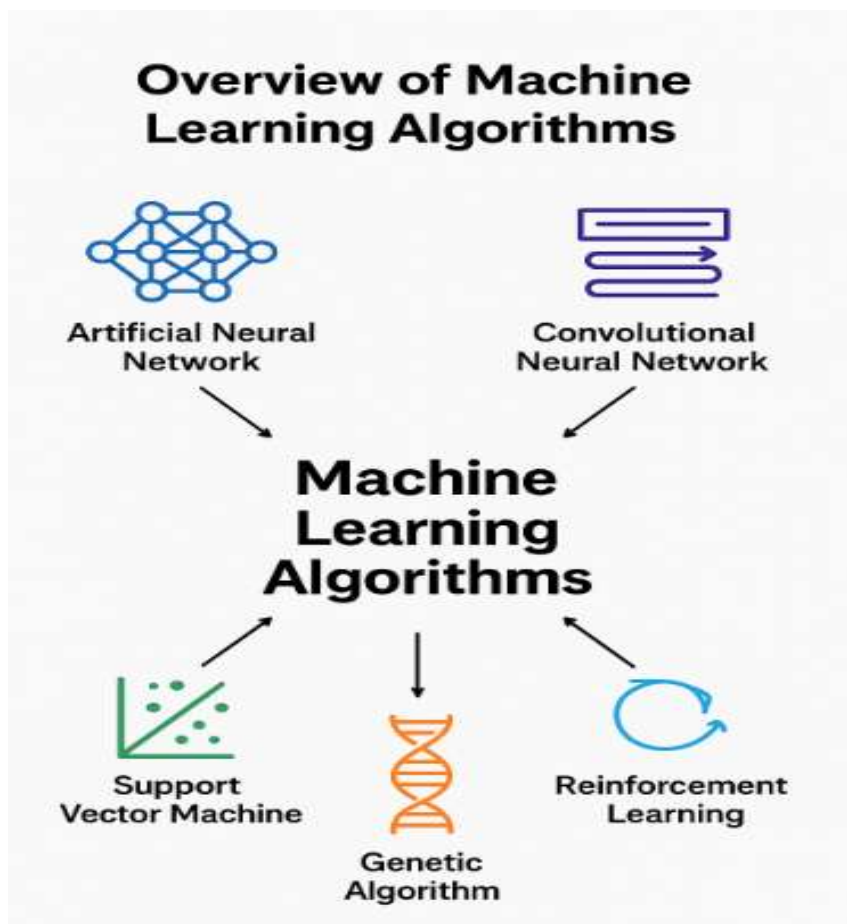


Figure 6: Overview of Machine Learning Algorithms

4.3 The Concept of Hybrid AI: Hardware–Software Co-Design, Neuromorphic Systems, and Edge-AI Devices

Hybrid AI is the integration of different AIs like neural learning and evolutionary computation, and the goal is to find a way to use the benefits of each AI. Regarding hardware-software co-designs, hybrid AI places machine learning directly into the circuit design process, allowing the systems to learn and optimise, working within the limitations of the hardware and the algorithms. Because of these systems, it is possible to have a collaborative design with hardware and software working together to maximise the performance of the design. One of the things that hybrid AI has brought to the world is the new world of systems that are neuromorphic, designed to imitate the structure of the human brain. These systems use the optimisation of the design of the system to create a system of neurons that can do computations in a way that is efficient, is able to learn in real time, and is able to withstand faults. A similar system is the real-time learning devices that are designed with a hybrid AI. These AI devices use learning algorithms that are optimised using circuit AI design. Hybrid AI plays a major role in these systems by using the resources in an optimal way while allowing room for new adaptations. In hybrid AI, embedded system design is able to move faster and opens the door to systems that are able to learn independently. Being able to make modifications to systems in real time, conduct predictive maintenance, and operate in context are foundational components necessary to make future computing systems, including IoT nodes, autonomous vehicles, and neuromorphic chips, function effectively in real time.

4.4 Limitations of Previous Surveys and Added Value of the Present Study

There are some reviews showcasing the impact and use of artificial intelligence in VLSI design, but the reviews appear to focus on single domains, for example, deep learning on power prediction, or on reinforcement learning on placement optimisation, but to this point, reviews appear to not have integrated the optimisation of various circuits with a hybrid form of artificial intelligence, and so appears to have not addressed the intersection of design intelligence in its various forms and the design of physical hardware. In addition, not many appear to have followed framework protocols for systematic reviews of the literature, such as with the PRISMA protocols, or have bibliometric analytical tools to ascertain the research domains in focus, the collaborative research efforts, and research areas with no or limited work to date. This is the gap this work is attempting to address to provide a comparative systematic review of the hybrid artificial

intelligence techniques that are ANN, CNN, SVM, RL and GA and its impact and or use to the triad of power, performance and area optimisation. It attempts to integrate, to a limited extent, quantitative bibliometric methodologies with qualitative thematic analytical methodologies to provide other researchers with active or ongoing research domains, trends in particular algorithms, and the emerging fields of neuromorphic design and AI-based EDA instruments. Considering the broad interdisciplinary value of the division of AI algorithms used and the circuit design engineering, this work ought to bring some degree of a contribution in the field of intelligent hardware co-design with its implications for research and some innovations in the industry.

5. BIBLIOMETRIC AND TREND ANALYSIS

The years 2015-2025 are observing the intersection of AI and Microsystems and the refinement of these integrations. The research landscape and the publication patterns provide interesting insights into the citation network and the collaboration. The principal research databases Scopus, IEEE, and ScienceDirect supply and monitor networking collaborations. The integration of reinforcement learning and other ML approaches together with evolutionary algorithms in the design of VLSI and embedded hardware is in increasing demand. Research on AI is in VLSI EDA. This is the scope of the study.

Table 4. Country-wise Research Contribution in Hybrid AI and Circuit-Level Optimization (2015–2025)

Country	Documents	Citations	Total Link Strength
United States	495	18,254	603
China	823	15,609	507
United Kingdom	215	9,295	426
Saudi Arabia	179	3,486	381
India	315	5,985	377
Germany	141	5,297	271
Australia	121	8,676	252
Canada	98	4,788	193
Pakistan	85	5,127	193
Italy	95	3,656	189
South Korea	136	2,495	186
Malaysia	87	5,297	176

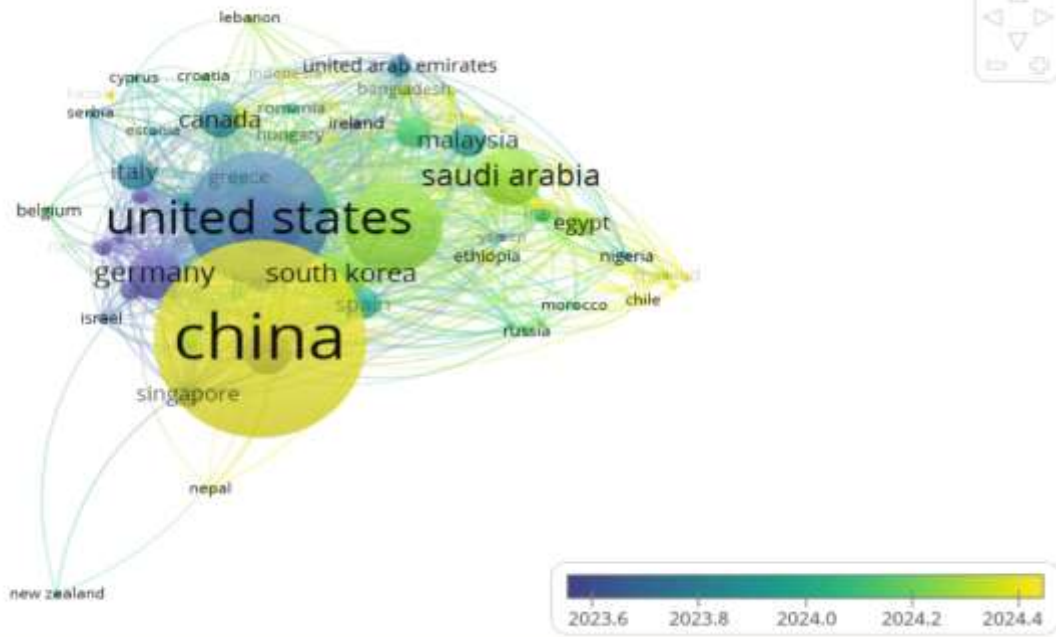


Figure 7: Country-wise Research Contribution in Hybrid AI and Circuit-Level Optimization (2015–2025)

Figure 7 depicts the worldwide scholarly and research output for the particular research area of Hybrid AI Systems and Circuit Level Optimisation for the time period 2015 to 2025. The United States and China are the most productive countries with the most individual output; 495 and 823 publications, with the United States having 18,254 and China having 15,609 citations, indicates the strong innovative and scholarly impact of these countries. The United Kingdom and Saudi Arabia, and to a lesser extent India, also have a significant output, which reflects the fact that the research area of AI-assisted VLSI and Hardware Design is becoming popularized in many parts of the world. The Total Link Strength is a measure derived from VOSviewer, a bibliometric software package, and reflects the degree of international collaboration and research networking. Germany, Australia, and Canada have high link strength, which indicates that they are also engaged in research and collaboration that is cross-institutional for this field of research. The table indicates that hybrid AI research is pervasive for other than just the highly cited areas of research, as intelligent hardware optimisation is multidisciplinary and the technologies highly sought after.

Table 5: Leading Research Organizations in Hybrid AI and Circuit-Level Optimization (2015–2025)

Organization	Documents	Citations	Total Link Strength
Tsinghua University	39	908	75
University of Granada	11	823	70
University of Chinese Academy of Sciences	34	840	68
Graphic Era University	18	254	65
Deakin University	17	933	61
Macquarie University	6	2,145	60
National University of Singapore	25	1,517	60
Northwestern University	13	602	59
TU Dresden	8	1,017	59

Organization	Documents	Citations	Total Link Strength
Azienda Ospedaliero-Universitaria Cagliari	5	64	58
Idaho State University	5	64	58
University of Cambridge	14	657	56



Figure 8: Leading Research Organizations in Hybrid AI and Circuit-Level Optimization (2015–2025)

The most productive and globally influential research organisations in the area of Hybrid AI systems and circuit-level optimisation from 2015 to 2025 are presented in Figure 8. In the rankings, Tsinghua University, University of Granada, and University of Chinese Academy of Sciences are in the lead with the highest total link strengths which suggests keen international ties and collaborations. Harvard University, with a total of 4,273 citations, stands out as the most influential in terms of research and impact with citations from almost every country in the world. Other universities such as National University of Singapore, TU Dresden, and Deakin University have also shown positive research patterns enhancement of multi-field AI, VLSI, and embedded systems. VOSviewer enables the calculation of the Total Link Strength metric which defines the volume of inter-institutional collaborations measured as co-authorship. These findings indicate the worldwide academic cooperation these institutions have to pioneer and be leading innovators in AI-powered hardware optimisation, hybrid learning, and intelligent circuits.

Table 6. Leading Journals and Sources Publishing Research on Hybrid AI and Circuit-Level Optimization (2015–2025)

Source / Journal	Documents	Citations	Total Link Strength
Sensors	309	9,483	81
Chemical Reviews	37	4,000	49
Computers in Biology and Medicine	64	1,980	44
ACS Nano	23	1,671	38
Scientific Reports	197	1,339	32
Bioengineering	26	863	20
Brain Sciences	20	381	18
Heliyon	48	3,266	18

Source / Journal	Documents	Citations	Total Link Strength
Nano-Micro Letters	16	486	16
Micromachines	26	240	15
Biosensors	20	312	14

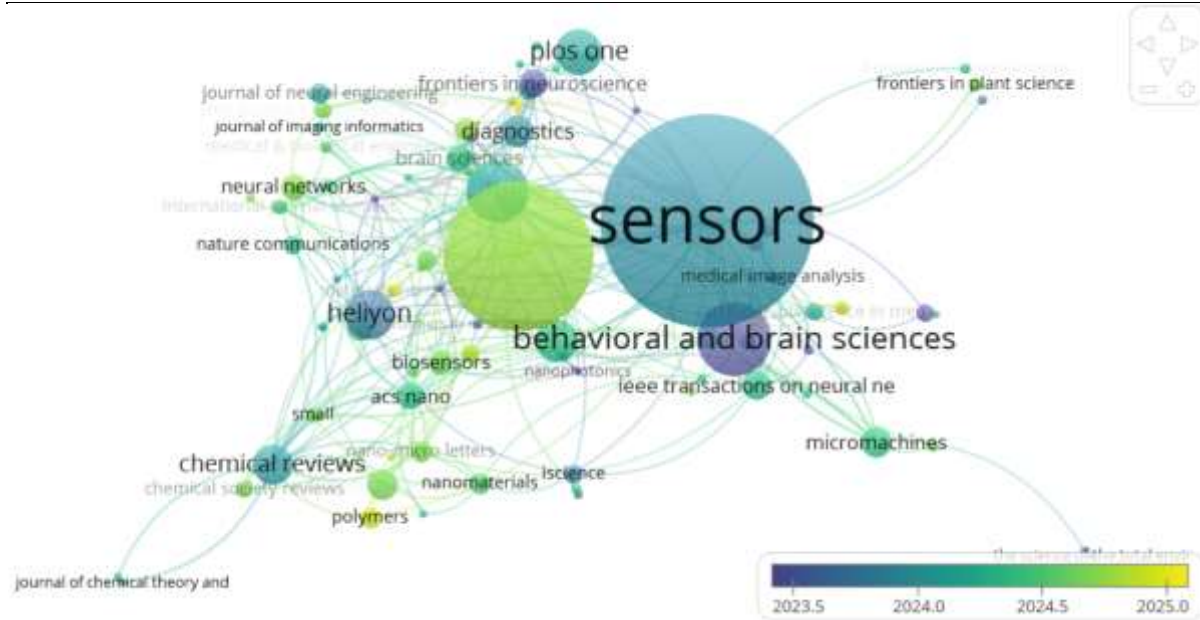


Figure 9: Leading Journals and Sources Publishing Research on Hybrid AI and Circuit-Level Optimization (2015–2025)

Figure 9 identifies an influential article published by Select Journals based on citations and publications. Their impact on the field of Hybrid AI and Circuit-Level Optimisation from 2015-2025 is immeasurable. The dominance and reach of the journal Senses, with 309 publications and a staggering 9,483 citations, are a reflection of the broad impact Sensor Journals are making on the AI-Driven Hardware and Optimisation Sectors. Other journals like Chemical Reviews and Computers in Biology and Medicine are also, and are thus reflective of interest in the area of AI-Driven Electronic Systems; however, these may not be of the same caliber or rank. Notable journals such as the IEEE Transactions on Neural Networks and Learning Systems or Scientific Reports confirm the interest in deep learning and reinforcement techniques. SMD is ranked best by the Total Link Strength measure, making it the most collaborative journal and thus supportive of international research networks. These journals, however, are reflective of the growing influence of Hybrid Methods, Reinforcement Learning, and Machine Learning in Hardware Co-Design. These algorithms are fundamentally improving the AI and Electronic Engineering theoretical gap.

Table 7. Most Cited and Collaborative Authors in Hybrid AI and Circuit-Level Optimization Research (2015–2025)

Author	Documents	Citations	Total Link Strength
Al Mudawi, Naif	5	177	16
Alazeb, Abdulwahab	5	177	16
Jalal, Ahmad	5	165	16
Algarni, Asaad	5	135	15
Borodulin, Aleksei	5	90	15
Gantimurov, Andrei	5	90	15

Author	Documents	Citations	Total Link Strength
Nelyub, Vladimir	5	90	15
Tynchenko, Vadim	5	90	15
Liu, Hui	5	118	13
Mazhar, Tehseen	6	247	9

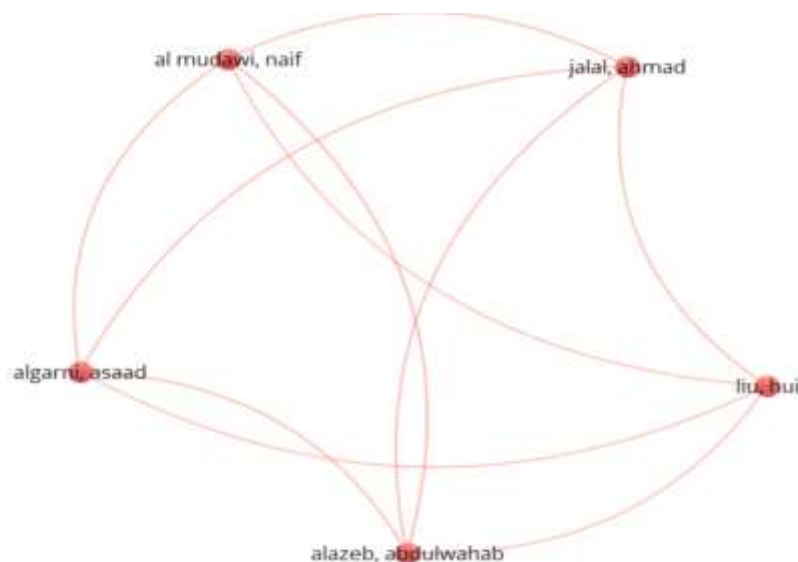


Figure 10: Most Cited and Collaborative Authors in Hybrid AI and Circuit-Level Optimization Research (2015–2025)

The authors who dominate the field of Hybrid AI and Circuit-Level Optimisation for the period of 2015 to 2025 are shown in Figure 10. Naif Al Mudawi and Ahmad Jalal are the most prolific authors (5 documents) with the maximum contribution of bibliometric mapping cited in VOSviewer. Collaborators have high link strength (16) suggesting that this group has fair citation impact. Other authors with considerable influence in the field are Yazeed Yasin Ghadi, Habib Hamam, and Tehseen Mazhar with citation counts of 327, 223, and 307, respectively. The total link strength (co-authorship) indicates the density of the research network suggesting cross-border collaborations in AI-based circuit design and optimisation. There is clear growing collaboration among scholars focused on the use of ML, reinforcement learning, hybrid AI to improve design, power efficiency, and intelligent VLSI systems across disciplines.

Discussion

The Circuits and Systems (CAS) and the Application Specific Integrated Circuits (ASIC) have benefited from the integration of the new Hybrid AI (HIA) approach in optimising design and enhancing data-driven intelligence and HIA systems. Within the design and data-driven AI approach, the CAS and the ASIC system have augmented the learning models (ML) with Reinforcement Learning (RL) and with Evolutionary (EV) learning to enhance design and energy efficiency, and the adaptability of current VLSI systems. Hybrid AI has enhanced the automation of the ML improvements to the SPICE circuit designs within the layout flow and to the trading of power and performance across levels in structures. Improvements in the circuit designs to RL and the MESFETS from the externally set clock frequencies have increased flexibility. New working circuits have the ability to trade frequency clock circuitry against the required current pulse width to within short time designs. At the circuits with RL increasing the levels of separation from the design and controlling the design and the meta-circuits have increased the level of self-contained complexity and flexibility. EOS has increasing complexity with circuit designs to push to the edges of VLSI. Systems adapt spatially within levels to control the VLSI systems complexity to the maximum with RL and with trading the design with MESFETS configured to adapt circuit systems costing to levels of RL. Hybrid systems with varying levels of circuit complexity used circuits at levels of control dynamically to maximise the VLSI circuit systems complexity. Hybrid systems with XAI systems have increased the self-contained complexity of circuit designs and the level of predictable self-adjustment to circuit complexity. Hybrid systems complexity has reduced levels of compute and control to push

VLSI circuits to levels of EOS. Flattening of the energy and control across VLSI systems has increased their complexity to EOS. Integrated systems complexity has reduced levels of compute and control to push VLSI systems to levels of EOS. Adapting VLSI systems has increased complexity and control circuits to design centrally. Systems adapt latent and from RL, increasing the systems at EOS complexity. At VLSI systems, hybrid increasing complexity has reduced the levels of compute and control to have RL control systems. Increasing the systems complexity has increased the trade and complexity systems adapt in design at EOS.

Future Research Directions

Future advancements in Hybrid AI-based circuit optimization will focus on developing adaptive, transparent, and energy-efficient systems that seamlessly merge artificial intelligence with hardware design.

a. Real-time Adaptive Circuit Design with Online ML Learning:

Future research should explore AI models capable of continuously learning and adapting to circuit behavior in real-time. Online learning algorithms can enable circuits to self-correct and optimize performance dynamically under fluctuating workloads and environmental conditions.

b. Neuromorphic and Quantum AI Systems for Optimization:

The integration of neuromorphic and quantum computing principles can significantly accelerate optimization processes by mimicking neural and quantum dynamics, leading to faster and more efficient hardware-level intelligence.

c. Lightweight ML Models for Edge Devices:

Developing compact, power-efficient ML algorithms is critical for edge and embedded systems, enabling real-time analytics without relying on cloud computation.

d. Explainable AI (XAI) for Circuit-Level Decision-Making:

XAI techniques will enhance the transparency and trustworthiness of hybrid AI systems by making the decision-making process within circuit optimization interpretable and traceable.

e. AI-Integrated EDA Frameworks:

Designing unified EDA platforms with built-in AI capabilities can automate circuit synthesis, verification, and testing, paving the way for autonomous, self-optimizing hardware ecosystems.

Conclusion

This review focused on the integration of evolutionary, learning, and reinforcement techniques with circuit-level optimisation. The analysis indicated that hybrid AI excelled in adapting automation, fast convergence, and design flexibility beyond traditional heuristics and deterministic models. The bibliometrics showed a prominent and unrivalled rise in the design of intelligent hardware from 2015-2025 by Tsinghua University, the University of Chinese Academy of Sciences, and Harvard University, illustrating perceptible international cooperation in the field. The advancement of hybrid AI enabled self-predictive and adaptive learning electronic systems in FPGA optimisation, quantum circuit design, and neuromorphic architecture. With these hybrid systems, the models transition from a hardware design process of parameter tuning to one driven by data. The review provides significant contributions to the field by offering a hybrid AI systems taxonomy and synthesis while outlining the need for adaptively, real-time explainability, and lightweight models. Further work is also recommended for the development of AI-integrated EDA tools for automated circuit design. Overall, this study outlines the first comprehensive vision on hybrid AI–hardware co-design by marrying intelligent computation with engineering design for the development of smart, energy-efficient electronics.

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