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A VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter

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Abstract: ***A FIR filter is used in digital signal processing to eliminate undesirable components or noise from a signal. In order to efficiently eliminate noise from the received channel data bits, this work presents the VLSI architecture of a Multi-Standard Digital Up Converter (DUC) based FIR filter. In the accumulation unit's existing architecture, carry skip addition was utilized. Shift add architecture is used in this proposed architecture to achieve an efficient adaptation delay, area, and power implementation.***

The architecture is designed using Carry look ahead adder, which is used in the accumulation unit. The results demonstrate that the proposed technique produces less area and power consumption than the existing DUC based RRC filter architecture. In this project, the suggested filter is implemented using the VERILOG programming language in Xilinx ise 14.7. In this project, the FIR filter's VERILOG coding is used, and simulation is used to view waveforms.

The increasing need for high performance and low power DSP is a result of the multimedia applications' rapid expansion. The RRC digital filter is the primary component of a DSP system that is most frequently employed.

Keywords— CarrySkipadder, DigitalUpconverter, Carry look ahead adder

I. INTRODUCTION

A filter is a network that selects frequencies. It attenuates the other frequencies while passing through a certain band. Analog and digital filters are categorized based on the type of inputs and outputs. Depending on the impulse response, filters are further divided into infinite and finite impulse response filters. The sorts of filters arbiter briefly discussed in this chapter. Active and passive analog filters are available. Only resistors, capacitors, and inductors are used in passive filters. When a low pass or band stop filter needs to pass a sizable amount of direct current (about 1 mA), passive designs are typically employed. Additionally, they are more frequently utilized in specialized settings where a wide dynamic range is required, like high-frequency filters. (The dynamic range is the difference between the highest signal level and the background noise floor.) Furthermore, passive filters use no power, which is advantageous in low-power systems.

Using passive filters with inductors has several drawbacks, the primary one being their bulk. This is especially true if they are intended to carry high currents, as the core needs to have the capacity to handle the magnetic flux and big diameter wire for the windings.

(a)Analog filters

Active and passive analog filters are available. Only resistors, capacitors, and inductors are used in passive filters. When a low pass or band stop filter needs to pass a sizable amount of direct current (about 1 mA), passive designs are typically employed. Additionally, they are more frequently utilized in specialized settings where a wide dynamic range is required, like high-frequency filters. The difference between the maximum signal level and the background noise floor is known as the dynamic range.

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one being their bulk. This is especially true if they are intended to carry significant currents, as they require big diameter wire for the windings and a sufficiently sized core to handle the magnetic flux.

Operational amplifiers are the "active" component of active analog filters; they come in a variety of package forms. To create a filter with the right frequency response, op-amps are coupled with resistors and capacitors. They do not utilize inductors as a result. The filter's performance may be limited because all op-amps have gain and bandwidth restrictions. Wide bandwidth op-amps have opened the door for active filter designs, which were previously limited to frequencies under 100 kHz. Today, filter designs can reach several megahertz. They are therefore appropriate for filtering video signals.

(b) Digital Filters

Digital filters are widely employed in the electronic industry as a whole. This is because, while analog filters introduce more noise into the signal at each intermediate stage of the transform, digital filters execute noiseless mathematical operations. As a result, digital filters have the potential to achieve significantly higher signal to noise ratios than analog filters. In communication architectures, digital filters have shown to be a potent solution for eliminating noise, modifying the spectrum, and reducing inter-symbol interference. These filters have gained popularity because design engineers can achieve performance levels with them that are challenging to achieve with analog filters thanks to their precise reproducibility. It is possible to build digital filters using three basic mathematical procedures.

(C) IIR Vs FIR

The two most popular types of filters are FIR and IIR. IIR filters have the limitation that their closed-form designs are initially restricted to low pass, band pass, and high pass filters. Moreover, these designs typically ignore the filter's phase response. Consider an elliptic low pass filter, which can provide great amplitude response qualities with a very simple computational process, but an extremely nonlinear phase response. Approximately constant frequency response magnitude and zero phases in that band are desired for building filters and other signal-processing systems that pass some section of the frequency range undistorted. Zero phases are not achievable for casual systems; as a result, some phase distortion needs to be permitted.

FIR filters are capable of accurate linear phase as opposed to IIR filters. Furthermore, there are no closed-form design equations for FIR filters. Although the window method is simple to apply, it could take some repetition to satisfy a required specification. With minimal more effort compared to designing low pass filters, it is possible to approximate more arbitrary frequency response characteristics using the window method and the majority of computational techniques. Furthermore, there exists an optimality theorem for FIR filters that holds significance in several real-world scenarios, suggesting that the design problem for FIR filters is considerably more manageable than the IIR design problem. Consequently, it is necessary to permit some phase distortion.

II LITERATURE SURVEY

Digital filters are widely used in audio applications. S. D. S. M. Mehendale and G. Venkatesh, "Synthesis of multiplier-less FIR filters with minimum number of additions," Therefore, excellent digital filter performance should be considered essential for audio system application design. As opposed to basic filters, which use computerized filters that use a limited exactness number juggling to register the filter reaction, digital filters use accuracy with limited precision for speaking to signals. Here, the VERILOG dialect has been used to realize the FIR-filter in Xilinx ISE. must be permitted.

L. Aksoy, C. Lazzari, E. Costa, P. Flores, and J. Monteiro, "Algorithms, architectures, and a CAD tool for the design of digit-serial FIR filters," The creation of low-complexity bit-parallel multiple constant multiplications (MCM) operations, which dominate the complexity of many digital signal processing systems, has seen the introduction of numerous effective algorithms and architectures throughout the past 20 years. Dialect in VERILOG must be permitted.

"Digital filter synthesis based on minimal signed digit representation," by C. Park & H. J. Kang Numerous studies have concentrated on reducing the complexity of multiplier blocks, which compute the constant coefficient multiplications needed in filters, since the amount of multiplications in digital filters determines their complexity. Using an efficient number system can greatly minimize the complexity of multiplier blocks.

In "Comparison of Parallel Prefix Adder," Nurdiani Zamhariu, Peter Voon, and Kuryati Kipli discuss how VLSI integer adders are used in memory addressing units, microprocessors, and arithmetic and logic units (ALUs). The microprocessor's minimum clock cycle time is frequently determined by the adder's speed. Because a Parallel Prefix Adder (PPA) is faster than a ripple carry adder, it is necessary. The PPA adder family is a descendant of the widely used carry look ahead adders. Wider word length additions are best suited for these adders.

III METHODOLOGY

A comprehensive literature review is the first step in the process of creating an effective VLSI architecture for a reconfigurable pulse-shaping FIR interpolation filter for multi-standard Digital Up Converters (DUC). This helps to gain an understanding of the current FIR filter architectures and pulse-shaping methodologies. The project then goes on to establish the filter specifications, emphasizing reconfigurability for different standards.

A high-level system design is crafted, incorporating mathematical modeling to derive key filter characteristics. The design is simulated using tools like MATLAB to validate performance metrics. Next, the RTL implementation is developed in VHDL or Verilog, followed by synthesis and layout design to prepare for fabrication. Functional verification is performed through simulation, with post-layout checks ensuring design integrity. Finally, the architecture is evaluated for performance and optimized based on testing results, with documentation of findings and suggestions for future enhancements.

VLSI Architecture Design

- **Modular Design**: Break the system into key components—FIR filter, interpolation logic, and reconfiguration control unit.
- **Data Path Optimization**: Design an efficient data path with pipelining and parallelism to meet speed and throughput requirements.
- **Coefficient Memory**: Develop a memory structure for dynamically loading coefficients to switch between different communication standards.
- **Control Logic**: Create a control unit to manage reconfiguration, coefficient selection, and interpolation factor adjustments.

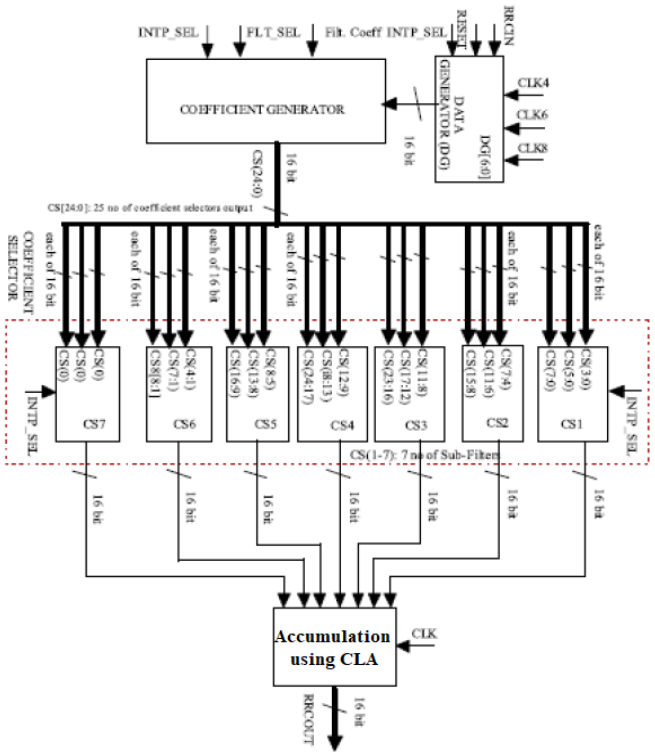

Fig1 : Proposed Architecture

1.Data Generator Block:

When the data generator receives a clock signal, it samples the input data (RRCIN) according to the multiplexer parameter's selection lines (INTP_SEL).

2. Coefficient Generator Block:

First and second coding passes, shift and add architecture, multiplexer unit lines of multiplexer parameter (INTP_SEL), and other components make up the coefficient generator. and the addition unit is displayed in Figure. The coefficient generator (CG) multiplies the values between the inputs and the filter coefficients. The two-phase optimization technique has resulted in a reduction of the hardware. Multiplexers are utilized in the structure of every block within the Coefficient Generator.

3. Coefficient Selector Block:

The coefficient generator picks the necessary data for processing, and the inputs are obtained from its output. The chosen inputs are then multiplied using the AND operation, and outputs are generated based on the selection line of the multiplexer.

4. Final Accumulation Block:

The data generator (DG), coefficient generator (CG), and coefficient selector (CS) outputs were used as the inputs for accumulation. These outputs were then combined to create the filter output.

IV ADVANTAGES

It offers significant advantages by providing a flexible, high-performance, and power-efficient solution for modern communication systems. Its reconfigurability allows seamless adaptation to various communication standards, such as GSM, LTE, and 5G, reducing hardware complexity and development costs. The architecture optimizes resource usage, minimizing chip area and power consumption while ensuring real-time signal processing with low latency. It enhances signal quality through pulse shaping and supports scalability, making it suitable for evolving technologies in mobile, IoT, and future communication networks.

V APPLICATIONS

RRC (Root Raised Cosine) filters find applications primarily in digital communications systems, especially in the context of pulse shaping for data transmission. Here are some key applications:

1. **Digital Communication Systems:**

   Symbol Shaping: RRC filters are used to shape the transmitted symbols in communication systems to minimize intersymbol interference (ISI). By controlling the bandwidth and spectral efficiency of the signal, RRC filters help in achieving better performance in terms of bit error rate (BER) and signal-to-noise ratio (SNR)

2. **Filtering and Equalization:**
   - **Channel Equalization:** RRC filters can be used in receiver-side equalization to compensate for the frequency-selective nature of the channel and to mitigate ISI caused by multipath propagation.
3. **Digital Broadcasting:**
   - **Digital TV and Radio:** RRC filters are employed in digital broadcasting standards like DVB (Digital Video Broadcasting) and DRM (Digital Radio Mondiale) to shape the transmitted signals, ensuring high fidelity and robustness against channel impairments.
4. **Software-Defined Radio (SDR):**
   - **Signal Processing:** In SDR applications, RRC filters are implemented in software to process received signals, enabling flexibility in adjusting filter parameters without hardware changes.
5. **Cognitive Radio:**
   - **Dynamic Spectrum Access:** RRC filters can be used in cognitive radio systems to adaptively shape signals based on spectrum availability and interference conditions, optimizing spectrum utilization.

VI SIMULATION AND RESULTS

Ultimately, the digital architecture for the FIR filter with a 16-bit channel basis was created. The purpose of this architecture is to lower the received signal's noise level. Next, calculate the circuit complexity, power, and speed level while simulating the binary end output results. Xilinx ISE 14.2 has been used to simulate the suggested design on ISIM. Following the input of binary data, a corresponding clock signal of either 0 or 1 is applied. Waveforms are produced in response to their respective inputs.

RTL SCHEMATIC: - The register transfer level, or RTL schematic, is an acronym for the architecture's blueprint and is used to compare the planned architecture to the ideal architecture that still needs to be developed.

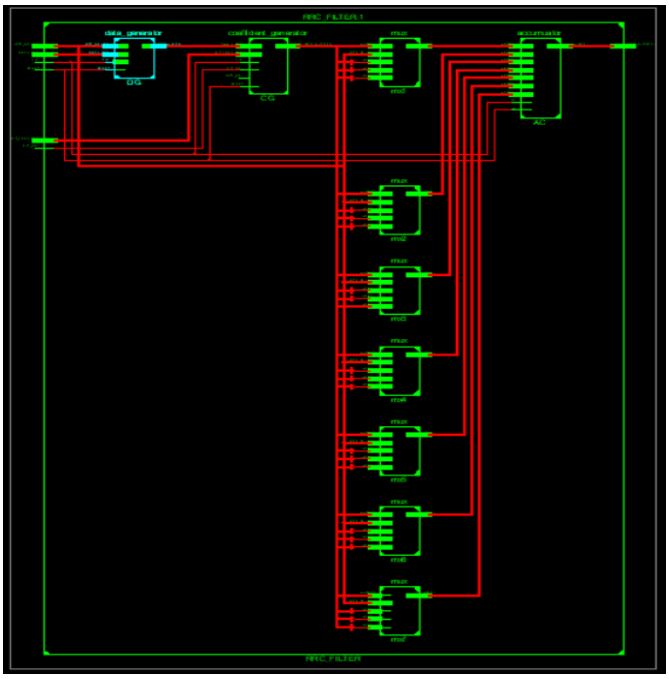

Fig2 : RTL Schematic of existing RRC filter

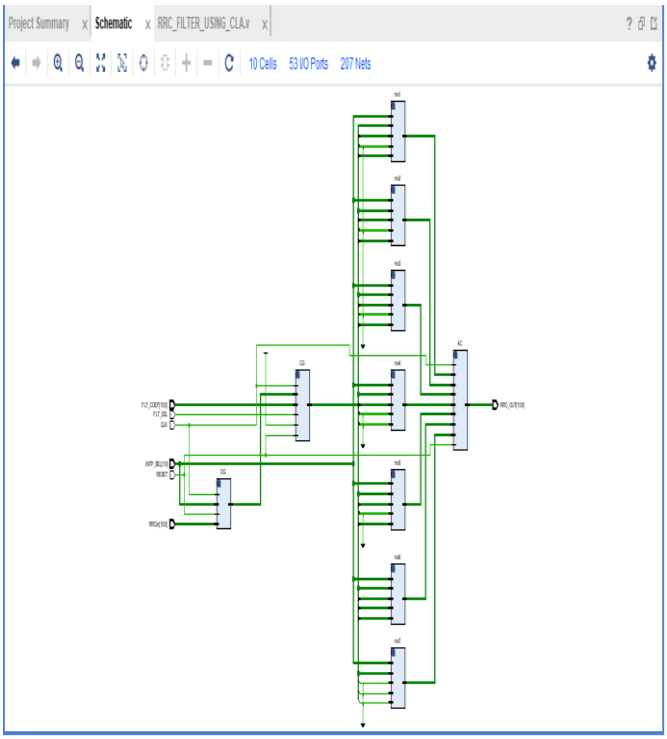

Fig3: RTL Schematic of Proposed RRC Filter

From the above figures we understand that the area occupied by the filter is reduced and it can be interpreted using the look up tables that are shown in figure 7. In the figure we have mentioned only the proposed values and the LUT's have been reduced from the existing architecture of the filter.

Fig4: Technology Schematic of proposed RRC Filter

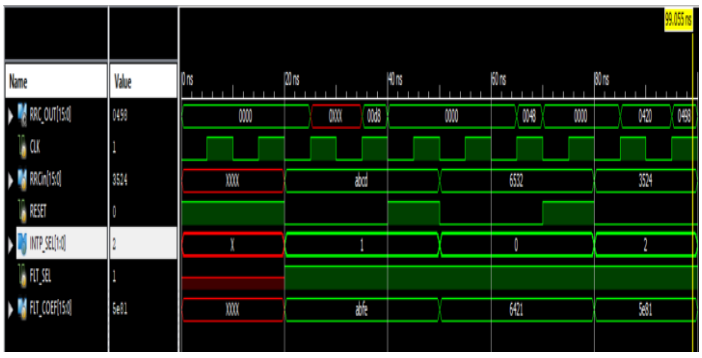

Fig5: Simulated Waveforms of proposed RRC Filter

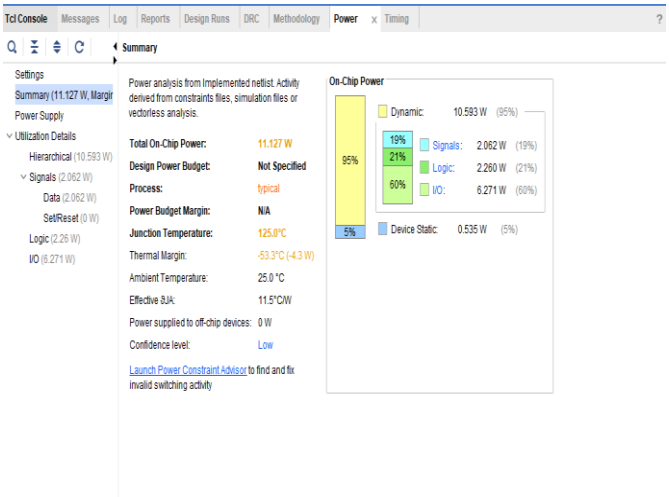

Fig6: Power Obtained

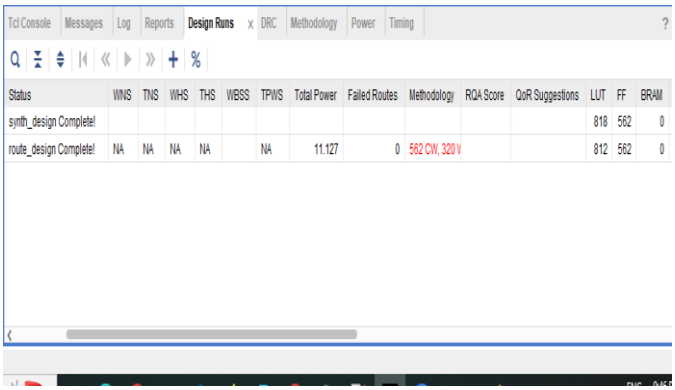

Fig7: Parameters

VII CONCLUSION

Ultimately, a multi-standard channel filter architecture for the FIR with DUC was devised. Both the delay and the degree of circuit complexity were decreased. It is possible to effectively eliminate noise from the received channel data bits by using this FIR filter architecture. This architecture tackles many issues that arose during the design of the reconfigurable filter utilized in the multi-standard DUC, a crucial part of cognitive radio and software-defined radio. The quantity of Look Up Tables (LUTs), power, and path delay.

This two-step optimization technique improves the design's operating clock frequency while simultaneously decreasing space and power consumption to achieve the desired filter's desired level of efficiency. The advantages of the suggested architecture over the current reconfigurable RRC filter architecture in terms of speed, power, and area consumption are shown by comparisons of its results with those of other reconfigurable FIR filter architectures implemented on FPGA. In addition, an efficient power and area architecture for the reconfigurable RRC filter has to be improved.

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