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A ZVZCS Full-Bridge Converter for MVDC Collection Systems Using Renewable Energy

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Abstract

This study proposes a full-bridge DC-DC converter incorporating zero-voltage zero-current switching (ZVZCS), based on a dual-transformer structure with two output filter capacitors. The converter is designed for seamless integration with DC collection systems in medium-voltage renewable energy applications, where stability, adaptability, and efficiency are crucial.

The primary switches operate under a pulse width modulation (PWM) scheme with a fixed duty cycle to regulate voltage and power output. Under full load conditions, the main full-bridge circuit delivers the majority of the power and achieves zero-voltage switching (ZVS) due to the precise design of the main transformer's turn ratio, significantly minimizing switching losses.

To complement this, an auxiliary circuit achieves ZVZCS and handles a small fraction of the power. Efficiency can be further improved by optimizing the auxiliary transformer's turns ratio, balancing power contribution and minimizing conduction losses.

In addition to conventional control methods, a fuzzy logic controller is incorporated to enhance real-time adaptability. The fuzzy controller dynamically adjusts control signals based on varying input voltage, load conditions, and switching timing, allowing the converter to maintain soft-switching conditions even under transient disturbances or parameter drift. It replaces rigid threshold-based decision-making with linguistic rules, enabling smarter handling of system nonlinearity and uncertainty.

Design characteristics, fuzzy rule base definition, and optimization strategies for the proposed converter are described in detail. To validate the effectiveness of the proposed scheme and verify the simulation results, a 200 V / 2 kV / 3 kW prototype has been developed and tested. The results demonstrate improved switching performance, better thermal management, and higher overall efficiency due to the combined use of ZVZCS and fuzzy logic control.

I. OVERVIEW

Researchers from all around the world have been paying attention to renewable energy sources because of the alarmingly growing impact of gas emissions and pollution on the environment. Large solar photovoltaic (PV) systems and offshore wind farms are examples of renewable energy sources that are primarily connected to grid stations at medium voltage levels before being stepped up to high voltages for the bulk transmission and distribution of electrical power [1], [2]. It is evident that MVDC offers notable advantages over MVAC when comparing the medium voltage AC (MVAC) and medium voltage DC (MVDC) voltages for large-scale integration of renewable energy sources. Higher efficiency, greater stability, reduced system weight, cheap cost, and no reactive power are some of these benefits [3], [4]. Therefore, MVDC technology is advised for the extensive integration of renewable energy sources. Additionally, the DC power output from renewable energy sources facilitates the integration of different sources with the MVDC collection system. Reactive power correction and frequency stability are not issues with this technology. As a result, this DC collection system represents the power systems of the future. In the literature, several kinds of electronic DC-DC converters with high gain power have been proposed. For MVDC systems, non-isolated power electronic DC-DC converters have been documented in [5] and [6], providing benefits like reduced power rating. In [7], a

switched-capacitor DC-DC converter with a low power rating and output capacitance was published. Using a soft-switching topology for their resonant switched-capacitor power electronic converter, [8] has demonstrated a high efficiency and low switching loss converter. The utilization of passive components, which lead to power losses and high voltage strains when utilized for high voltage applications, is the primary disadvantage of employing these non-isolated power electronic DC-DC converters. Depending on the voltage levels, such as medium-to-high, a frequency transformer can be used to isolate the power electronic DC-DC converters. This galvanic isolation eliminates the requirement for high-voltage switches and reduces the amount of protection needed in renewable energy sources. For high power applications, such as phase shift full-bridge converters [9], [10], [11], LCC series-parallel resonant converters [12], [13], single active type bridge converters [14], [15], and three phase dual active bridge DC-DC converters [16], isolated power electronic DC-DC converters have thus been frequently selected. For high-power applications, the full-bridge construction is used to build the aforementioned converters. Two methods are employed to accomplish soft-switching for these full-bridge converter topologies. To attain a high gain, they lower the power and switching losses. The ZVS is the first method [11], [17], and [18]. ZVZCS is the second method [19], [20]. ZVS is best suited for MOSFETs because of their high parasitic capacitance [13]. MOSFETs are typically used in low power applications because of their constrained voltage and current ratings. However, IGBTs are becoming more common for high power applications since they provide higher current and voltage ratings than MOSFETs. However, the tail current effect affects the IGBTs [21], [22]. The zero-current switching (ZCS) technique minimizes the tail current effect by lowering the turn-off switching loss [23], [24]. However, the current must drop to zero before the commutation occurs in order to attain ZCS. Either the resonance mode [25] or the current reset mode [26] do this. Through modifications to the converter's structure, the auxiliary circuits of [27] and [28] have attained the resonance mode. ZCS can be achieved with the help of resonance techniques, such as the LCC resonance type, and the switch's frequency can be adjusted to control the output voltage [29]. These auxiliary circuits' primary flaw is their electromagnetic compatibility and inductive filter design. grows more intricate when variable switching frequency is applied [29], [30]. Interleaving currents are used by the single active bridge converter in [15] to lessen the ripple in the output current. The primary disadvantage of this approach is that the high switch turn-off currents lower conversion efficiency. A soft-switching study across a wide range of operation was offered by the three phase dual active bridge converter that was proposed in [16]. It is less appropriate for high voltage applications, though, because the switches must endure high voltage pressures. In order to achieve ZCS, the researchers in [31] proposed a topology for the primary IGBT switches that uses full-bridge cells and a dual transformer. Conduction loss and the transformer, however, rose as a due to the triangle current's enormous amplitude. Consequently, the design of the inductive filter becomes intricate and expensive to produce. The efficiency is significantly impacted by all of these restrictions. The converter's viability and practicality. A full-bridge ZVZCS DC-DC converter based on a dual transformer with two output filter capacitors is suggested in this research; it is especially appropriate for medium-voltage DC collecting systems that use renewable energy. To achieve power and voltage management of the entire converter, the auxiliary circuit uses pulse width modulation, or PWM. This enables the fixed duty cycle operation of the basic full-bridge four switches, which offers the benefit of easy control. Through optimization, the primary transformer and primary full-bridge converter's turns ratio can transfer a sizable amount of power while also achieving ZCS within the entire load range. The switching losses are significantly decreased as a result. To further lower converter losses and raise conversion efficiency, the secondary transformer's turns ratio can also be adjusted. Additionally, the converter avoids the use of large inductance and high voltages by using output capacitive filtering for medium and high output voltages. The structure of this document is as follows. The suggested converter's circuit architecture and working principle are presented in Section II. Section III reports on the parameter design. The simulation analysis used to verify the suggested converter's design is shown in Section IV. to confirm the efficacy of the suggested topology and the simulation results.

II. DESIGN AND OPERATION PRINCIPLE OF CIRCUITS

For high power applications, IGBTs are accommodated

by the full-bridge converter structure. ZVZCS can be implemented for the switches to function with a 50% fixed duty cycle and achieve great efficiency at high power levels without the need for extra control circuitry. This is used in the discontinuous conduction mode (DCM), which is typically found in traction systems and resonant transformers. Its primary flaw, though, is that this state cannot be sustained in high power applications. An auxiliary circuit is implemented in Fig. 1 to overcome the aforementioned limitation, enabling the IGBTs to function through their control.

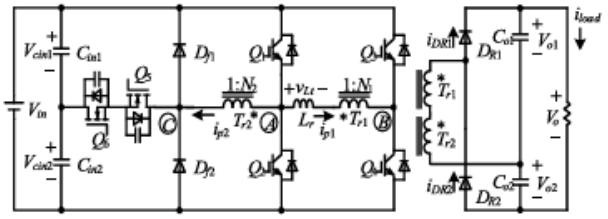


FIGURE 1. Proposed converter.

where both the voltages and currents will drop to zero in DCM. It is possible to reduce the control current and switching losses by modifying the transformer turns ratios so that a smaller current passes through the auxiliary switches and a larger current passes through the main switches. A ZVZCS full-bridge converter is suggested based on the analysis above. The suggested converter is in charge of ZVZCS function, as illustrated in Figure 1. Four primary IGBT switches (Q1–Q4), an inductor (Lr), and a transformer (Tr1) with a turns ratio of N1 make up the full-bridge circuit. Two MOSFET switches (Q5 and Q6), capacitors Cin1 and Cin2, diodes for freewheeling operations Df1 and Df2, and a transformer Tr2 with a turns ratio N2 make up the auxiliary circuit. The connection between the transformers' two secondary terminals is shown in Fig. 1. This is done in order to obtain a voltage-doubler rectifier circuit input where the current stays constant. The power is distributed so that the full-bridge converter provides around 90% of the power and the auxiliary circuit provides the remaining 90%.

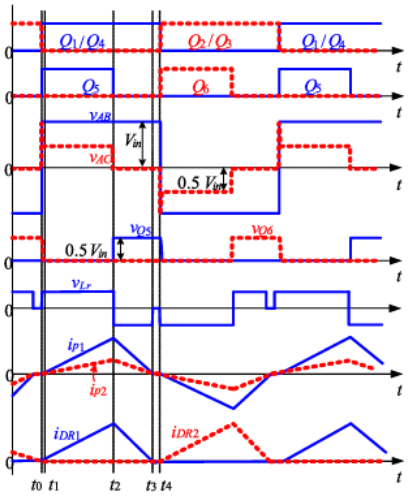


FIGURE 2. Key waveforms of the proposed converter.

The main waveforms of the suggested converter are displayed in Fig. 2. The gating pulse substitutes for the Q1, Q4, Q2, and Q3 switches having sufficient dead time and a predetermined duty cycle of 50%. Q1/Q4 and Q2/Q3 transitions are not in phase. PWM-based control, which operates on the leading edges of Q1, Q4, is utilized for the switches Q5, Q6. The duty pulses of Q5 and Q6 regulate the output voltages of the suggested converter. The analyses are predicated on the following assumptions:

1) Every semiconductor device in use is regarded as an ideal device.
2) Since the values of the input capacitors Cin1 and Cin2 are maintained constant, Vcin1 = Vcin2 = Vin/2.

3) To help the output voltage attain a constant state where Vo1 = Vo2 = Vo/2, the filter capacitors Co1 and Co2 are maintained at the same high value.
4) Because of its low value, the auxiliary transformer Tr2's leakage inductance is considered insignificant.

To keep things simple, we will simply talk about the proposed circuit's half-cycle. Fig. 3 displays the converter's four operating modes. At time t0, the new switching cycle begins. The switches Q1, Q4, and Q5 are turned ON and Q2, Q3, and OFF at the moment of t0. Before the start time instant t0, no current passes through any of the switches. ZCS is used to turn the switches Q1, Q4, and Q2, Q3, ON and OFF, respectively. Additionally, the voltage across Q6 is Vin/2, but the voltage across Q5 is zero, meaning it is turned-on with ZVZCS. The following is the presentation of the full analysis:

Mode 1: This mode runs between t0 and t1. vAB = Vin is the outcome of the principal current ip1 from Tr1 flowing through Q1, Q4, Lr, Tr1, and Cin1. In a similar manner, the windings of Q1, Q4, Q5, Tr2, the parasitic capacitance of Q6, and Cin1 receive the principal current ip2 from Tr2. vAC = 0.5Vin is the consequence of the voltages across Q6 discharging from 0.5Vin to zero at instant t0. Current ip1 flows through Q1, Lr, Tr1, and Q4, whereas ip2 flows through Tr2, Q5, and Q1, as seen in Fig. 3(a). Consequently, the current flowing via switches Q1 and Q4 is equal to the total of ip1 and ip2.

Mode 2: This mode runs between t1 and t2. The current ip2 also passes through the switch Q6's body diode since the voltage across it was zeroed out in the prior mode at instant t1. As a result, IP1 follows a similar route. As a result, the current through Lr increases linearly. Right now, the point voltages are the same as they were in Mode-1, meaning that vAB = Vin and vAC = 0.5Vin. Tr2's main current, ip2, passes through Q1, Q4, Q5, and Cin1. Tr1's secondary terminal voltage is 0.5(Vo − N2Vin), while Tr2's secondary terminal voltage is 0.5VinN2. In order for the circuit to function properly in this mode, vLr must be greater than zero. As seen in Fig. 4, this causes vp2 to drop nonlinearly while ip1, ip2, iDR1, and vp1 all increase linearly. Through Q6's anti-parallel diode, the current ip2 now f lows. The current passing via switches Q1, Q4 is depicted in Fig. 3(b) as the sum of ip1 and ip2.

$$V_{Lr} = V_{in} + 0.5N_2V_{in}/N_1 - V_o/2N_1$$

(1)

$$i_{p1}(t) = \frac{V_{in}+0.5N_2V_{in}/N_1-V_o/(2N_1)}{L_r}(t - t_0)$$

(2)

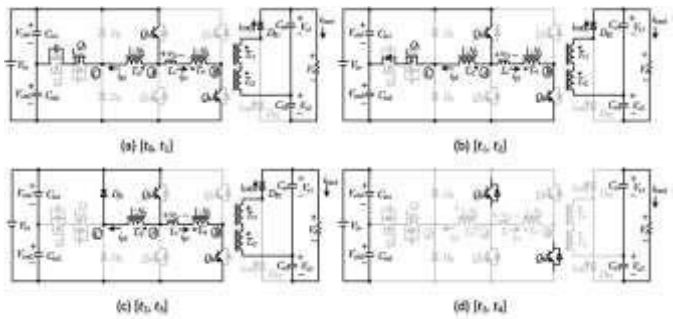


FIGURE3. Circuit paths of the four modes of operation of the proposed converter.

$$i_{p2}(t) = i_{p1}N_2/N_1$$

(3)

$$i_{DR1}(t) = i_{p1}(t)\ /N_1$$

(4)

Mode 3: This mode functions between t2 and t3. With ZCS, the switch Q5 is switched off. The current that was passing through Q6's body diode now begins to charge Q5's parasitic capacitance, resulting in a reduced and insignificant charge time. As the voltage across Q5 becomes closer to 0.5Vin, the current ip2 starts to flow via Q1 and Df1. AC=0 is the result of no current flowing through switches Q5, Q6, and

$$i_{Lr} = V_{in} - V_o/(2N_1)$$

(5)

This mode requires vLr to be less than zero in order to function properly, which results in alineardecay in the currents ip1, ip2, and iDR1, as follows:

$$i_{p1}(t) = \frac{V_{in}+\frac{N_2V_{in}-V_o}{2N_1}}{L_r}\frac{D}{T_s} + \frac{V_{in}-\frac{V_0}{2N_1}}{L_r}(t - t_1)$$

(6)

$$i_{DR1}(t) = i_{p1}(t)/N_1$$

(7)

$$i_{p2}(t) = i_{p1}(t)N_2/N_1$$

(8)

In this case, D denotes the duty ratio for switches Q5, Q6.

Ts provides the switching time period. The current flowing via switch Q4 is depicted in Fig. 3(c) as the sum of bothip1 and ip2.

Mode 4: This mode runs between t3 and t4. At the instant t3, the currents ip1, ip2, and iDR1 decline to zero due to

good design on Lr,N1,N2. ZCS is used to turn off the diodes Df1 and DR1. N1Vin−N2 <0.2V0 because the magnitude of the reflected voltage is less than the rectified voltage. In this mode, the switches Q1 and Q4 are turned on, but no current passes through them. It is supplied by ip1, ip2, iDR1, Co1, and Co2. The current path of Mode-4 is shown in Fig. 3(d). The first half of the switching cycle ends at instant t4, and the second part of the cycle begins at the same time. Since the Lt is in charge of regulating the current rise, the switches Q2, Q3, and Q6 are now turned ON with ZCS, and Q1 and Q4 are now turned OFF with ZCS. It turns on with ZVZCS since the voltage across switch Q6 is zero from Mode-3 to Mode-4. For the Q1Q4 switches, a fixed gating sequence mechanism has been utilized. But they can also be used with PWM so that the switches Q1 and Q4 can be switched off at instant t3. Since there is no current passing through these switches, the PWM-based control won't have an impact on how the suggested converter operates. The primary disadvantage of using the PWM-based control for switches Q1 and Q4 is that a current sensor is needed to overify ZCS switching in order to record the precise time instant of t3. For the first four switches, the PWM-based control is therefore not chosen. In conclusion, In order for the switches Q1 and Q4 to be turned ON and OFF using ZCS, they must tolerate Vin. For the switches Q5, Q6, to be switched ON with ZVZCS and turned OFF with ZVS, they must be able to tolerate 0.5Vin. The switching properties of the switches and diodes taken into consideration in the aforementioned analysis are shown in Table 1.

TABLE1. Voltage Stress and Switching Characteristics

	Q_1 Q_4	Q_5,Q_6	D_{f1},D_{f2}	D_{R1},D_{R2}
Turn-ON	ZCS	ZVZCS	—	—
Turn-OFF	ZCS	ZVS	ZCS	ZCS
Voltage Stress	V_{in}	$0.5V_{in}$	V_{in}	V_o

III. PARAMETER DESIGN

Table 2 contains the characteristics of the suggested converter for this experimental study.

TABLE 2. Specifications.

Input Voltage V_{in}	1.5 kV
Output Voltage V_o	15 kV
Rated Power P_N	1 MW
Switching Frequency f_s	1 kHz

A. RATIO OF TURNS

An essential design parameter for all industrial applications is the turns ratio. It is necessary that the transformer's turns ratio ought to be sized so that the auxiliary circuit supplies the remaining power and the full-bridge portion supplies the majority. To keep things simple, we will simply talk about the first half-cycle to show how the turns ratio affects how power is distributed between the two circuit components. If the suggested converter's transmission efficiency is 100%, the total power Ptot of [t0,t4] can be written as follows:

$$P_{tot} = \frac{2}{T_s}\frac{V_o}{2}\int_{t_o}^{t_3} i_{DR1}\,dt = \frac{V_o}{T_s}\int_{t_0}^{t_2} i_{DR1}\,dt \quad (9)$$

The power that the Tr1 transfers during [t0,t4] is stated as follows:

$$P_m = \frac{2}{T_s} V_{in}\int_{t_0}^{t_3} i_{p1}\,dt = \frac{2V_{in}}{T_s}\int_{t_0}^{t_2} i_{p1}\,dt \quad (10)$$

From (3) and (7), Pm also can be expressed as:

$$P_m = \frac{2V_{in}}{T_s}\int_{t_0}^{t_3} N_1 i_{DR1} dt = \frac{2N_1V_{in}}{T_s}\int_{t_0}^{t_2} i_{DR1}\,dt \quad (11)$$

Combining (9) and (11), one can obtain

$$\frac{P_m}{P_{tot}} = \frac{2N_1V_{in}}{V_0}$$

(12)

The following is an expression for the power transferred by the auxiliary circuit as a result of the law of conservation of energy:

$$P_a = P_{tot} - P_m$$

(13)

The following is the power distribution derived from (12) and (13):

$$\frac{P_m}{P_a} = \frac{P_m}{P_{tot}-P_m} = \frac{2N_1V_{in}}{V_o-2N_1V_{in}}$$

(14)

After N1 and the voltages are computed, the Pm/Pa ratio is estimated. The power ratios and their parameters are displayed in Fig. 4. One can see that the ratios of Pin/Ptot and Pa/Ptot rise and fall in tandem with an increase in N1. Thus, it is evident that the power distribution between the full-bridge and the auxiliary circuit is determined by the value of N1. Additionally, the full-bridge circuit needs a big value of N1 in order to process more power than the auxiliary circuit. According to Fig. 4, the ratios of Pin/Ptot = 90%, Pa/Ptot = 10%, and Pm/Pa = 9:1 are obtained if N1 is adjusted to 4.5. The time ratio rt of the rise time to fall time can be smaller, larger, or equal to 1 as decided since the rise time of this half-cycle is longer than the fall time from Fig 2.

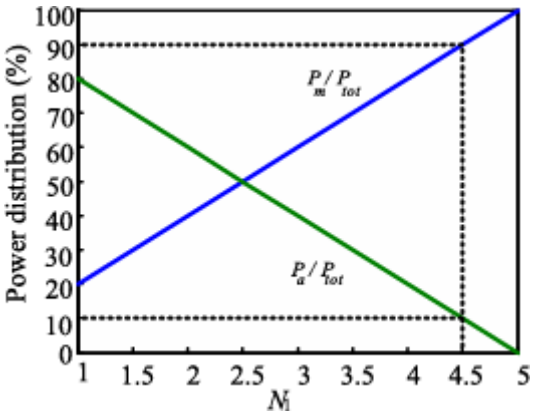


FIGURE 4. Power distribution versus N1.

from N2. The value of rt can be found using (15) and the inductor's volt-second balance law.

$$r_1 = \frac{t_1-t_0}{t_2-t_1} = \frac{V_o/2-N_1V_{in}}{N_1V_{in}+0.5N_2V_{in}-V_o/2}$$

(15)

The following can be obtained by rearranging this equation:

Since N1 is assumed to be 4.5, Fig. 5 displays the rt vs N2 curve derived from (16). As the rt decreases, it is evident that the value of N2 rises. Consequently, this illustrates how the value of N2 affects the converter's power loss.

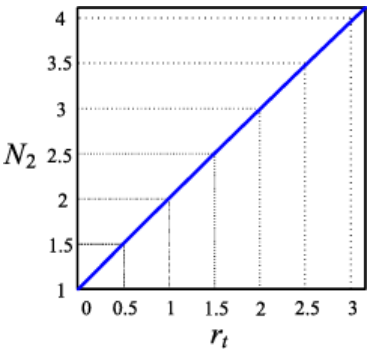


FIGURE 5. Curve of rt versus N2 when N1 = 4.5.

B. INDUCTOR "LR"

It is necessary to reduce both the low-voltage inductance and the utilization of high-voltage inductors. Ts/2 is equal to the sum of the rising and fall times. These times are stated as follows:

$$T_r = t_1 - t_0 = T_s r_1/(2 + r_1) \quad (17)$$

$$T_f = t_2 - t_1 = T_s/(2 + 2r_1) \quad (18)$$

From (2) and (17), the inductance can be written as follows:

$$L_r = T_s \frac{(N_1 V_{in} + \frac{1}{2} N_2 V_{in} - 2N_1 V_{in})}{2N_1 N_2 V_{in} I_{peak}} \quad (19)$$

The peak current of IP1 at the rated power is denoted by Ipeak. The inductor's value must be maintained below the figure determined in (19) for the converter to function properly.

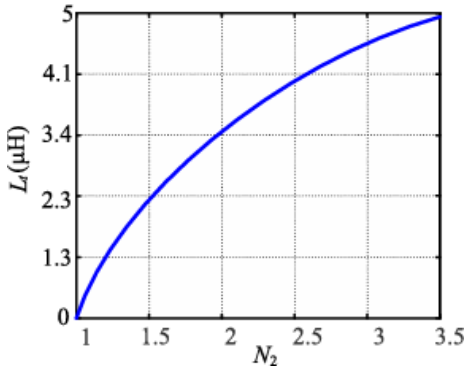


FIGURE 6. Relationship of Lt and N2 when N1 = 4.5.

Fig. 6 displays the Lr and N2 connection curve from (19). It is evident that when N2 grows, so does the inductance.

C. "CO1 & CO2" OUTPUT FILTER CAPACITORS

The output filter capacitors are used to lessen the high voltage ripples brought on by high current ripples, and the voltage-doubler rectifier design is used to lower the main transformer's turns ratio. "U" stands for the charging stage of Co1, where iCo1 = iDR1 − Iload > 0, and "D" stands for the discharging condition, where iCo1 < 0. As a result, under steady state conditions, the areas "U" and "D" are equal. One way to express the load current is as follows:

$$I_{load} = \frac{P_N}{V_o} = \frac{1}{T_s} \int_{t_0}^{t_3} i_{DR1}\, dt = \frac{1}{4} \frac{I_{peak}}{N_1} \quad (20)$$

where the ratio Ipeak/N1 provides the peak value of iDR1. The time interval for "U" is expected to be 3Ts/8 for any value of rt based on (17) and (20). Based on this estimation, the peak-to-peak voltage ripple value is as follows:

$$\Delta V_{pp} = \frac{1}{C_{o1}} \left(\frac{I_{peak}/N_1 - I_{load}}{2}\right) \frac{3T_s}{8} \quad (21)$$

When (20) and (21) are added together, the output filter capacitor values are as follows:

$$C_{01} = C_{02} = \frac{9}{64} \frac{I_{peak}}{N_1 \Delta V_{ppfs}} \quad (22)$$

D. DESIGN ILLUSTRATION

A detailed design example is given in this chapter and is presented as Case A in the Simulation Analysis section that follows. First, it is established that the output voltage Vo is 15 kV and the input voltage Vin is 1.5 kV. The converter has a rated power of 1 MW and a switching frequency (fs) of 10 kHz. The design of the temporal ratio rt is based on to (15), with 0.5 chosen. N1 is set at 4.5 based on the previous subsection and Fig. 4, and N2 is chosen using (16), which comes out to be 1.5. Based on the output voltage and rated power, the load current Iload, which is 67 A, is calculated from (20). The peak current Ipeak, which is determined to be 1.2 kA based on the load current measurement, can also be found using equation (20). Based on equation (19), the inductor Lr value is 2.315 μH. The peak-to-peak voltage ripple Vpp, or almost 1% of the output voltage, is 150 V and is used to estimate the output filter capacitors. Lastly, it is

calculated that the output capacitors Co1 and Co2 have a 25 µF value from (22).

E. ASSESSMENT OF OTHER CONVERTERS

The literature suggests several converter topologies based on twin transformers. To illustrate the superior performance and efficacy of the suggested converter, Table 3 presents a comparison between the suggested converter and the current literature.

IV. ANALYSIS OF SIMULATIONS

A simulation is carried out using PLECS software to confirm the suggested converter's working principle and estimate the impact of the turns ratio N2 on the losses and current magnitude. For the simulation analysis, three cases—A, B, and C—have been created with various parameters. Table 4 lists these important parameters that were employed in the simulation. To examine its impact on the inductor Lr and capacitors Co1 and Co2, as well as the other parameters to confirm ZVZCS, the value of the turns ratio N2 is maintained constant for each scenario. The real power Po is marginally smaller than the theoretical power PN. The primary factor influencing the power transfer between the primary full-bridge and auxiliary full-bridge circuits is the turns ratio of N1. Nonetheless, the converter's overall power losses are significantly impacted by the turns ratio N2.

Three scenarios—A (N2 = 1.5, n = 0.5), B (N2 = 1.25, n = 0.25), and C (N2 = 1.1, n = 0.1)—have been examined in order to ascertain the impact of the turns ratio N2, while maintaining a comparable turns ratio N1 = 4.5 across all cases to maintain the same power distribution for all values of N2. These examples, Tr < Tf, Tr = Tf, and Tr > Tf, respectively, depict three distinct current waveforms. The value of the inductance Lr for each of the three scenarios can be found using (19) for various N2 values. According to (20), the three examples' ip1 peak and average values are identical. Since the currents passing through both transformers' secondary windings are the same, the primary current (ip2) and the currents passing through Q5, Q6, and N2 are directly proportional to each other. Since the currents flowing through Q3, Q4, and ip1 and ip2 equal the sum of both, they likewise fluctuate in direct proportion to N2. The converter's total power Ptot is set below its rated power of 1 MW in order to guarantee that it operates in DCM. The simulated waveforms for vAB, vAC, vLr, ip1, and ip2 for the three scenarios are displayed in Fig. 7. Figure 8 displays the ip1, ip2, and current through Q1 waveforms for the three

TABLE 3. Comparison of proposed converter with similar topologies in literature.

	[24]	[19]	[32]	[33]	[28]	Proposed
Switching Frequency	5 kHz	10 kHz	15 kHz	20 kHz	10 kHz	10 kHz
No. of Switches	6	6	10	10	6	6
No. of Diodes	4	6	0	0	6	4
Rated Power	1.4 kW	1.4 kW	1.2 kW	0.3 kW	1.4 kW	3 kW
Soft-switching	ZVS & ZCS	ZVS & ZCS	ZVS	ZVS	ZVS & ZCS	ZVS & ZCS
Full-load Efficiency	97.3%	97.3%	96.5%	94%	97.2%	97%

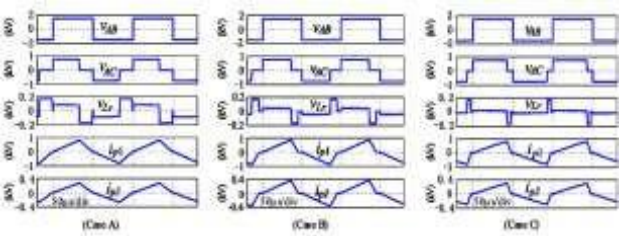


FIGURE 7. Simulation waveforms showing vAB,vAC,vLr,ip1 and ip2 for the three cases.

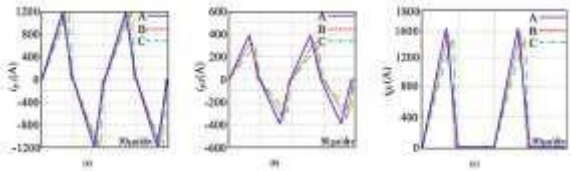


FIGURE 8. Simulation waveforms of the three cases. (a) ip1, (b) ip2, (c) Current flowing through switch Q1.

TABLE 4. Simulation parameters.

Parameters	A	B	C
Theoretical Power P_N	1 MW		
Input Voltage V_{in}	1.5 kV		
Output Voltage V_o	15 kV		
Switching Frequency f_s	1 kHz		
Time Ratio r_t	0.5	0.25	0.1
Turns Ratio N_1	4.5		
Turns Ratio N_2	1.5	1.25	1.1
Inductance L_r	$2.315\mu H$	$1.389\mu H$	$0.631\mu H$

instances. The principal current ip1 has the same average and peak values for various time ratios rt, as shown in Fig. 8(a). Consequently, For various N2, the losses in switches Q1 and Q2 are the same in all three scenarios. Fig. 8(b) shows the values of In every instance, there are notable variations in both the average and peak values of ip2. Since the circumstances are different, the conduction loss can be grouped as A>B>C. The principal current ip1 has the same average and peak values for various time ratios rt, as shown in Fig. 8(a). It may be inferred that

case C has the lowest conduction losses as the 32440 turn-off currents of Q5, Q6, and ip2 are equal. It is evident from Fig. 8(c) that The current flowing through Q3(Q4) is equal to the total of the currents flowing through Q2, Q6(Q1, Q5), with Q3(Q4) having the lowest current value. These three examples show that the average and peak current values through the switches Q3 and Q6 decrease with decreasing N2, which leads to less switching and conduction.

losses. It should be noted that the simulation analysis above used perfect transformers without taking into their defeats. For each of the three scenarios, the primary transformer processes the same power, turns ratio, average, and peak values. As a result, in all three scenarios, the primary transformer's losses are roughly equal. The same power and current values are processed by the auxiliary transformer in each of the three scenarios, but in example C, it has a substantially smaller value of primary current compared to cases A and B, indicating that case C's auxiliary transformer is the most loss-effective. In summary, the simulation results show that a modest value of N2 is necessary to achieve a high conversion efficiency and a minimal required inductance.

The following is the presentation of the full analysis:

Improved Version with Fuzzy Logic:

For high-power applications, IGBTs are integrated into a full-bridge converter structure, where a fuzzy logic controller (FLC) is employed to enhance operational efficiency. Unlike conventional control methods, FLC provides dynamic adaptability by processing imprecise inputs and adjusting the switching states in real-time. This approach ensures optimal performance under varying load conditions while maintaining a 50% fixed duty cycle. The use of FLC enhances the system's robustness, particularly in traction systems and resonant transformers, by improving response time and reducing power losses. Additionally, the auxiliary circuit in Fig. 1 supports precise control of the IGBTs, enabling efficient operation at high power levels. Where both the voltages and currents will drop to zero in DCM, it is possible to reduce the control current and switching losses by modifying the transformer turns ratios so that a smaller current passes through the auxiliary switches and a larger current passes through the main switches. A ZVZCS full-bridge converter is suggested based on the analysis above. The suggested converter is in charge of the ZVZCS function, as illustrated in Figure 1. Four primary IGBT switches (Q1–Q4), an inductor (Lr), and a transformer (Tr1) with a turns ratio of N1 make up the full-bridge circuit. Two MOSFET switches (Q5 and Q6), capacitors Cin1 and Cin2, diodes for freewheeling operations Df1 and Df2, and a transformer Tr2 with a turns ratio N2 make up the auxiliary circuit. The connection between the transformers' two secondary terminals is shown in Figure 1. This is done in order to obtain a voltage-doubler rectifier circuit input where the current stays constant. The power is distributed so that the full-bridge converter provides around 90% of the power and the auxiliary circuit provides the remaining 10%. The paragraph model effectively manages the system's performance by adjusting switching sequences and regulating power distribution, ensuring efficient energy conversion and minimal losses.

The main waveforms of the suggested converter are displayed in Fig. 2. The gating pulse substitutes for the Q1, Q4, Q2, and Q3 switches having sufficient dead time and a predetermined duty cycle of 50%. Q1/Q4 and Q2/Q3 transitions are not in phase. PWM-based control, which operates on the leading edges of Q1 and Q4, is utilized for the switches Q5 and Q6. The duty pulses of Q5 and Q6 regulate the output voltages of the suggested converter. The analyses are predicated on the following assumptions:

Every semiconductor device in use is regarded as an ideal device.

Since the values of the input capacitors Cin1 and Cin2 are maintained constant, Vcin1 = Vcin2 = Vin/2.

To help the output voltage attain a constant state where Vo1 = Vo2 = Vo/2, the filter capacitors Co1 and Co2 are maintained at the same high value.

Because of its low value, the auxiliary transformer Tr2's leakage inductance is considered insignificant.

To keep things simple, we will discuss only the proposed circuit's half-cycle. Fig. 3 displays the converter's four operating modes. At time t0, the new switching cycle begins. The switches Q1, Q4, and Q5 are turned ON, while Q2 and Q3 are turned OFF at the moment of t0. Before the start time instant t0, no current passes through any of the switches. ZCS is used to turn the switches Q1, Q4, and Q2, Q3 ON and OFF, respectively. Additionally, the voltage across Q6 is Vin/2, but the voltage across Q5 is zero, meaning it is turned ON with ZVZCS. The

paragraph model effectively manages these switching sequences and optimizes energy conversion through precise power regulation

Mode 1: This mode occurs between time instants t_0 and t_1. During this interval, the voltage vAB=Vinv_{AB} = V_{in}vAB=Vin results from the primary current ip1i_{p1}ip1 of transformer Tr1 flowing through switches Q1, Q4, inductor LrL_rLr, Tr1, and capacitor Cin1. Simultaneously, the primary current ip2i_{p2}ip2 from Tr2 flows through Q1, Q4, Q5, Tr2, the parasitic capacitance of Q6, and Cin1. The voltage across point AC, vAC=0.5Vinv_{AC} = 0.5V_{in}vAC=0.5Vin, is due to Q6 discharging from 0.5Vin to 0 at time t_0. Currents ip1i_{p1}ip1 and ip2i_{p2}ip2 share a common path through Q1 and Q4, and their combined flow is illustrated in Fig. 9(a).

Mode 2: Spanning from t_1 to t_2, this mode sees ip2i_{p2}ip2 begin to flow through Q6's body diode as the voltage across it drops to zero at the end of Mode 1. In parallel, ip1i_{p1}ip1 continues along a similar path, resulting in a linear rise in current through LrL_rLr. Voltage conditions remain unchanged from Mode 1, maintaining vAB=Vinv_{AB} = V_{in}vAB=Vin and vAC=0.5Vinv_{AC} = 0.5V_{in}vAC=0.5Vin. Tr2's primary current ip2i_{p2}ip2 flows through Q1, Q4, Q5, and Cin1. Tr1's secondary terminal voltage is 0.5(Vo−N2Vin)0.5(V_o - N_2V_{in})0.5(Vo−N2Vin), and Tr2's is 0.5VinN20.5V_{in}N_20.5VinN2. To ensure reliable mode transition, the voltage across LrL_rLr, vLrv_{L_r}vLr, must remain greater than zero. As shown in Fig. 10, this causes nonlinear behavior in vp2v_{p2}vp2, while ip1i_{p1}ip1, ip2i_{p2}ip2, iDR1i_{DR1}iDR1, and vp1v_{p1}vp1 increase linearly.

Here, a fuzzy logic controller can enhance dynamic adaptability by detecting transition points (like body diode conduction) and adjusting gate signals in real-time to reduce switching losses and ensure soft switching.

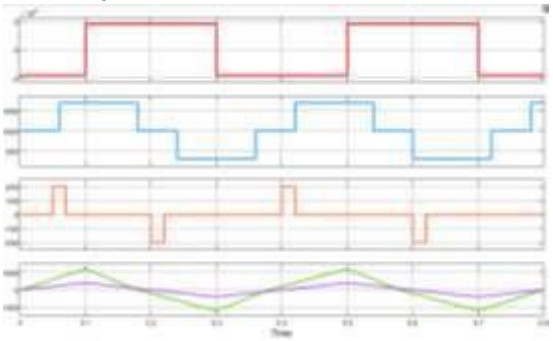
Mode 4: Operating between t_3 and t_4, this mode marks the decay of currents ip1i_{p1}ip1, ip2i_{p2}ip2, and iDR1i_{DR1}iDR1 to zero, influenced by optimal selection of LrL_rLr, N1N_1N1, and N2N_2N2. Zero-current switching (ZCS) is used to turn off diodes Df1D_{f1}Df1 and DR1D_{R1}DR1, facilitated by the condition N1Vin−N2<0.2V0N_1V_{in} - N_2 < 0.2V_0N1Vin−N2<0.2V0. During this time, switches Q1 and Q4 are ON but carry no current, with the supply maintained by energy stored in ip1i_{p1}ip1, ip2i_{p2}ip2, iDR1i_{DR1}iDR1, and capacitors Co1C_{o1}Co1 and Co2C_{o2}Co2. The second half of the switching cycle begins at t_4, where switches Q2, Q3, and Q6 are turned ON using ZCS, and Q1 and Q4 are turned OFF with ZCS. Q6, benefiting from a zero-voltage zero-current switching (ZVZCS) condition, turns ON with minimal switching stress. The current path of Mode 4 is shown in Fig. 9(d).

For Q1 and Q4, a fixed gating sequence is used, though they can alternatively be controlled using PWM. However, turning them OFF at t_3 via PWM requires precise current sensing to detect ZCS accurately, which increases complexity. Fuzzy logic control offers a smart alternative by estimating ZCS conditions based on input voltage behavior, current slopes, and timing history — eliminating the need for high-speed sensors while preserving soft-switching behavior.

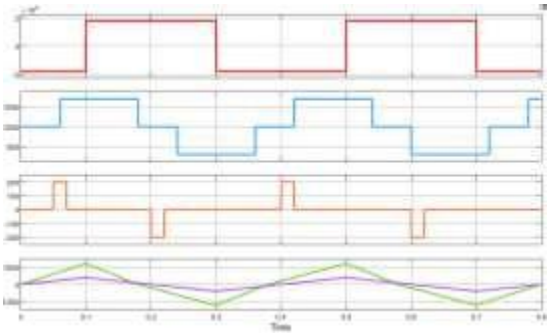
In conclusion, for effective switching:

- Q1 and Q4 must withstand VinV_{in}Vin and support ZCS-based transitions.
- Q5 and Q6 must handle 0.5Vin0.5V_{in}0.5Vin, turning ON with ZVZCS and OFF with ZVS.

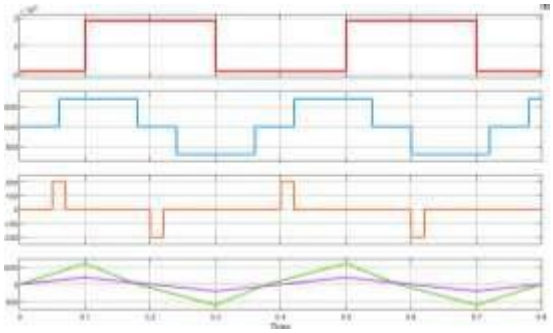
These switching characteristics, summarized in Table 1, are managed efficiently through the use of fuzzy control logic, which dynamically adapts to system conditions to optimize performance, power flow, and switching reliability.



Case1



Case2



Case 3

Figure 9: Simulation waveforms showing vAB,vAC,vLr,ip1 and ip2 for the three cases.

CONCLUSION

This paper proposes a ZVZCS full-bridge DC-DC converter that operates in DCM and is based on a dual transformer with two output capacitive filters. One main transformer, two auxiliary transformers, and four main switches make up the suggested converter. The power and current stress handled by the auxiliary switches are significantly less and smaller, respectively, than by the main switches. The power distribution between the two transformers is determined by the main transformer's turns ratio. Based on the ZCS technique, a full-bridge DC DC converter is suggested, achieving ZCS for every major switch. MOSFETs can be used for the auxiliary switches since their voltage stresses are smaller than those of the primary switches. has the ability to turn on ZVZCS. As a result, the converter's switching loss can be greatly decreased while still achieving high efficiency. Together with a thorough explanation of the suggested PWM-based full-bridge converter's working principles, the design parameters have been determined. The performance of the suggested converter is further confirmed by experimental results, and simulation results are consistent with the deduced operation principles. Over a broad load range, high experimental efficiency has been attained.

REFERENCES

[1] C. Rahmann, V. Vittal, J. Ascui, and J. Haas, ‘‘Mitigation control against partial shading effects in large-scale PV power plants,’’ IEEE Trans. Sustain. Energy, vol. 7, no. 1, pp. 173–180, Jan. 2016.

[2] S. Cui, N. Soltau, and R. W. De Doncker, ‘‘A high step-up ratio soft switching DC–DC converter for interconnection of MVDC and HVDC grids,’’ IEEE Trans. Power Electron., vol. 33, no. 4, pp. 2986–3001, Apr. 2018.

[3] C.Meyer,KeyComponentsforFutureOffshoreDCGrids.RWTHAachen: Shaker, 2007.

[4] Y.Chen,Z.Li,S.Zhao,X.Wei,andY.Kang,‘‘Designandimplementation of a modular multilevel converter with hierarchical redundancy ability for electric ship MVDC system,’’ IEEE J. Emerg. Sel. Topics Power Electron., vol. 5, no. 1, pp. 189–202, Mar. 2017.

[5] H. Athab, A. Yazdani, and B. Wu, ‘‘A transformerless DC–DC converter with large voltage ratio for MV DC grids,’’ IEEE Trans. Power Del., vol. 29, no. 4, pp. 1877–1885, Aug. 2014.

[6] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, ‘‘Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems,’’ IEEE Trans. Power Electron., vol. 28, no. 4, pp. 2014–2023, Apr. 2013.

[7] W.Qian,D.Cao,J.G.Cintron-Rivera, M.Gebben,D.Wey,andF.Z.Peng, ‘‘A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count,’’ IEEE Trans. Ind. Appl., vol. 48, no. 4, pp. 1397–1406, Jul. 2012.

[8] W. Chen, X. Ruan, and R. Zhang, ‘‘A novel zero-voltage-switching PWM full bridge converter,’’ IEEE Trans. Power Electron., vol. 23, no. 2, pp. 793–801, Mar. 2008.

[9] J. You, D. M. Vilathgamuwa, N. Ghasemi, and B. Fu, ‘‘Virtual resistor based integrated DC bus voltage conditioner for stability improvement of cascaded power converters,’’ IEEE Access, vol. 7, pp. 95959–95969, 2019.

[10] D.-D.Tran,H.-N.Vu,andW.Choi,‘‘Anovelquasi-resonantZVZCSphase shift full bridge converter with an active clamp in the secondary,’’ in Proc. IEEE8thInt. PowerElectron. Motion Control Conf. (IPEMC-ECCEAsia), May 2016, pp. 492–495.

[11] S.-T. Wu and B.-Y. Yang, ‘‘Design and implementation of an isolated bidirectional phase-shift full-bridge converter with high transformation ratio,’’

IEEE Access, vol. 11, pp. 17945–17955, 2023. [12] G.Li, J. Xia, K. Wang, Y. Deng, X. He, and Y. Wang, ‘‘Hybrid modulation of parallel-series LLC resonant converter and phase shift full-bridge converter for a dual-output DC–DC converter,’’ IEEE J. Emerg. Sel. Topics Power Electron., vol. 7, no. 2, pp. 833–842, Jun. 2019.

[13] X. Tan and X. Ruan, ‘‘Optimal design of DCM LCC resonant converter with inductive filter based on mode boundary map,’’ IEEE Trans. Power Electron., vol. 30, no. 8, pp. 4144–4155, Aug. 2015.

[14] M. Najjar, A. Moeini, M. K. Bakhshizadeh, F. Blaabjerg, and S. Farhangi, ‘‘Optimal selective harmonic mitigation technique on variable DC link cascaded H-bridge converter to meet power quality standards,’’ IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 3, pp. 1107–1116, Sep. 2016.

[15] K. Park and Z. Chen, ‘‘Analysis and design of a parallel-connected single active bridge DC–DC converter for high-power wind farm applications,’’ in Proc. 15th Eur. Conf. Power Electron. Appl. (EPE), Sep. 2013, pp. 1–10.

[16] H. A. B. Siddique, S. M. Ali, and R. W. De Doncker, ‘‘DC collector grid configurations for large photovoltaic parks,’’ in Proc. 15th Eur. Conf. Power Electron. Appl. (EPE), Sep. 2013, pp. 1–10.

[17] S. Shao, H. Chen, X. Wu, J. Zhang, and K. Sheng, ‘‘Circulating current and ZVS-on of a dual active bridge DC–DC converter: A review,’’ IEEE Access, vol. 7, pp. 50561–50572, 2019.

[18] J. Zeng, Z. Yan, J. Liu, and Z. Huang, ‘‘A high voltage-gain bidirectional DC–DCconverterwithfull-range ZVSusing decoupling control strategy,’’ IEEE J. Emerg. Sel. Topics Power Electron., vol. 8, no. 3, pp. 2775–2784, Sep. 2020.

[19] S. W. Azeem, W. Chen, I. Tariq, H. Ye, and D. Kaija, ‘‘A hybrid resonant ZVZCS three-level converter suitable for photovoltaic power DC distribution system,’’ IEEE Access, vol. 8, pp. 114981–114990, 2020.

[20] Y. Shi, L. Feng, Q. Li, and J. Kang, ‘‘High power ZVZCS phase shift full bridge DC–DC converter with high current reset ability and no extra electrical stress,’’ IEEE Trans. Ind. Electron., vol. 69, no. 12, pp. 12688–12697, Dec. 2022.

[21] D. Dujic, G. K. Steinke, M. Bellini, M. Rahimo, L. Storasta, and J. K. Steinke, ‘‘Characterization of 6.5 kV IGBTs for high-power medium frequency soft-switched applications,’’ IEEE Trans. Power Electron., vol. 29, no. 2, pp. 906–919, Feb. 2014.

[22] A. Mousavi, P. Das, and G. Moschopoulos, ‘‘A comparative study of a new ZCS DC–DC full-bridge boost converter with a ZVS active-clamp converter,’’ IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1347–1358, Mar. 2012.

[23] Z. Yin, J. Hu, H. Shu-hung Chung, and A. Ioinovici, ‘‘A ZCS PWM voltage-driven three-level converter with a secondary-side simple soft-switching snubber,’’ IEEE Trans. Ind. Electron., vol. 63, no. 12, pp. 7542–7552, Dec. 2016.

[24] S. W. Azeem, I. Tariq, K. Mehmood, M. Ehab, M. Rizwan, and M. A. Mond, ‘‘Hybrid resonant three-level ZCS converter suitable for photovoltaic power MVDC distribution network,’’ IET Renew. Power Gener., vol. 14, no. 11, pp. 1956–1963, Aug. 2020.

[25] S. W. Azeem, W. Chen, Y. Jinjie, and I. Tariq, ‘‘A hybrid resonant three level ZCSconvertersuitableformediumvoltageDCdistribution network,’’ in Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC), Mar. 2020, pp. 2968–2972.

[26] X. Ruan and Y. Yan, ‘‘Soft-switching techniques for PWM full bridge converters,’’ in Proc. IEEE 31st Annu. Power Electron. Specialists Conf. Conf., vol. 2, 2000, pp. 634–639.

[27] A. Mousavi and G. Moschopoulos, ‘‘A new ZCS-PWM full-bridge DC–DC converter with simple auxiliary circuits,’’ IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1321–1330, Mar. 2014.

[28] S. W. Azeem, K. Mehmood, K. M. Cheema, M. F. Tahir, and A. M. El-Sherbeeny, ‘‘Dual-transformer-based hybrid resonant three-level ZCS converter,’’ Energy Rep., vol. 7, pp. 421–429, Nov. 2021.

[29] J. Liu, L. Sheng, J. Shi, Z. Zhang, and X. He, ‘‘LCC resonant converter operating under discontinuous resonant current mode in high voltage, high power and high frequency applications,’’ in Proc. 24th Annu. IEEE

Appl. Power Electron. Conf. Exposit., 2009, pp. 1482–1486.

[30] C. Liu, H. Liu, G. Cai, S. Cui, H. Liu, and H. Yao, ‘‘Novel hybrid LLC resonant and DAB linear DC–DC converter: Average model and experimental verification,’’ IEEE Trans. Ind. Electron., vol. 64, no. 9, pp. 6970–6978, Sep. 2017.

[31] K. Park and Z. Chen, ‘‘A double uneven power converter-based DC–DC converter for high-power DC grid systems,’’ IEEE Trans. Ind. Electron., vol. 62, no. 12, pp. 7599–7608, Dec. 2015.

[32] V. N. S. R. Jakka, A. Shukla, and G. Demetriades, ‘‘Three-winding transformer based asymmetrical dual active bridge converter,’’ IET Power Electron., vol. 9, no. 12, pp. 2377–2386, Oct. 2016.

[33] Y. Liang, X. Liu, G. Xu, and S. Yue, ‘‘A dual-transformer-based bidirectional DC–DC converter of using blocking capacitor for wide ZVS range,’’ IEEE Access, vol. 8, pp. 170568–170578, 2020.