Accelerating High-Performance Voltage Source Inverter Prototyping with FPGA Implementation

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Abstract —

This paper highlights the advantages of FPGA-based rapid prototyping as a powerful tool for accelerating the development cycle of high-performance Voltage Source Inverters. By providing a flexible and efficient platform for algorithm testing, hardware evaluation, and performance optimization, it contributes to advancements in power electronics and facilitates the deployment of robust VSIs in diverse application domains. Through extensive experimentation, we demonstrate the effectiveness of the FPGA-based rapid prototyping platform in achieving high-performance VSI control. The FPGA's real-time capabilities facilitate swift algorithm development and testing, ensuring robustness and reliability. Moreover, the platform supports real-time hardware-level fault analysis and mitigation strategies, enhancing the overall resilience of the VSI. This paper presents an innovative approach utilizing Field-Programmable Gate Arrays (FPGAs) for rapid prototyping of high-performance VSIs. This abstract outlines the core objectives, methods, and potential contributions of a project aimed at expediting the development of high-performance Voltage Source Inverters through FPGA-based prototyping.

KEYWORDS

FPGA (Field-Programmable Gate Array), Voltage Source Inverter, High-Performance Prototyping, Power Electronics, Hardware-in-the-Loop (HIL), Rapid Prototyping, Real-Time Simulation, Control Algorithms, Digital Signal Processing (DSP),Power Conversion, Description Language (HDL),System-on-Chip (SoC),Field-Programmable Analog Array (FPAA),Power Quality, Grid Integration

Introduction

When delving into the world of high-performance voltage source inverter (VSI) prototyping, the integration of FPGA (Field-Programmable Gate Array) technology presents an exciting avenue for acceleration and innovation. This introduction aims to outline the transformative potential of FPGA implementation in expediting the development and testing phases of VSI systems.

Voltage source inverters stand as pivotal components in numerous power electronics applications, facilitating the conversion of DC power to AC power with high precision and efficiency. However, the intricacies of designing and refining

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these systems pose significant challenges, often requiring extensive time and resources for prototyping and validation.

FPGAs, known for their flexibility, reconfigurability, and parallel processing capabilities, offer a promising solution to expedite VSI prototyping. By leveraging FPGA-based platforms, engineers can swiftly model, simulate, and validate complex VSI algorithms and control strategies in a hardware-in-the-loop (HIL) environment. This approach not only accelerates the development cycle but also allows for rapid iterations and optimizations. This introduction will delve into the advantages of FPGA implementation in VSI prototyping, exploring how it streamlines algorithm development, enhances real-time performance, and facilitates seamless integration with other power electronic components. Additionally, it will highlight case studies and methodologies that demonstrate the efficiency gains and performance enhancements achievable through FPGA-based VSI prototyping.

Overall, this exploration aims to underscore the transformative impact of FPGA technology in expediting high-performance VSI prototyping, ultimately driving innovation and advancements in power electronics engineering.

METHODOLOGY

The workflow of the proposed FPGA design methodology for rapid prototyping digitally controlled power electronics system is shown in Fig. 1. The design methodology emphasizes the con- current design of the power stage and digital controller, which enables high-level system performance and optimum resource utilization. The power stage's basic specifications include topology, power device performance, passive component values, and sensor performance. These hardware specifications could also affect the digital control system's design, such as the controller structure, controller parameters, and control iteration speed. Using software like PLECS and Simulink, the power stage can be accurately represented by the circuit diagram. Simultaneously, the function blocks like C-Script and S-Function could simulate the C code-based digital controller's behavior. This way, the pre- liminary system specifications can be established. After the preliminary round of design iteration, we should have a functional prototype C code for the digital controller. The next question is whether to implement the control algorithm in PS or PL cores.

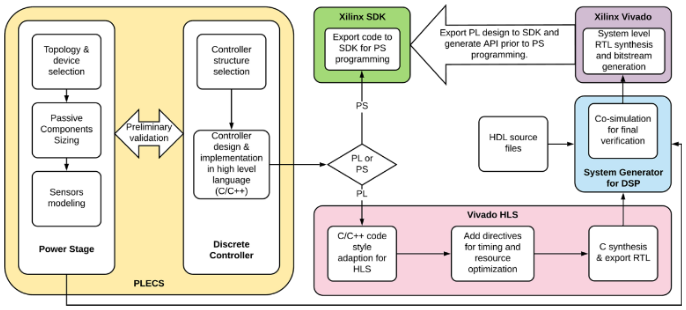

Topology & device selection
Passive Components Sizing
Sensors modeling
Power Stage
Preliminary validation
Controller structure selection
Controller design & implementation in high level language (C/C++)
Discrete Controller
PLECS
Xilinx SDK
Export code to SDK for PS programming
Export PL design to SDK and generate API prior to PS programming.
Xilinx Vivado
System level RTL synthesis and bitstream generation
PS
PL or PS
PL
HDL source files
Co-simulation for final verification
System Generator for DSP
Vivado HLS
C/C++ code style adaption for HLS
Add directives for timing and resource optimization
C synthesis & export RTL

Fig. 1. Workflow of proposed FPGA design methodology for rapid prototyping in power electronics.

This involves the controller's structure, parameters, and control speed. We use software like PLECS and Simulink to represent the power stage and simulate the digital controller's behavior using function blocks like C-Script and S-Function, which are based on C code. After an initial round of design iterations, we obtain a functional prototype C code for the digital controller. We then face the choice of implementing the control algorithm in either the PS or PL cores of the FPGA.

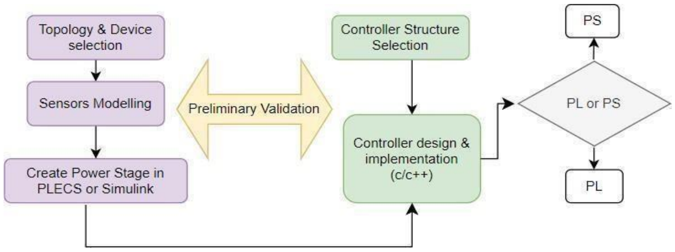
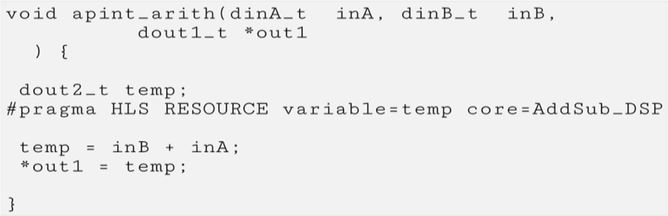

Topology & Device selection
Sensors Modelling
Create Power Stage in PLECS or Simulink
Preliminary Validation
Controller Structure Selection
Controller design & implementation (c/c++)
PS
PL or PS
PL

FIG 2. DESIGN METHODOLOGY

With the help of tools like HLS, those optimization techniques can be easily applied using corresponding directives. Whereas using the conventional FPGA design method, the exploration of the design space might not be sufficiently rigorous. However, if the algorithm is to be implemented in PL, HLS would be a goodchoice. The Xilinx HLS tool synthesizes a C function into an IP block to integrate into a hardware system. It is tightly integrated with the rest of the Xilinx design tools and provides comprehensive language support, and features for creating the optimal implementation for a C algorithm.



```
void apint_arith(dinA_t  inA, dinB_t  inB,
          dout1_t *out1
  ) {

 dout2_t temp;
#pragma HLS RESOURCE variable=temp core=AddSub_DSP

 temp = inB + inA;
 *out1 = temp;

}
```

FIG. 3. EXAMPLE CODE SNIPPET WITH HLS PRAGMA FOR RESOURCE UTILIZATION OPTIMIZATION.

The PS CPU is versatile and easy to program using high-level languages. However, the PS's sequential nature means the absolute performance (algorithm execution time) for a specific task is no match to the PL. Although there are HLS tools to simplify FPGA's design process, it is still more complicated than the PS design.

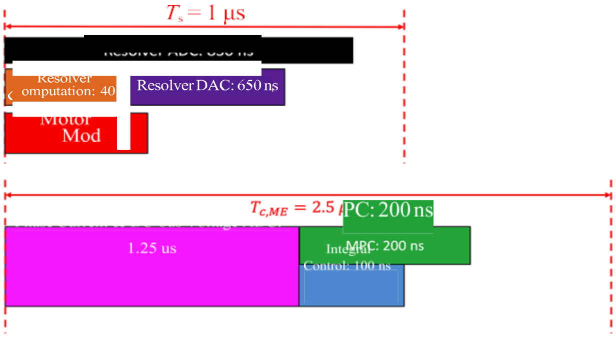


FIG. 4. TASK PARALLELISM AND LATENCY ANALYSIS FOR ME.

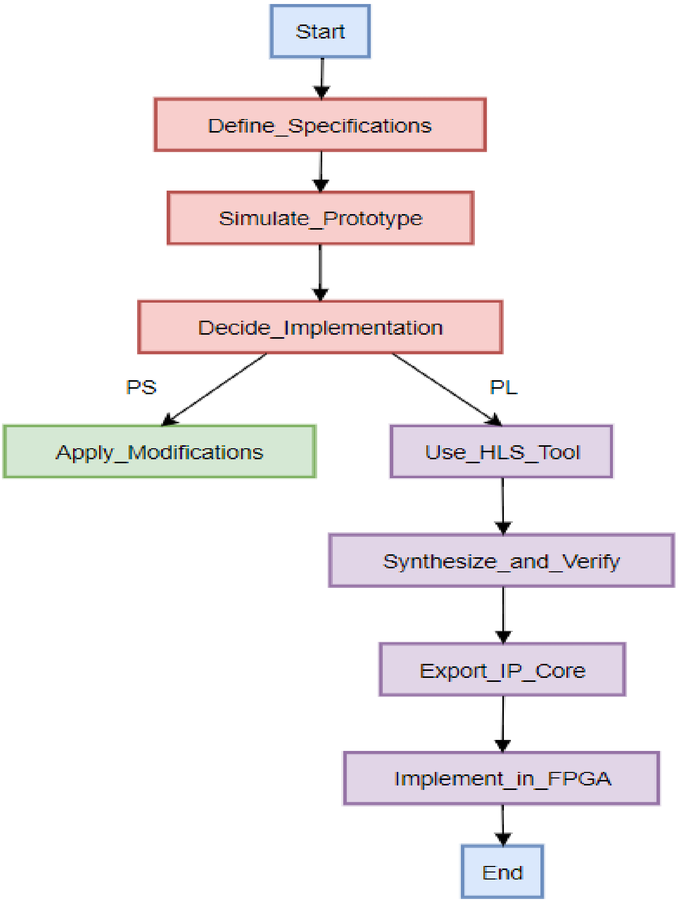
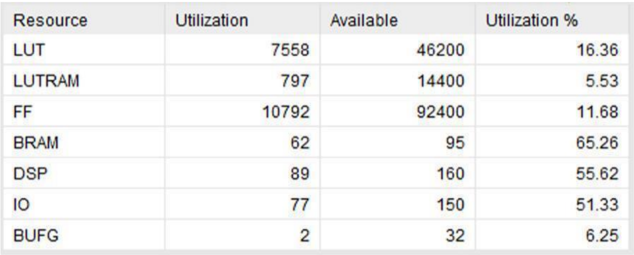


FIG 5. FPGA DESIGN METHODOLOGY

When the conversion is finished, then the MPC and integral (I) controller update are initiated. For the sequential logic blocks, the PWM generation block consists of several counters and logic gates, designed using library blocks from the System Generator for DSP toolbox in Simulink. However, the ADC interface requires careful design. There are five physical quantities in the ME application that need to be sampled at 400 kHz rate

For PL computation core design, the workflow in Fig. 1 is followed. One critical decision to make is whether to use floating-point or fixed-point arithmetic. The main advantage of floating-point data type is the ease of implementation, and the PL of ZYNQ-7000 SoC also supports floating-point data types. However, since both the real-time motor model and MPC require lots of computation and low latency, the full floating-point implementation would exceed the limit of on-chip resources and timing requirement.



Resource	Utilization	Available	Utilization %
LUT	7558	46200	16.36
LUTRAM	797	14400	5.53
FF	10792	92400	11.68
BRAM	62	95	65.26
DSP	89	160	55.62
IO	77	150	51.33
BUFG	2	32	6.25

TABLE 1. ZYNQ-7000 RESOURCE UTILIZATION REPORT FOR ME

Regarding resource utilization, the excerpt details the distribution across different FPGA components. It mentions that I/O pins and DSP (Digital Signal Processing) cores are extensively utilized, likely due to interfacing requirements with peripheral circuits such as ADCs (Analog-to-Digital Converters) and DACs (Digital-to-Analog Converters). These are crucial for sensing, resolver emulation, and executing computationally intense tasks like model predictive control and motor modeling.

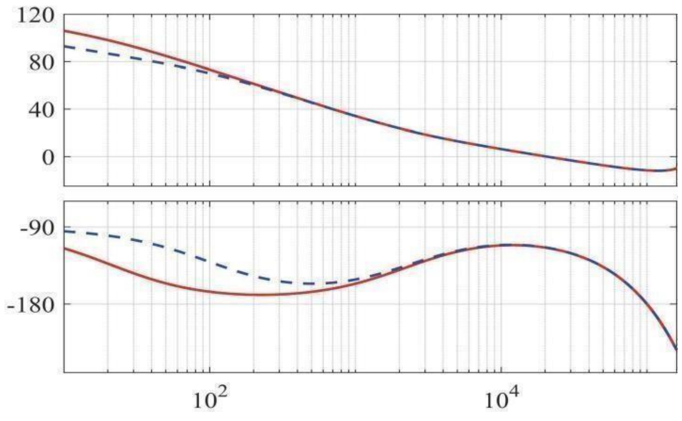


CHART 1 COMPENSATEDOPENLOOP RESPONSE.

RESULTS AND DISCUSSIONS

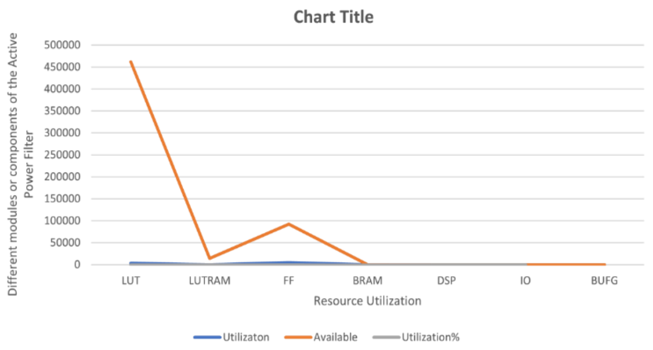


Chart-2 Resource Utilization report for APF

The examination of resource utilization in the implemented system reveals a distinctive pattern, with the FPGA bearing a predominantly light load. This characteristic arises from a strategic distribution of computational tasks, with the Processing System (PS), housing the ARM Cortex-A9 processor, taking on a significant portion of the workload. The FPGA's role in parallel processing is optimized, focusing on tasks where its capabilities are most beneficial. This cooperative arrangement ensures an efficient system where computational demands are met through a harmonious interplay between the PS and FPGA, showcasing the versatility of the architecture. Additionally, the interaction with external ADC ICs, integral for analog-to- digital conversion, underscores the system's sophistication. The extensive use of I/O pins reflects the system's adaptability to handle complex external interfaces, emphasizing its capability to manage intricate communication requirements effectively. Steady-state operation signifies the condition where the system has stabilized and is functioning without any transient changes. This waveform captures the behavior of the APF once it has settled into a consistent and regular mode of operation, usually after any initial transient effects have subsided.

The waveform displayed in Fig. 1might exhibit details such as voltage or current harmonics, phase relationships, or the effectiveness of the APF in mitigating power quality issues like harmonics, reactive power compensation, or voltage regulation. It could highlight the APF's ability to maintain stability, reduce distortion, or regulate specific electrical parameters within acceptable limits.

Understanding the characteristics presented in this waveform aids in assessing the APF's performance under normal operating conditions, verifying its efficacy in addressing power quality concerns, and validating its suitability for its intended application within electrical systems.

CONCLUSION

The presented paper clearly dealt the lot of designing methods for SRAM design for low power applications. The paper contains both CMOS and CNFET technology-based practical implementations. As a result of this implementation, the CMOS technology does not perform properly when considering the 32 nm channel length. At 32 nm channel length, it produced undesired effects like short channel effect and mobility degradation, etc., This limitation is overcome by CNFET-based SRAM cell design approaches. Hence, the paper proves that CNFET-based Multi-Threshold SRAM design performs better than traditional SRAM cells in CMOS techniques. The proposed design will be further developed by infusing the power reduction techniques.

In many electronic devices and microprocessors, the SRAM (Static Random Access Memory) is commonly used for caches. The SRAM produced better performance compared with the Dynamic Random Access Memory (DRAM). The DRAM capacity is much greater than the static type and it needs more time to refresh itself. This time delay causes the increment of the latency to access the data. In recent electronic devices that are assigned for particular applications such as multimedia, object tracking, video processing, and medicine, the computation process and complexity have been increased and it is also reflected in the power consumption. These devices have unique processors that consumed huge SRAM sub-modules. Hence, the SRAM is one of the much delegated memory modules for power considerations. The limitation of the SRAM power consumption is performed by decreasing Vdd supply voltage or Vth threshold voltage.

The high-low threshold transistor pairs are used to change the channel length by modifying the oxide thickness of the transistors. The overall implementation of the Multi-threshold-based SRAM cells are implemented with the help of CNFET. Carbon Nanotube Field-Effect Transistors (CNFETs) in Static Random Access Memory (SRAM) have shown promising potential due to their ability to offer

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