Adaptive Frequency Synthesizer for 5G SDR

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Abstract—Traditional frequency synthesizer techniques for scalable Software Defined Radio (SDR) systems often struggle with the high demands of modern applications due to their complex computations and sensitivity to path interference, leading to degraded performance in real-time environments. To address these challenges, designing an efficient and robust frequency synthesizer framework within the SDR system is crucial, particularly for 5G wireless communication systems that require enhanced Quality of Service (QoS). This research introduces a hardware-optimized, reconfigurable digital baseband processing and frequency synthesizer model that incorporates error correction and compensation mechanisms within a Direct Digital Frequency Synthesizer (DDFS). By integrating these mechanisms, the proposed model reduces design complexity while improving tolerance to phase noise, quantization errors, and other nonlinearities, ensuring reliable performance across a wide range of frequency bands. Experimental results and comparative analyses validate the enhanced performance metrics, and exhaustive test bench simulations confirm the functionality and robustness of the system.
Index Terms—SDR system, Frequency synthesizer, DDFS, Error correction, Phase noise compensation.

I. INTRODUCTION

In modern communication systems like SDR and 5G, the demand for high-performance frequency synthesizers has grown. Traditionally, analog-based PLLs have been used, but they face challenges in scalability and integration with digital systems. DDFS offers a more flexible, digital solution, though issues like phase noise and quantization errors impact signal quality in high-demand applications such as 5G.

This research enhances DDFS by integrating error correction and compensation mechanisms to reduce these issues, maintaining hardware efficiency for SDR systems. The proposed DDFS model is reconfigurable, optimized for wide frequency bands, and supports multiple standards. Validations through simulations show its potential in addressing modern communication needs.

SDR systems require optimized frequency synthesizers to minimize hardware cost and energy consumption. A QDDFSbased SDR transceiver system can accelerate digital operations while accommodating various wireless standards through indirect, analog, or digital design approaches. High-

performance synthesizers must balance wide frequency tuning, reduced phase noise, and minimized spurs.

Hardware platforms like DSPs and FPGAs support SDR implementations, with FPGAs offering dynamic reconfiguration and high throughput, making them more suitable for scalable SDR systems. Recent advancements in FPGA and GPU technologies further enhance SDR performance and flexibility in meeting modern communication demands.

A. DIRECT DIGITAL FREQUENCY SYNTHESISER (DDFS)

A Direct Digital Frequency Synthesizer (DDFS) is a sophisticated electronic system designed to generate precise frequencies through purely digital means. Unlike traditional analog frequency synthesizers, which rely on analog components such as Phase-Locked Loops (PLLs) and voltage- controlled oscillators (VCOs), a DDFS utilizes digital logic and memory to produce a stable and accurate frequency output. The core of a DDFS is its phase accumulator, which incrementally adds a phase increment value on each clock cycle to generate a phase value. This phase value is then mapped to a sine or cosine wave lookup table (LUT) to produce the desired frequency signal. The main advantages of DDFS include high frequency resolution, improved frequency accuracy, and the ability to rapidly switch between different frequencies. Additionally, DDFS can be implemented using digital hardware such as Field-

Programmable Gate Arrays (FPGAs) or Digital Signal Processors (DSPs), providing significant flexibility and scalability. Recent advancements in FPGA technology have further enhanced the performance of DDFS systems, making them suitable for a wide range of applications, including communication systems and signal processing tasks. Despite its benefits, DDFS systems must address challenges such as phase noise, quantization errors, and hardware resource utilization, necessitating ongoing improvements in error correction and compensation techniques to ensure optimal performance. Frequency synthesizer proposed in Van Driessche et al (2006) enables the quadrature LO-signals for generating an extremely wide range of frequencies which is ranging from 174 MHz to 5.825 GHz. The tuning range is precisely increased using programmable dividers and a reconfigurable delay locked loop (DLL). In [12] developed PLL with high-speed dividers for designing frequency synthesizer to generate inphase/quadrature phase signal with frequency bands of 0.6-4.6 GHz, 5-7 GHz, 10-14 GHz, and in-phase signal over 20-28 GHz for softwaredefined radio applications [13]. In [14] proposed monolithic software-defined radio design for 2 × 2 MIMO system which includes dedicated wide-band frequency synthesizers for both uplink and downlink paths to enable Frequency Division Duplex (FDD) radios. Here Direct Digital Synthesis (DDS) based integer-N PLL is used in frequency synthesizer with 3-tank VCOs, loop-filter. Due to the inclusion of zero-spur phase detector low-spur and high resolution is achieved [15]. In [16] developed fully integrated frequency synthesizer using dual-band quadrature output voltage- controlled oscillator for generating frequencies ranges from 47 MHz to 6 GHz and tuneable transformer-based narrow-band load. This synthesizer can support Multi Band-OFDM and UWB bands with optimal settling time and accommodate wireless standards ranges from 47 MHz to 10 GHz. Ga and Fathima (2015) proposed highly optimized Quadrature Direct Digital Frequency Synthesizer (QDDFS) for SDR wireless applications such as Orthogonal Frequency Division Multiplexing (OFDM) system [17]. This Quadrature based approach rapidly hopping between the various ranges of frequencies with its functionality which helps improved response time. Moreover the sine and cosine values are generated in digital domain to produce appropriate phase and frequency resolution with least complexity overhead [18]. In

[19] developed transient PLL with switched capacitors to cover a frequency range of several GHz (¿10GHz) for implementing SDR in avionic communication applications. The single mixer based PLL core reduces the settling time into 3.92 s with suppressed total phase noise. In [20] proposed narrow band PLL which can generates wideband outputs by mixing and dividing. The quadrature single side-band (QSSB) mixer operates in constant loop parameters and passive negative resistance (PNR) during frequency mixing for a superior image side-band rejection ratio (ISRR). In [21] developed dual-mode VCO with highly optimized automatic frequency calibration (AFC) to implement PLL component. This method also includes multi- phase counter (MPC) accelerates supports configurable band selection which increase the calibration accuracy well as an energy consumption. In [22] introduced fractionalN frequency synthesizer for improved system performance which includes level-shift-less phase frequency detector and a chopping differential charge pump components. Experimental results proves reduction in quantization noise and in-band and out- band phase noises also reduced by 3dB and 6dB with root mean square jitter value of 210fs. In [23] proposed energy efficient ADPLL loop for hybridloop receiver (RX) to accomplish interference tolerant Bluetooth communication. This digitalized frequency synthesizer in hybrid-loop structure improves the interference tolerance and allows to digitize frequency- modulated signal without an ADC component. In [24]developed discrete time event-driven compound ADPLL to interconnect as a Cartesian grid like system-on-chip components. The oscillator completely integrated using 65-nm CMOS processing to carry out phase and frequency synchronization over small-scale multiple input multiple- output systems (MIMO). Digital implementation of ADPLLs and most of its functional blocks are easily configured on Field Programmable Gate Arrays to incorporate parallel computation and reconfigurability measures. In [25] utilized binary search algorithm to regulate the locking range of ADPLL over any arbitrary frequency generated during frequency synthesis. Here Coordinate Rotational Digital Computer (CORDIC) is used for phase to amplitude conversion to reduce the hardware complexity overhead and overcome the limitation of exiting Look Up Table (LUT) based implementation. In [26] introduced quadrature oscillator model which comprises of four low-Q series LC tanks in a ring structure. It reduces distortion levels of delta-sigma architecture and performance rate significantly increased. In [27] increased feasibility and other performance metrics of the ADPLL using digitally controlled ring-oscillator (ring-DCO) design for system-level integration. Both the frequency resolution and the tuning ranges are significantly increased. In [28] developed FPGA based an event-driven all-digital phase locked loop (ADPLL) for asynchronous control. The simulations are carried out using exhaustive test bench to verify individual components of ADPLL networks and statistically comparison with other models in terms of transient response, phase noise and the performance rate.

II. LITRATURE SURVEY

[1] Kumar, B. P., Paidimarry, C. S. (2020). Improved real- time GPS RF data capturing for GNSS SDR applications. Gyroscopy and Navigation, 11(1), 59-67. Summary: This paper discusses advancements in real-time GPS RF data capturing systems for Global Navigation Satellite Systems (GNSS) within SDR frameworks. It emphasizes improvements in capturing and processing GPS signals to enhance the accuracy and efficiency of GNSS SDR applications. The focus is on optimizing the data acquisition process to achieve better performance in real-time scenarios.

[2] Petrov, A. A., Davydov, V. V., Grebennikova, N. M. (2018). On the potential application of direct digital synthesis in the development of frequency synthesizers for quantum frequency standards. Journal of Communications Technology and Electronics, 63(11), 1281-1285. Summary: This paper explores the use of Direct Digital Synthesis (DDS) in creating frequency synthesizers for quantum frequency standards. The authors highlight the potential benefits of DDS technology in achieving precise frequency generation and its relevance to high-precision applications like quantum standards. The study provides insights into the design considerations and performance improvements enabled by DDS.

[3] Mortezapour, Siamak, and Edward KF Lee. (1999). Design of low-power ROM-less direct digital frequency

synthesizer using nonlinear digital-to-analog converter. IEEE Journal of Solid-State Circuits, 34(10), 1350-1359. Summary: This paper presents a design for a low-power Direct Digital Frequency Synthesizer (DDFS) that eliminates the need for a read-only memory (ROM) by using a nonlinear digital- toanalog converter. The approach aims to reduce power consumption while maintaining performance, making it suitable for low-power SDR applications. The design is evaluated for its effectiveness in achieving low-power operation and high frequency accuracy.

[4] Haas, Sebastian, et al. (2017). A heterogeneous SDR MPSoC in 28 nm CMOS for low-latency wireless applications. Proceedings of the 54th Annual Design Automation Conference 2017. Summary: This paper discusses a heterogeneous SDR Multiprocessor System-on-Chip (MPSoC) designed using 28 nm CMOS technology. The focus is on achieving low-latency performance for wireless applications. The study details the architectural design and integration of various processing units to support efficient SDR operation and meet the demands of low-latency communication systems.

[5] Hatami, Safar, et al. (2013). Single-bit pseudoparallel processing low-oversampling delta–sigma modulator suitable for SDR wireless transmitters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(4), 922-931. Summary: This paper introduces a single-bit pseudoparallel processing delta–sigma modulator designed for low- oversampling applications in SDR wireless transmitters. The modulator is evaluated for its suitability in high-performance SDR systems, focusing on its ability to handle oversampling requirements and improve signal quality in wireless communication.

[6] Inguva, S. C., Seventiline, J. B. (2019). LH-CORDIC: Low power FPGA based implementation of CORDIC architecture. International Journal of Intelligent Engineering and Systems, 12(2), 305-314. Summary: This paper presents the LHCORDIC architecture, a low-power FPGA-based implementation of the Coordinate Rotation Digital Computer (CORDIC) algorithm. The design aims to reduce power consumption while maintaining the performance of the CORDIC algorithm in FPGA implementations. The study discusses the benefits of this approach for applications requiring efficient digital signal processing.

[7] Yan, B., Pan, C., Beck, T., Jin, X., Wang, L., Liang, D., ... Hao, W. (2022). New Reprocessing towards LifeTime Quality-Consistent Suomi NPP OMPS Nadir Sensor Data Records (SDR): Calibration Improvements and Impact Assessments on Long-Term Quality Stability of OMPS SDR Data Sets. Remote Sensing, 14(13), 3125. Summary: This paper addresses improvements in the calibration of Suomi National Polar-orbiting Partnership (NPP) OMPS Nadir Sensor Data Records (SDR). The focus is on reprocessing techniques to ensure consistent quality and stability of long-term data records. The study highlights the impact of these calibration improvements on the accuracy and reliability of sensor data used in remote sensing applications.

[8] Garcia, E. O., et al. (2006). Pipelined CORDIC design on FPGA for a digital sine and cosine waves generator. In 2006 3rd International Conference on Electrical and Electronics Engineering, pp. 1-4. IEEE. Summary: This paper describes a pipelined CORDIC design implemented on an FPGA for generating digital sine and cosine waves. The design aims to improve the efficiency and performance of sine and cosine wave generation by leveraging FPGA technology. The study includes performance metrics and discusses the benefits of pipelining in achieving high-speed operations in digital signal processing.

III. EXISTING WORK

Digital Clock Synthesizers are crucial components in Software-Defined Radio (SDR) systems, where they play a vital role in generating and tuning local oscillators (LO) for optimal signal processing. The design and implementation of frequency synthesizers (FS) are fundamental to ensuring that SDR systems can meet performance requirements, including accurate frequency generation and minimal phase noise. A generic digital frequency synthesizer, as illustrated in Figure 1, takes an input frequency and generates a range of output frequencies with high precision. This process involves using various digital techniques to achieve the desired frequency accuracy and stability. Despite its utility, meeting the performance demands for local oscillators (LOs) is challenging. The accuracy and phase noise characteristics of these oscillators can be difficult to control, particularly over wide frequency ranges. The inherent instability in phase noise and the difficulty in achieving precise frequency tuning are common issues faced in the design of digital frequency synthesizers. Figure 2 depicts a typical digital clock synthesizer architecture for SDR systems. In most digital synthesizers, the PhaseLocked Loop (PLL) is employed as a fundamental component. The PLL includes a Voltage-Controlled Oscillator (VCO) and associated signal mixers to generate various frequency bands within its tuning range. The VCO's role is to produce a frequency signal that is adjustable based on control voltage. The signal mixer, typically a Single-Sideband (SSB) mixer, is used to mix the output of the VCO with a reference signal to achieve the desired output frequency. frequency synthesizers, each with its advantages and drawbacks. Analog VCOs are known for their continuous frequency tuning and generally better phase noise performance. However, they may suffer from limitations in frequency range and tuning granularity. Dual VCOs offer extended frequency ranges and improved flexibility but can introduce additional complexity and power consumption. In practical applications, PLL-based frequency synthesizers often use a single SSB mixer and a single VCO. This configuration simplifies the design and reduces

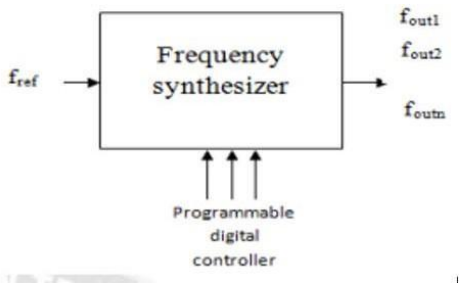

Fig. 1. Digital frequency synthesizers

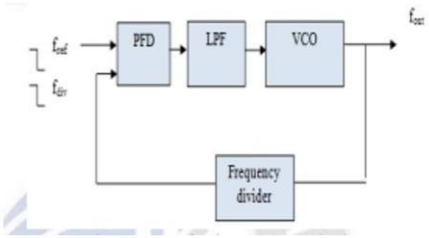

Fig. 2. PLL for frequency synthesizer

the system's complexity but may lead to performance tradeoffs. These trade-offs include reduced energy efficiency and limitations in the frequency tuning range. The challenge is to balance these factors to meet the specific requirements of real- time applications, ensuring that the synthesizer provides accurate and stable frequency outputs while minimizing energy consumption and system complexity. Overall, the choice of architecture and components in a frequency synthesizer is driven by the need to optimize performance metrics such as frequency accuracy, phase noise, and energy efficiency. As SDR technology advances, ongoing improvements in digital synthesizer designs and component technologies will continue to address these challenges and enhance the capabilities of SDR systems. In Software-Defined Radio (SDR) systems, frequency synthesizers are critical components responsible for generating a broad range of frequencies based on a given input reference frequency. They play a key role in ensuring the stability,

accuracy, and spectral performance of the overall system. Various types of Phase-Locked Loops (PLLs) are employed to meet the diverse needs of frequency synthesis in SDR applications. These include Generic PLL (GPLL), Digital PLL (DPLL), and All-Digital PLL (ADPLL). Each type offers different advantages and is suited for specific applications based on its design and performance characteristics. Generic PLLs are traditionally based on analog techniques. They use analog components to achieve frequency synthesis by locking a feedback loop to a reference signal. While GPLLs can offer good performance in terms of phase noise and frequency stability, they are often limited by their sensitivity to component variations and external noise. Additionally, GPLLs can be complex to design and integrate, particularly when aiming for wide frequency tuning ranges. Digital PLL (DPLL): Digital PLLs combine both analog and digital components to enhance robustness and performance. The analog portion typically includes a Voltage-Controlled Oscillator (VCO) and a loop filter, while the digital part includes phase detection and frequency control units. DPLLs improve upon GPLLs by integrating digital signal processing techniques, which offer better precision and flexibility. This hybrid approach allows for more precise control and reduces susceptibility to analog component variations. All-Digital PLL (ADPLL): All-Digital PLLs represent a significant advancement over traditional PLL models. ADPLLs exclusively use digital components, ADPLLs provide enhanced flexibility in generating a wide range of system clocks and signals, making them particularly suitable for SDR systems that require dynamic frequency adjustments. Reduced Sensitivity: Digital components are less sensitive to process variations compared to analog components, leading to improved stability and reliability. ADPLLs can offer better performance in terms of phase noise and jitter due to their digital nature and the ability to perform precise mathematical operations. PLLs, in general, are used to produce output signals with frequencies that are dynamically adjustable by programmable units, often set as multiples of an input frequency. They help maintain phase and frequency locking conditions, which is essential for stable signal generation. PLLs can exhibit frequency discrimination effects due to their loop filter, which impacts their ability to track signals over a broad frequency range. This can lead to narrowband tracking characteristics that may affect performance in applications requiring wide bandwidth. The linearity of the Voltage- Controlled Oscillator (VCO) in a PLL affects the overall linearity of the design. Nonlinearities in the VCO can introduce distortions and degrade signal quality. PLLs may face constraints related to modulation frequency range. Analog components in traditional PLLs are sensitive to low-frequency regions, which can affect the stability and performance of the synthesizer. Overall, while PLLs are fundamental to frequency synthesis in SDR systems, the choice between GPLL, DPLL, and ADPLL depends on the specific requirements of the application. ADPLLs, with their all-digital design, offer significant advantages in terms of flexibility, stability, and performance, making them a popular choice for modern SDR systems. As discussed in the previous section, among the three primary methodologies for designing frequency synthesizer (FS) units—Indirect, Analog, and Digital—Direct Digital Synthesizers (DDS) offer notable advantages over indirect synthesizers such as Phase-Locked Loops (PLLs). DDS is particularly advantageous for generating precise frequencies in Software-Defined Radio (SDR) systems and wireless applications due to its ability to produce accurate and stable frequencies with minimal step sizes. Unlike indirect synthesizers that rely on analog components and complex feedback mechanisms, DDS employs digital components throughout the synthesis process. This direct approach allows DDS to achieve fine frequency resolution and precision. The key benefits of DDS over indirect synthesizers include its precision and accuracy, with the quality of the output directly

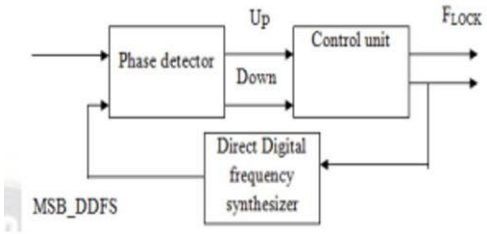

Fig. 3. Block of digital frequency synthesizer system

related to the input signal. This ensures that the synthesized frequencies closely match the desired specifications. Furthermore, the digital implementation of DDS simplifies the design and reduces susceptibility to component variations, enhancing overall system reliability. Among the various DDS models, the All-Digital Phase-Locked Loop (ADPLL) stands out as a widely used choice due to its effectiveness in improving lock-in time and performance. ADPLLs are favored in DDS applications because they eliminate analog components, which enhances scalability and portability while mitigating issues related to analog non-linearities and variations. Additionally, ADPLLs are

designed to achieve faster lock-in times compared to traditional PLLs, which is beneficial for systems requiring rapid frequency adjustments and precise synchronization. The all-digital nature of ADPLLs also allows for easy scalability and integration into various SDR systems, making them suitable for a wide range of applications.

IV. PROPOSED WORK

To ensure enhanced system reliability and performance, the proposed model incorporates a comprehensive suite of error correction and compensation mechanisms. Advanced error correction techniques are employed, including sophisticated codes such as Reed-Solomon and Turbo codes, which are designed to detect and correct errors in the transmitted data. Reed-Solomon codes are particularly effective in correcting burst errors, while Turbo codes offer high performance through iterative decoding, making them suitable for applications requiring robust error resilience. These codes improve data integrity by addressing errors that may occur due to noise or other distortions during transmission. In addition to error correction, the model integrates compensation mechanisms to tackle phase noise and quantization errors. Phase noise, which can degrade signal quality, is mitigated through techniques that stabilize the frequency reference and reduce phase jitter. Quantization errors, which arise from approximating continuous signals with discrete values, are addressed by employing advanced algorithms that minimize the impact of these errors on the signal quality. Together, these mechanisms not only enhance the system's tolerance to common issues but also improve overall performance and reliability across a wide range of operating conditions. This multifaceted approach ensures that the system remains robust and efficient, even in challenging real-time environments.

The proposed system presents a reconfigurable, hardwareoptimized digital baseband processing and frequency synthesizer model specifically engineered to address the shortcomings of traditional frequency synthesizers within Software Defined Radio (SDR) systems, with a focus on 5G wireless communication applications. Traditional synthesizer techniques often encounter challenges due to their intricate computations and susceptibility to path interference, which can significantly impair performance in real-time scenarios. To tackle these issues, the proposed model incorporates a Direct Digital Frequency Synthesizer (DDFS) coupled with sophisticated error correction and compensation mechanisms. This integration aims to enhance the system's performance by improving its resilience to phase noise, quantization errors, and other non-linearities, ultimately ensuring reliable operation across diverse frequency bands and reducing the design complexity inherent in traditional approaches.The system architecture includes a digital baseband processing unit that leverages processing elements such as DSP cores, FPGAs, or ASICs. It incorporates sophisticated signal processing algorithms for modulation, demodulation, filtering, and error correction, ensuring adaptability to various communication protocols and standards. The frequency synthesizer, based on the DDFS, is designed with a high level of precision, featuring detailed specifications for frequency resolution, output frequency range, phase noise performance, and quantization error management. To enhance system reliability, the proposed model integrates robust error correction techniques, including advanced error detection and correction codes like Reed- Solomon or Turbo codes. Additionally, compensation mechanisms are employed to mitigate phase noise and quantization errors, thus improving the overall system tolerance to these common issues. Implementation details reveal that the model is realized on FPGA or ASIC platforms, with a focus on efficient integration of baseband processing and frequency synthesis functionalities. Performance metrics, including quality of service (QoS) improvements, signal-tonoise ratio (SNR), and bit error rate (BER), demonstrate the system's capability to deliver enhanced performance while reducing design complexity. Experimental results and test bench simulations validate the proposed system's functionality and robustness. Comparative analyses further confirm that the new model outperforms traditional synthesizer techniques, showing significant improvements in performance metrics and system efficiency. Overall, this research highlights a successful approach to addressing the high demands of modern SDR applications, ensuring reliable performance across a wide range of frequency bands.

V. FUTURE SCOPE

Explore the integration of the optimized DDFS with nextgeneration communication systems beyond 5G, including 6G and Internet of Things (IoT) networks, where frequency synthesis demands are even higher. Investigate the development of adaptive DDFS architectures that can dynamically adjust error correction and compensation parameters in real-time, based on varying operational conditions and environmental factors.

VI. RESULTS

A. *Error Detector*

Minimum period: (Maximum frequency)	**1.174ns 851.426MHz**
Minimum input arrival time before clock	**0.992ns**
Maximum output required time after clock	**0.511ns**
Maximum combinational path delay	**No path found**

Table 1. Delay

1) Delay: Minimum period: 1.174 ns, corresponding to a Maximum Frequency of 851.426 MHz. This means the design can run up to this maximum clock frequency. Minimum input arrival time before clock: 0.992 ns, indicating how much time the input signal must arrive before the clock edge. Maximum output required time after clock: 0.511 ns, meaning the output must be ready within this time after the clock edge. Maximum combinational path delay: No path found, suggesting there might not be any significant combinational logic paths, or the tool could not determine this parameter. This summary provides a good indication that the design has an excellent maximum frequency and tight timing performance, suitable for high-speed digital applications such as a frequency synthesizer.

Devices utilization			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of slice Registers	24	35200	0%
Number of slice LTUTs	13	17600	0%
Number of fully used LUT-FF pairs	12	25	48%
Number of bonded IOBs	26	100	26%
Number of BUFG/BUFGCTRLs	1	32	3%

Table.2. Area

Area: This table shows how much of the FPGA resources are used for the implementation:
Number of Slice Registers: 24 used out of 35,200 available, which is 0Number of Slice LUTs: 13 used out of 17,600 available, also 0Number of fully used LUT-FF pairs: 12 out of 25 possible pairs used, resulting in 48Number of bonded IOBs (Input/Output Blocks): 26 used out of 100, which translates to 26Number of BUFG/BUFGCTRLs (Clocking Resources): 1 used out of 32 available, showing 3This data indicates that the design is very light in terms of resource consumption, with most of the available FPGA resources unused, making the design quite efficient.

2) Simulation: Key Details in the Waveform: sine out[11:0]:
This signal is a 12-bit output (11:0 indicates the bit range) representing the synthesized sine wave. The value of sine

out changes over time, indicating the generation of a digital sine wave. The X symbols at the beginning indicate an undefined or unknown state, typical during initialization. clk:
This is the clock signal, which is a fundamental timing reference in digital circuits. It shows a regular pattern, alternating between high and low states, which synchronizes the operations of the DDFS. reset:

4.Simulation

The reset signal appears to be held low, which likely means the system is not in a reset state during the simulation. phase[31:0]:

Fig.3.Simulation

This 32-bit signal likely represents the phase accumulator output. The value of the phase signal changes over time, controlling the frequency of the output sine wave. Analysis: The waveform demonstrates a steady operation of a DDFS circuit, where the sine out signal changes in a manner consistent with the digital representation of a sinusoidal signal. The proper synchronization between the clk and the other signals indicates a functioning digital synthesizer design. The presence of the X state initially could imply the beginning of the simulation or the period before the system stabilizes. This simulation waveform can be used to validate the functionality of the DDFS design, ensuring that it generates the desired frequency and waveform characteristics for 5G SDR applications.

B. PLL

Minimum period (Maximum frequency)	**1.558ns 641.84MHz**
Minimum input arrival time before clock	**1.257ns**
Maximum output required time after clock	**0.525ns**
Maximum combinational path delay	**No path found**

Minimum period (Maximum frequency)	***1.222ns 818.465MHz***
Minimum input arrival time before clock	***1.037ns***
Maximum output required time after clock	***0.521ns***
Maximum combinational path delay	***No path found***

Table 3. Delay-PLL

Devices utilization			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of slice Registers	14	35200	0%
Number of slice LTUTs	21	17600	0%
Number of fully used LUT-FF pairs	14	21	66%
Number of bonded IOBs	7	100	7%
Number of BUFG/BUFGCTRLs	1	32	3%

Table.4. Area-PLL

Table.5.Delay-DDFS

Devices utilization			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of slice Registers	35	35200	0%
Number of slice LTUTs	36	17600	0%
Number of fully used LUT-FF pairs	32	39	82%
Number of bonded IOBs	51	100	51%
Number of BUFG/BUFGCTRLs	1	32	3%

Table.6. Area-DDFS

VII. CONCLUSION

In this section, a novel ADPLL frequency synthesizer is proposed for high performance SDR system and its extensive performance metrics in terms of complexity reduction, memory efficiency and throughput rate are presented. Reconfigurable buffer chain enabled concurrent phase matching is incorporated for both parallel computation and reconfigurable dynamic updation. The hardware synthesis results indicated that our proposed ADPLL model offers the 70 and 50 percentages frequency tuning resolution in lower and higher region respectively as compared to existing ring counter enabled DCO and also mitigate both memory constraints and computational complexity with its simplified configurable buffer chains. The performance metrics of the proposed high speed CONFIGURABLE DCO models is compared to other state-of the art CONFIGURABLE and DCO models.

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