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ADVANCED CONTROL STRATEGY TO ENHANCE PERFORMANCE OF D-STATCOM

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ABSTRACT:
The proposed project introduces a new voltage control strategy for a distribution static compensator (DSTATCOM) to enhance its performance in electric grid applications. The control scheme combines two DSTATCOM operation methods, leveraging power factor and voltage magnitude as degrees of freedom to mitigate voltage and current harmonics, balance source currents, improve power factor, regulate voltage during sags and swells, reduce inverter losses, and control load power for improved energy conservation. This advanced DSTATCOM control outperforms conventional operation across all scenarios. Furthermore, the DSTATCOM utilizes a multilevel H-bridge voltage source inverter (VSI) topology. MATLAB/Simulink simulations validate the viability and advantages of the implemented DSTATCOM configuration over conventional topologies

Index Terms—**Distribution static compensator (DSTATCOM), multilevel inverter (MLI), cascaded H-bridge, passive filter, power quality (PQ).**

I. INTRODUCTION

In a static capacitors and passive filters have traditionally been used to improve power quality (PQ). However, fixed compensation, system-parameter-dependent performance, and potential resonance with line reactance are common challenges [2]. To overcome these drawbacks, a static distribution compensator (DSTATCOM) has been developed in the literature [3]-[8]. The DSTATCOM injects reactive and harmonic components into the load currents to ensure the source currents are adjusted, sinusoidal, and in phase with the load voltages.Traditional DSTATCOM designs require a powerful voltage source inverter (VSI) for load compensation. The DSTATCOM's power rating is proportional to the current to be compensated and the DC-link voltage [10]. In a three-phase four-wire system, the DC-link voltage is typically much higher than the maximum phase-to-neutral voltage for proper compensation (in a three-phase three-wire system, it is higher than the phase-to-phase voltage) [2], [10]–[12]. However, increasing the DC-link voltage increases the VSI's rating, size, and the voltage stress on the IGBT switches, leading to higher cost, size, weight, and power consumption.

Traditional DSTATCOM architectures also use an L-type interface filter [13], [14]. The L-filter has high inductance, slow current tracking, and significant voltage drop, necessitating an even higher DC-link voltage. This further increases the size, cost, and power rating of the VSI. Some hybrid topologies have been proposed to address these limitations, using a lower-rated active filter in combination with passive components [15]–[21]. While these reduce the DC-link voltage requirement, the voltage reduction is still limited due to the use of the L-filter. The L-filter's large size and slow response also remain issues. To overcome the L-filter's limitations, an LCL-filter has been proposed as the VSI front-end in the literature [22]–[25]. The LCL-filter provides better current tracking performance while allowing the use of smaller passive components. This reduces the cost, weight, and size of the passive parts. However, the DC-link voltage requirement for the LCL-filter remains similar to the L-filter case. Additionally, the LCL-filter's resonance dampening is a challenge that requires active or passive damping techniques, adding complexity.

This work proposes an enhanced hybrid DSTATCOM topology using an LCL-filter followed by a series capacitor. This reduces the passive component size and the DC-link voltage rating while providing excellent current tracking. It also significantly reduces the damping power loss, making the scheme more efficient and suitable for practical applications.

II. PROPOSED DSTATCOM TOPOLOGY

A three-phase equivalent circuit diagram of the proposed DSTATCOM topology is shown in Fig. 1. It is realized using

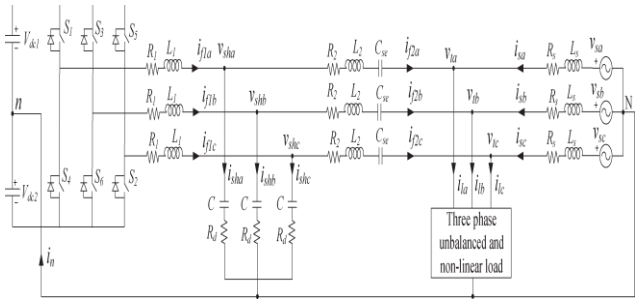


Fig.1. Proposed DSTATCOM topology in the distribution system to compensate unbalanced and nonlinear loads.

The proposed DSTATCOM topology uses a three-phase equivalent circuit schematic, as shown in Figure 1. This circuit employs a three-stage, four-wire, two-level VSI (voltage source inverter) to achieve the desired functionality. The VSI's front end includes an LCL filter, followed by a series capacitor Cse. The LCL filter reduces the size of the filtering inductor and improves the output waveform quality. The series capacitor Cse lowers the DC-link voltage and, consequently, the power rating of the VSI. The LCL filter components are as follows: R1 and L1 are

the VSI-side resistance and inductance, respectively; R2 and L2 are the load-side resistance and inductance; and C is the filter capacitance. A damping resistor Rd is used in parallel with C to dampen oscillations and provide passive damping to the overall system. The VSI and filter currents (if1a, if2a) as well as the voltages (Vsha) and currents (isha) in the shunt branch of the LCL filter are monitored across the three phases. The DC-link capacitor voltages are maintained at a constant reference value (Vdc1 = Vdc2 = Vdcref).The DSTATCOM, source, and loads are all connected to a common point known as the point of common coupling (PCC). The loads can be linear or nonlinear, balanced or unbalanced.

In the standard DSTATCOM topology, the VSI is coupled to the PCC through an inductor Lf. In the LCL filter-based DSTATCOM topology, the LCL filter is placed between the VSI and the PCC.

III. D-STATCOM CONTROL:

Figure 2 depicts the entire control block diagram. The DSTATCOM is programmed to ensure that source currents are balanced, sinusoidal, and in phase with the terminal voltages. In addition, the source provides average load power and losses in the VSI. Because the source in this case is not rigid, using terminal voltages to calculate reference filter currents will not be sufficient compensation. To generate reference filter currents, the fundamental positive sequence components of three-phase voltages are removed.

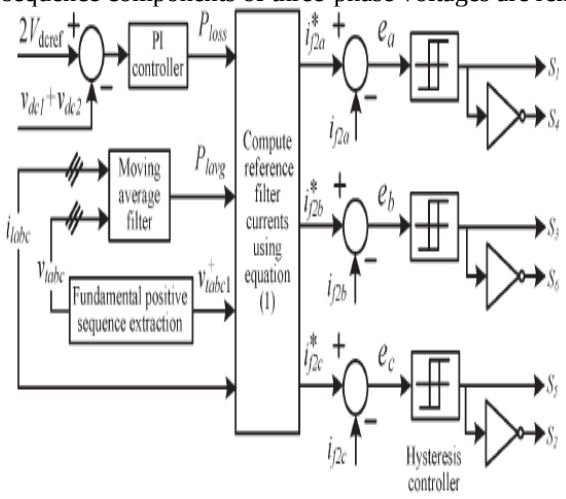


Fig 2 Controller block diagram.

IV.SIMULATION CIRCUITS AND RESULTS

4.1 SIMULATION BLOCK DIAGRAM WITHOUT D-STATCOM/COMPENSATION:

The suggested topology offers several advantages: it requires a lower VSI rating, has a smaller filter inductor value, reduces damping power loss, and improves current compensation. MATLAB software was used to verify all of these benefits. The system parameters utilized to validate the performance are listed below (1).Figure 3 illustrates the unbalanced and distorted three-phase source and load currents, due to the presence of imbalanced linear and nonlinear loads, as well as the feeder impedance. In contrast, Figure 4(a) depicts the balanced and sinusoidal three-phase source currents achieved with the traditional DSTATCOM topology. However, the source currents and PCC voltages shown in Figure 4 contain switching frequency components from the VSI, as seen in the waveforms.

Figure 4(b) shows the imbalanced and distorted three-phase PCC voltages resulting from the feeder impedance. Figure 5 provides further details on the performance of the traditional DSTATCOM, including the three-phase filter currents (c) and the voltages across the higher and lower DC capacitors, as well as the total DC-link voltage (d). The PI controller maintains the voltage across each capacitor at 520V, while the total DC-link voltage is kept at 1040V.

The source currents and PCC voltages are now balanced and sinusoidal, but the switching harmonics ripple is still substantial. The total harmonic distortions (THDs) as a percentage are presented (1). The source currents are slightly increased compared to the typical design to account for power losses in the damping resistor. Furthermore, the total DC-link voltage is maintained at 1040V (the same as the previous approach) to achieve load compensation.

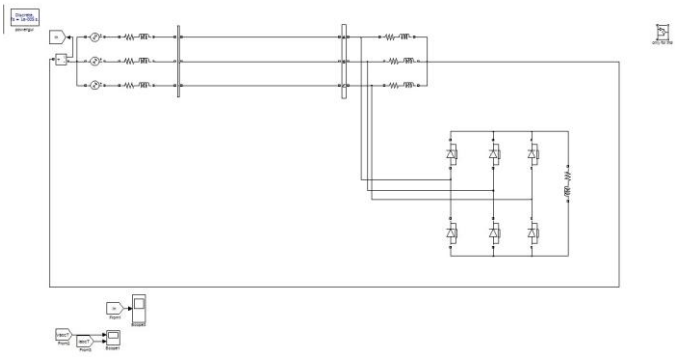


Fig.4.1WITHOUT D-STATCOM/COMPENSATION

4.2 SIMULATION RESULTS:

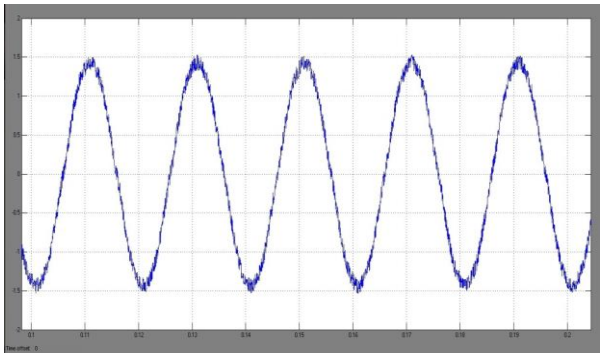


Fig.4.2 (a) wave form for Isa

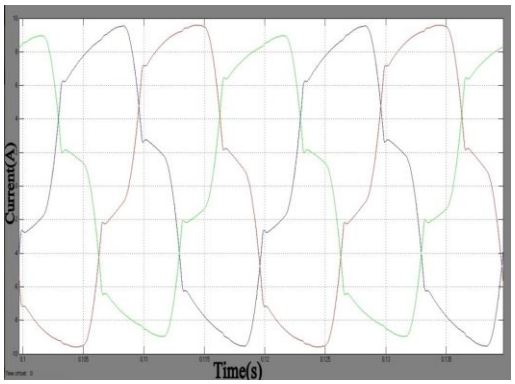


Fig.4.2 (b) Source current:

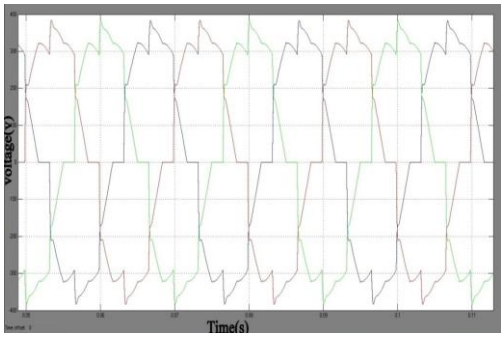


Fig.4.2(C) PCC Voltage

4.3a SIMULATION BLOCK DIAGRAM WITH PROPOSED D-STATCOM:

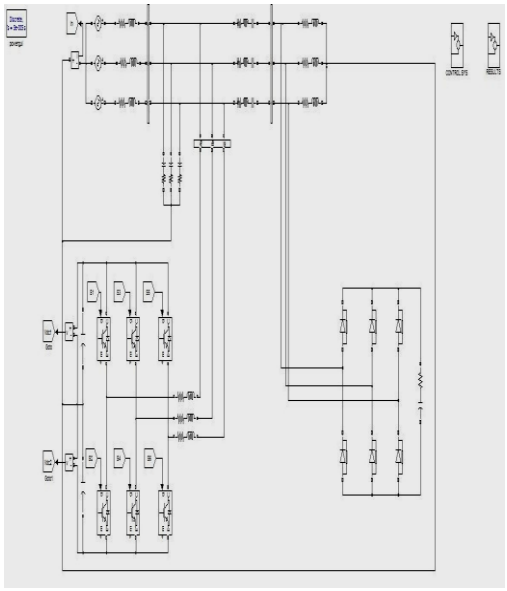
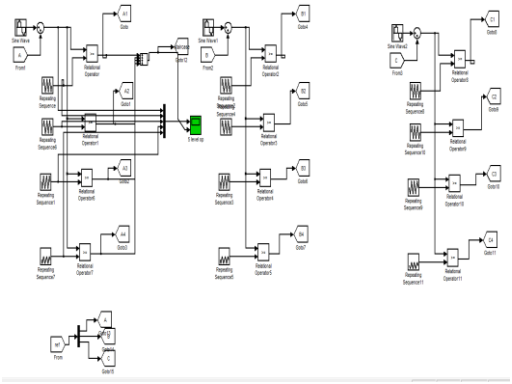


fig 4.3 (b) Control block diagram



4.3.1 SIMULATION RESULTS:

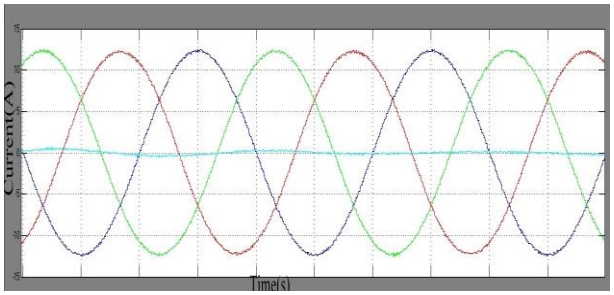


Fig.4.3.1(a)Source currents

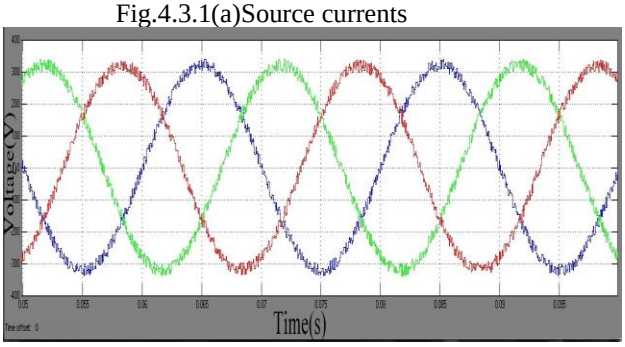


Fig.4.3.1(b) PCC voltages

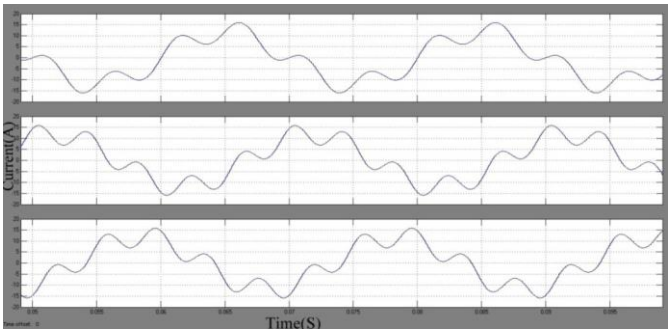


Fig.4.3.1(c) Filter currents

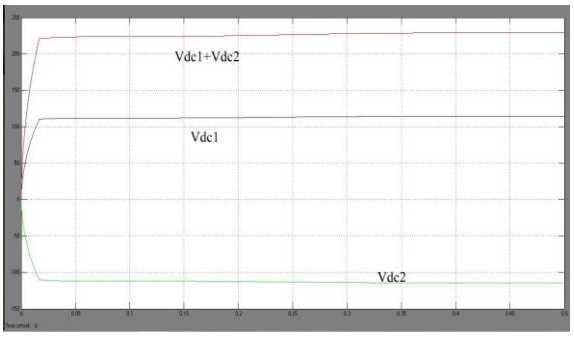


Fig.4.3.1 (d) Voltage across the dc link

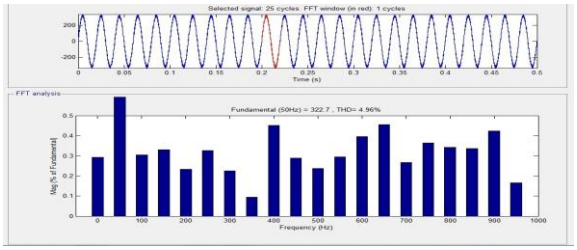
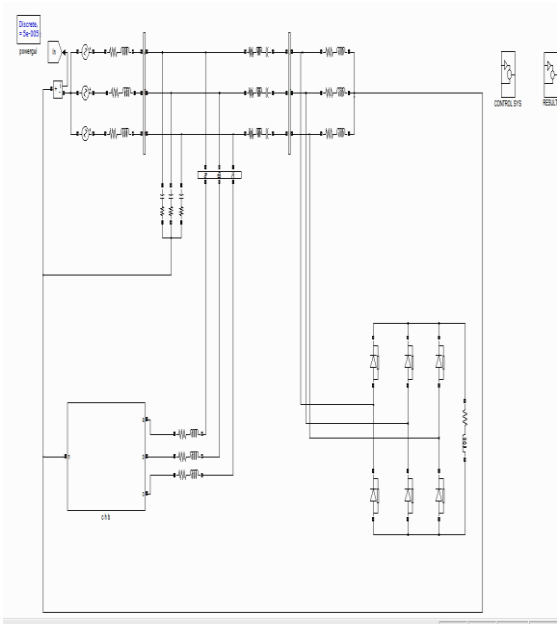
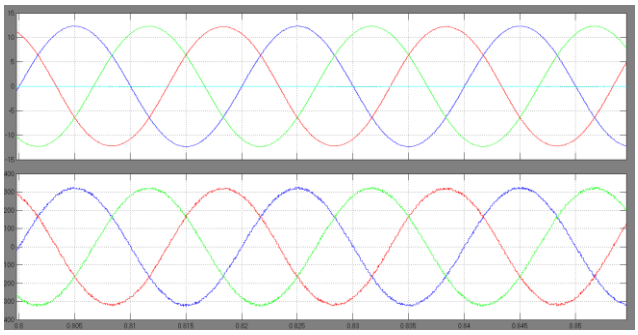


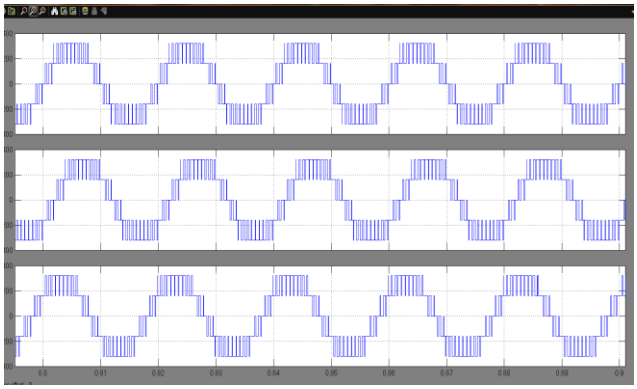
Fig.4.3.1 (e)Reduced Total Harmonic Distortion(4.96%)



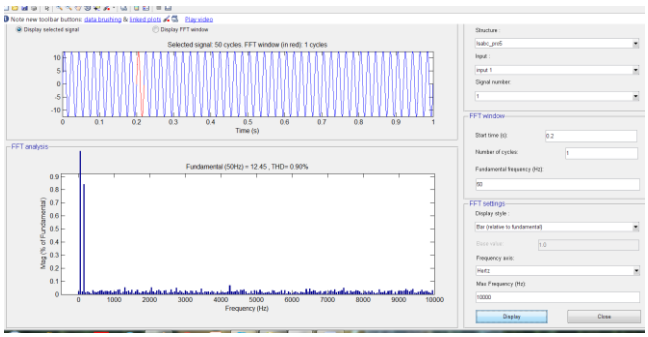
5.1 SIMULINK BLOCK DIAGRAM OF PROPOSED TOPOLOGY



5.2 Source currents and PCC voltages



5.3 Filter voltages



5.4 Reduced Total Harmonic Distortion(0.9%)

VI.CONCLUSION

The paper proposes an enhanced hybrid DSTATCOM architecture to mitigate reactive and harmonic loads. This hybrid interface filter uses a series capacitor following the LCL filter. This design improves the load current compensation capabilities while reducing the dc-link voltage and interfacing filter inductance. Compared to the LCL filter-based DSTATCOM, the current through the shunt capacitor and damping power losses are greatly reduced. As a result, the cost, weight, size, and power rating of the standard DSTATCOM topology are significantly lowered. Additionally, a cascaded multilevel inverter called D-STATCOM greatly reduces the total harmonic distortion. The effectiveness of the proposed topology is verified through extensive MATLAB/simulation.

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