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Advanced Modelling and Assessment of Conventional and Multi-Level Unified Power Quality Conditioner (UPQC) Performance

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ABSTRACT

In the domain of power quality enhancement, both conventional and dual compensation strategies have been widely employed in Unified Power Quality Conditioners (C-UPQC and D-UPQC). However, their comparative analysis often lacks depth, particularly under varying grid conditions. This study introduces an advanced approach by extending the scope to a **Multi-UPQC** configuration, which integrates multiple compensation units to operate in coordination. The paper establishes small-signal models in the dq-axis for both conventional, dual, and multi-UPQC systems, while accounting for the effects of grid impedance and phase-locked loop (PLL) dynamics. A comprehensive performance analysis is conducted under both steady-state and dynamic scenarios, including abrupt changes in grid voltage and load conditions. The results reveal that the D-UPQC demonstrates superior dynamic response under transient conditions, whereas the C-UPQC and D-UPQC show varying capabilities in harmonic suppression. Notably, the impact of grid impedance on load voltage quality is more pronounced in the C-UPQC, whereas the **Multi-UPQC system** effectively overcomes this limitation by distributing the compensation effort across multiple nodes. This collaborative compensation enhances reliability, expands coverage area, and improves both voltage regulation and harmonic mitigation. The study's insights offer valuable guidance in selecting the most suitable compensation strategy for specific grid applications. Experimental validations confirm the accuracy of the proposed comparative framework and the superior adaptability of the Multi-UPQC system.

I. OVERVIEW

Numerous compensatory devices have been developed to address the PQ concerns. These compensation devices could be categorized into three groups according to their topologies: three types of compensating devices: hybrid, shunt, and series. The dynamic voltage restorer (DVR), a type of series compensation device, is capable of mitigating all voltage-related PQ difficulties [5, 6]. However, an excellent shunt compensation device that can suppress all current-related PQ difficulties is the static synchronous compensator (STATCOM) [7], [8]. One intriguing hybrid device to address all voltage- and current-related PQ problems is the unified power quality conditioner (UPQC) [9], [10], [11], [12], [13]. The UPQC's research focuses on conventional and dual compensation strategies from the standpoint of compensation strategies. In the conventional-UPQC (C-UPQC) [14], [15], [16], the shunt converter acts as a current source to keep the grid current balanced, sinusoidal, and in-phase with the voltage at the point of common coupling (PCC), while the series converter acts as a voltage source to keep the load voltage balanced and sinusoidal. Conversely, the series converter in the dual-UPQC (D-UPQC) [17], [18], [19], [20] functions as a current source to

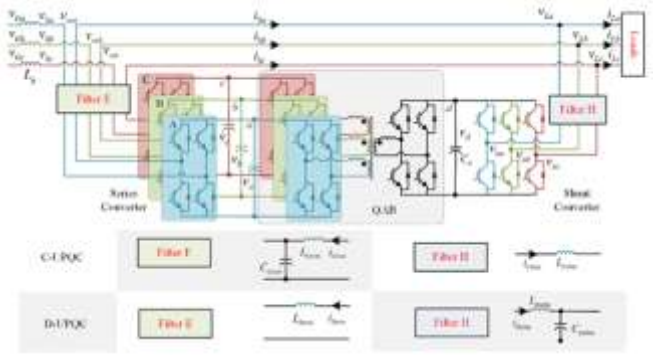


FIGURE 1. Configuration of three-phase UPQC-QAB.

regulate the grid current, while the shunt converter regulates the load voltage by acting as a voltage source. Theoretically, the intended load voltage and grid current

can be tracked error-free by both the C-UPQC and the D-UPQC. However, the topologies, models, and control performance will also differ because of the distinct features of the C- and D-UPQC. The C- and D-UPQC's overall performance evaluation based on proportional resonant (PR) control [22] is shown in [21]. However, the comparative performance analysis ignores a number of crucial criteria. [21] sis. For instance, 1) the phase-locked-loop (PLL) effects are ignored by all closed-loop systems; 2) the control and circuit parameters' impact on control performance is ignored; and 3) the grid impedance's influence is likewise ignored. The proportional integral (PI) control-based dq-axis tiny signal models are developed in order to assess the C- and D-UPQC's performance in a more thorough and realistic manner. The PLL tracks the PCC voltage's phase angle in synchronous rotation frames (SRF) and facilitates the conversion of three-phase AC signals to the DC signals in dq frame [23], [24]. the dq frame's DC signals [23], [24]. Because of its impact on the frequency-domain characteristic, the PLL's dynamics should thus not be disregarded [25]. Furthermore, the static and dynamic performance of the C-and-D-UPQC were thoroughly examined and contrasted using small signal models that took into account the impacts of the PLL and grid impedance.

In conclusion, this study's primary contributions are as follows:

1) This article offers the groundwork for both static and dynamic performance analysis by establishing the dq-axis small signal models of the C- and D-UPQC while taking grid impedance and PLL effects into account.

2) The C- and D-UPQC's static and dynamic performance analyses are contrasted and assessed. It is determined that: (a) When the grid voltage or load experiences abrupt fluctuations, the D-UPQC performs better dynamically; (b) grid voltage harmonics clearly affect the load voltage quality in the C-UPQC; (c) load current harmonics primarily distort the load voltage in the D-UPQC and the gird current in the C-UPQC; and (d) grid impedance primarily affects the load voltage quality in the C-UPQC.

The following is the arrangement of the remaining contents. The UPQC's topologies and average models are presented in Sections II and III. The UPQC's dq-axis small signal models are inferred in Section IV. The comparison of the C- and D-UPQC's performance is shown in Section V. Experimental results are shown and discussed in Section VI. The findings are presented in Section VII. The dq-axis small signal models based on proportional integral (PI) control are established in order to more thoroughly and realistically evaluate the performance of the C- and D-UPQC. The PLL is used in the synchronous rotation frame (SRF) to track the phase angle of the PCC voltage and aids in the realization of the conversion from three-phase AC signals to DC signals in the dq frame [23], [24], so the dynamics of the PLL should not be disregarded due to its impact on the frequency-domain characteristic [25]. Additionally, the static and dynamic performance of the C-and D-UPQC were discussed and compared in detail based on the small signal models that took grid impedance and the PLL into account. To summarize, this study's primary contributions are as follows: 1) The dq-axis small signal models of the C- and D-UPQC are established in this article, taking into account the effects of the grid impedance and PLL, laying the groundwork for both static and dynamic performance analysis; 2) The static/dynamic performance analysis of the C- and D-UPQC is compared and evaluated, and the following conclusions are reached: The remaining contents are arranged as follows: Sections II and III introduce the topologies and average models of the UPQC; Section IV deduces the dq-axis small signal models of the UPQC; Section V presents the comparative performance analysis of the C- and D-UPQC; Section VI presents and discusses experimental results; Section VII presents the conclusions. (a) The D-UPQC has better dynamic performance when the grid voltage or load suffers sudden variation; (b) Grid voltage harmonics have an obvious influence on the load voltage quality in the C-UPQC; (c) Load current harmonics primarily distort the gird current in the C-UPQC and load voltage in the D-UPQC; (d) Grid impedance has an influence on the load voltage quality in the C-UPQC.

II. TOPOLOGIES OF THREE-PHASE C- AND D-UPQC

Fig. 1 shows the circuit configuration of a quadruple-active-bridge based UPQC (UPQC-QAB) [26]. It is primarily composed of series converters consisting of three single phase (TSP) H-bridges, a three-phase shunt converter, and a QAB [27] with four DC ports, of which one DC port (port d) is connected to the shunt converter and the other three (ports a, b, and c) are connected to the

series converters. The LC filter is used to suppress the high-frequency voltage harmonics at the series side of the C-UPQC, which also controls the shunt converter as a current source. As a result, the L filter is used to reduce the high frequency current harmonics at the shunt side. Conversely, with the D-UPQC, the series converter is used as a current source to directly control the grid current. Since the shunt converter is used as a voltage source to directly regulate the load voltage, the LC filter is therefore employed at the series side. Adopted at the hunt side. The primary distinctions between the C- and D-UPQC topologies are these.

III. ABOVE MODELSOFC-ANDD-UPQC

The LC and L filter parameters in the C- and D-UPQC are maintained at the same level for convenience. In particular,

$$\begin{cases} L_{Csrm} = L_{Dshm} = L_V \\ L_{Csrm} = L_{Dshm} = L_V \\ L_{Csrm} = L_{Dshm} = L_f \end{cases} \quad (1)$$

wherem is {a,b,c}. The subscripts "C" and "D" stand for the variables in the C- and D-UPQC, respectively. "Sr" and "sh," the subscripts, are the linked variables of the series and shunt converters. Filter inductance and capacitance of the LC filter are denoted as LV and CV. LI is the filter's inductance.

Furthermore, this study ignores the DC-link voltage's dynamic since it is significantly slower than the grid current [25].

The average of the three-phase UPQC

Figure 1 shows the average model of the series converter for the C-UPQC (without line frequency transformers) as

$$\begin{cases} C_V dv_{srm}/dt = i_{Csrm} - i_{Sm} \\ L_V dv_{Crm}/dt = -v_{Csrm} + v_{Cim} \end{cases} \quad (2)$$

where iSm is the grid current and vsrm is the series injected voltage. iCsrm is the filter's inducer current. vCimis is the series converter's output voltage.

The Kirchhoff's law states that the C-UPQC's gridcurrent can be expressed as

$$i_{Sm} = i_{Lm} - iC_{shm} \quad (3)$$

where iCshmist the injected current and iLmist the load current.

The Shunt Converter's average model is expressed as (4).

$$L_1 di_{Cshm}/dt = V_{com} - v_{Lm} \quad (4)$$

where Lmist the load voltage, vCompose the shunt converter's output voltage.

Additionally, the connection between the load and PCC voltage

(vSm) is expressed as

$$v_{Lm} = v_{Sm} + v_{srm} \quad (5)$$

By combining (2) through (5) and using the abc/dq coordinate transformation, the C-UPQC's dq-axis state-space representation is provided by

$$X_c = A_{xc} + B_{uC} + W_C \quad (6)$$

In this case, the subscript "dq" represents the d-and-q-axis components of associated variables. ω is the gridangular frequency.

B. AVERAGE MODE OF THE THREE-PHASED-UPQC

According to Figure 1, the average model of these converters for the D-UPQC is written as

$$L_1 di_{sm}/dt = V_{Dim} - v_{Lm} + v_{sm} \quad (7)$$

where the output voltage of these converters is dimmed.

For the D-UPQC, the average model of the shunt converter is written as

$$\begin{cases} C_V dv_{srm}/dt = i_{Lm} + i_{sm} - i_{Dshm} \\ L_V dv_{Dshm}/dt = -v_{Dom} - v_{Lm} \end{cases} \quad (8)$$

where Dshm is the shunt filter's inducer current in the D UPQC. The output voltage of a shunt converter is represented by vDom.

Using the Park transformation, (7)–(8) are expressed as

$$X_D = A_{xD} + B_{uD} + W_D \quad (9)$$

where the matrices in (6) are identical to those in A and Bin (9). With reference to (6), the control quantities in the C-UPQC will contain dvSm/dt and diLm/dt if the

controllers directly control the load voltage and grid current. These characteristics will impact the C-UPQC's dynamic performance. According to the D-UPQC model (9), it is practical to directly manage the grid current and load voltage [21].

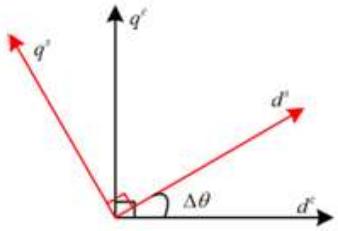


FIGURE2. The system and control frames.

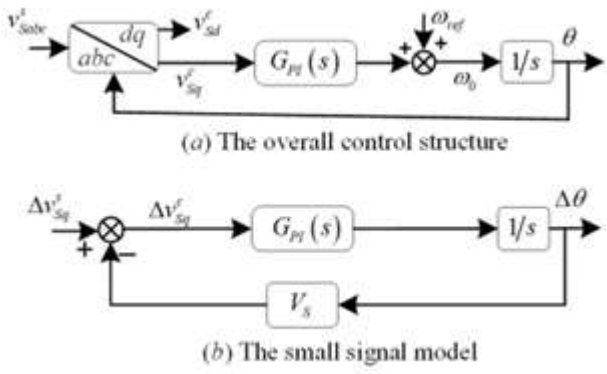


FIGURE3. The control block diagram of the SRF-PLL

IV. Small Sign Language Design of UpQC

In this section, the dq-axis small signal models are created to examine the static and dynamic performance of the UPQC. Both the C-UPQC converter and the D-UPQC shunt converter use the dual closed loop control technique to enable comparison analysis. The inner inductor current loop uses proportional (P) control, while the outer load voltage loop uses PI control. As a result, both the C-UPQC's shunt converter and the D-UPQC's series converter employ the dual closed loop control system, with the PI control scheme being used for the inner grid current loop and the outer DC-link voltage loop.

A. Small Sign Language OFPLL

Both this and shunt controllers of the UPQC must monitor the phase angle of the PCC voltage in order to regulate the output voltages of the series and shunt converters based on the PI control schemes. Nevertheless, when the PCC voltage is disrupted, the controller's input phase angle is impacted via the PLL, which then affects the state variables (such voltage and current) in the controller coordinate [25].

The UPQC system (dsqs) and control (dcqc) frames are displayed in Fig. 2. The variables in the system and control coordinates are denoted by the superscripts "s" and "c." The "sign" stands for a disturbance signal. As can be seen, the control frame is defined by the PLL, and the rotation speed is influenced by the PLL's output, whereas the system frame is defined by the actual PCC voltage and rotates in accordance with the actual PCC synchronous angular speed. When the system and control frame coincide in the steady-state, the PLL can detect the error-free tracking of the PCC voltage; when the PCC voltage is disrupted,

A phased discrepancy θ will exist between the control frames and the system. The following relationship might be derived from Fig. 2.

$$n^c_{dq} = \begin{bmatrix} cos(\Delta\theta) & sin(\Delta\theta) \\ -sin(\Delta\theta) & cos(\Delta\theta) \end{bmatrix} \boldsymbol{n}^s_{dq} \quad (10)$$

$$\Delta\theta = \frac{G_{PI}(s)}{s+G_{PI}(s)V_S}\Delta v^s_{Sq} \quad (12)$$

where the proportional and integral gains of the PI controller are denoted by kPpll and kIpll. Because the controller monitors the PCC voltage's phase angle, the following relationship is realized:

$$\begin{bmatrix} V^s_{Sd} \\ V^s_{Sq} \end{bmatrix} = \begin{bmatrix} V_S \\ 0 \end{bmatrix} \quad (13)$$

$$\Delta\boldsymbol{n}^c_{dq} = \Delta\boldsymbol{n}^s_{dq} + \begin{bmatrix} 0 & \frac{G_{PI}(s)N^s_q}{s+G_{PI}(s)V_s} \\ 0 & \frac{G_{PI}(s)N^s_q}{s+G_{PI}(s)V_s} \end{bmatrix} .\Delta\boldsymbol{v}^s_{Sdq} \quad (14)$$

Following the perturbation of (10), the relationship that follows is obtained.

B. UPQCCIRCUIT SMALL SIGNAL MODELING 1) SMALL SIGNAL MODELING OFTHEC-UPQCCIRCUIT

Figure 4 illustrates the C-UPQC circuit's dq-axis tiny signal model. The frequency-domain dynamic of the series converter circuit is expressed using the average model (6) as

$$\Delta \boldsymbol{v}^{s}_{Cidq} - \Delta \boldsymbol{v}^{s}_{srdq} = \boldsymbol{Z}_{LV}(s).\Delta\, \boldsymbol{i}^{s}_{srdq} \quad (15)$$

$$\Delta \boldsymbol{i}^{s}_{Sdq} - \Delta \boldsymbol{i}^{s}_{Crdq} = \boldsymbol{Z}_{LV}(s).\Delta \boldsymbol{v}^{s}_{srdq} \quad (16)$$

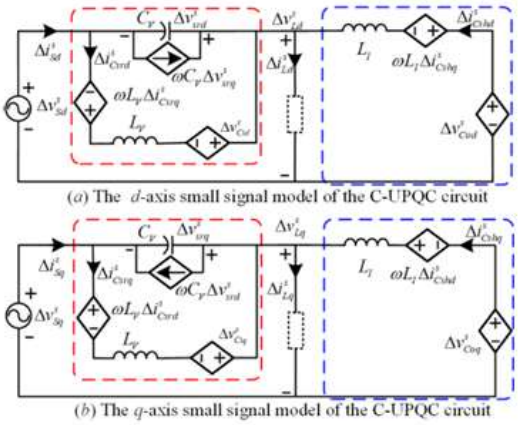
Consequently, the C-UPQC's shunt converter circuit's dynamic is provided by

Where $\boldsymbol{Z}_{LV}(s) = \begin{bmatrix} sL_V & -\omega L_V \\ \omega L_V & sL_V \end{bmatrix}, \boldsymbol{Z}_{CV}(s) = \begin{bmatrix} sC_V & -\omega C_V \\ \omega C_V & sC_V \end{bmatrix}$

$$\Delta \boldsymbol{i}^{s}_{Codq} - \Delta \boldsymbol{v}^{s}_{Ldq} = \boldsymbol{Z}_{L1}(s).\Delta \boldsymbol{i}^{s}_{Ldq} - \Delta \boldsymbol{i}^{s}_{Sdq} \quad (17)$$

Where

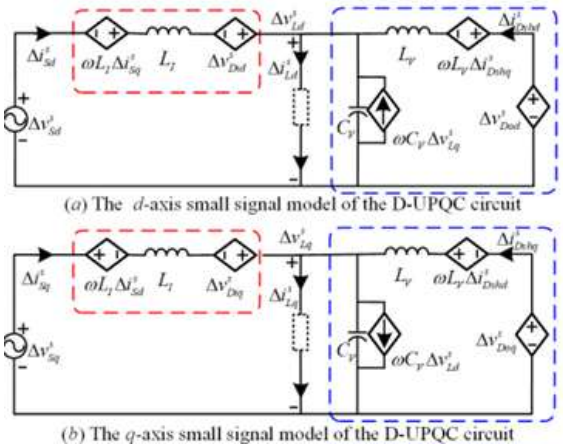
$$\boldsymbol{Z}_{CV}(s) = \begin{bmatrix} sL_1 & -\omega L_1 \\ \omega L_1 & sL_1 \end{bmatrix}$$



(a) The d-axis small signal model of the C-UPQC circuit

(b) The q-axis small signal model of the C-UPQC circuit

FIGURE4. The dq-axis small signal model of the C-UPQC circuit.



(a) The d-axis small signal model of the D-UPQC circuit

(b) The q-axis small signal model of the D-UPQC circuit

FIGURE5. The dq-axis small signal model of the D-UPQC circuit.

2) THE UPQCCIRCUIT'S SMALLSIGNALMODELING

Fig. 5 displays the D-UPQC circuit's tiny signal model. The frequency-domain dynamic of these converter circuits can be expressed as

$$\Delta \boldsymbol{v}^{s}_{Didq} - \Delta \boldsymbol{i}^{s}_{Lidq} = \boldsymbol{Z}_{CV}(s).\Delta \boldsymbol{v}^{s}_{Ldq} \quad (18)$$

The D-UPQC's shunt converter circuit's infrequency domain dynamic is expressed as

$$\Delta \boldsymbol{i}^{s}_{Sdq} + \Delta \boldsymbol{i}^{s}_{Dshdq} - \Delta \boldsymbol{i}^{s}_{Ldq}(s) =.\Delta\, \boldsymbol{i}^{s}_{srdq} \boldsymbol{Z}_{CV}(s).\Delta \boldsymbol{v}^{s}_{Ldq} \quad (19)$$

$$\Delta \boldsymbol{v}^{s}_{Dodq} - \Delta \boldsymbol{v}^{s}_{Ldq} = \boldsymbol{Z}_{CV}(s).\Delta \boldsymbol{i}^{s}_{Dshdq} \quad (20)$$

Additionally, because of the grid impedance, the grid-to-PCC voltage relationship is stated as

$$\Delta \boldsymbol{v}^{s}_{Gdq} - \Delta \boldsymbol{v}^{s}_{sdq} = \boldsymbol{Z}_{g}(s).\Delta \boldsymbol{i}^{s}_{sdq} \quad (21)$$

C. Small Sign Language Design of UPQC

1) THEEC-UPQC SMALLSIGNALMODELING

The dual closed-loop control block diagram of these converters for the C-UPQC is displayed in Fig. 6(a). The output of the outer voltage loop PI controller is displayed by Fig. 6(a).

$$\Delta \boldsymbol{i}^{c}_{Csdqr} = G_{Cvv}(s).\boldsymbol{I}.\Delta \boldsymbol{v}^{C}_{Ldqr} - \Delta \boldsymbol{v}^{C}_{Ldqr} \quad (22)$$

$$G_{Cvv}(s) = k_{Cvvp} + k_{Cvvi}/\boldsymbol{s} \quad (23)$$

where the transfer function (TF) of the outer loop PI controller is GCvv(s). The gains are kCvvp and kCvvi, in that order. is a 2x2 identity matrix. In equation (22) the input vc Ldq is taken from equation (14) and the difference value vc Ldqr is given explicitly.

$$\Delta \boldsymbol{v}^{c}_{Ldq} = \Delta \boldsymbol{v}^{s}_{Ldq} + F_{CL}(s).\Delta \boldsymbol{v}^{s}_{sdq} \quad (24)$$

Where

$$F_{CL}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s)V_{Lq}^{S}}{s+G_{PI}(s)V_S} \\ 0 & -\frac{G_{PI}(s)V_{Lq}^{S}}{s+G_{PI}(s)V_S} \end{bmatrix}$$

The UPQC-P[9] methodology is applied in this investigation. The load voltage should therefore be in phase with the PCC voltage following adjustment (VsLd=VS0 and VsLq=0V). The output of the series converter's inner current loop PI controller is shown in Fig. 6(a) as

$$\Delta \boldsymbol{i}_{Csrdq}^{c} = \Delta \boldsymbol{i}_{Csrdq}^{s} + F_{Cr}(s).\Delta \boldsymbol{v}_{sdq}^{s} \quad (25)$$

Where

$$F_{CL}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s)V_{Lq}^{S}}{s+G_{PI}(s)V_S} \\ 0 & -\frac{G_{PI}(s)V_{Lq}^{S}}{s+G_{PI}(s)V_S} \end{bmatrix} \begin{bmatrix} I_{Csrd}^{S} \\ I_{Csrd}^{S} \end{bmatrix}, \quad (26)$$

where kCvip is the Pcontroller's gain. The input ic Csrdq is acquired by using the transformation (14) and the inductor current reference ic Csrdqr is obtained from equation (22).

$$\Delta \boldsymbol{i}_{Csrdq}^{c} = \Delta \boldsymbol{i}_{Csrdq}^{s} + F_{Cr}(s).\Delta \boldsymbol{v}_{sdq}^{s} \quad (27)$$

Given the impact of the PLL and control delay Gd(s), the connection between vc Cidqr and vs Cidq is stated as

$$\Delta \boldsymbol{v}_{Cirdq}^{c} = \Delta \boldsymbol{v}_{Cidqr}^{c} - F_{Ci}(s).\Delta \boldsymbol{v}_{sdq}^{s} \quad (28)$$

$$\Delta \boldsymbol{v}_{Cidq}^{s} = K_{PWM}G_{d}(s).\boldsymbol{I} + \Delta \boldsymbol{v}_{Cidqr}^{s} \quad (29)$$

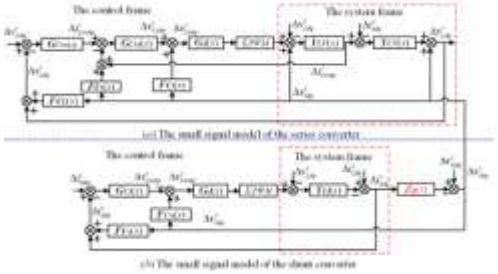


FIGURE6. The dq-axis small signal model of the C-UPQC.

where the sampling period is Ts. The PWMgain is KPWM.

When (6) and (13) are combined, the steady-state output voltage for these converters is expressed as

$$\begin{bmatrix} V_{Cid}^{s} \\ V_{Cid}^{s} \end{bmatrix} = \begin{bmatrix} (1-\omega^2 L_V)(V_{s0}-V_S)/K_{PWM} \\ \omega L_V V_{s0} I_{Ld}^{s}/K_{PWM}V_S \end{bmatrix} \quad (30)$$

Consequently, the load voltage in the C-UPQC is expressed as

$$\Delta v_{Ldq}^{s} = G(s)\Delta i_{sdq}^{s} + G_2(s)\Delta_{sdq}^{s} C G_3(s)\Delta v_{Ldqr}^{c} \quad (31)$$

where, as indicated by the equation at the bottom of the following page.

Fig. 6(b) displays the grid current-loop control block diagram of the C-UPQC's shunt converter. The gridcurrent loop PI controller's output is provided by

$$\Delta v_{Codqr}^{c} = -G_{ci}(s).I.(\Delta i_{Sdqr}^{c} - \Delta i_{Sdq}^{c}) \quad (32)$$

$$G_{Ci}(s) = k_{Cip} + k_{Cii}/s \quad (33)$$

which are the gains of the grid current PI controller, kCip and kCii.

The d-axis grid current reference value, icSdr, is provided directly by the DC voltage loop in equation (32) and is thought to have a constant value. The reference value icSqr for the q-axis current is supplied as 0A.

Using the transformation, the input ic Sdq is obtained (14)

$$\Delta i_{Sdq}^{c} = \Delta i_{Sdq}^{c} + F_{Cs}(s).\Delta v_{Sdq}^{s} \quad (34)$$

The link between vc Codqr and vs Codq is described in Fig. 6(b).

$$\Delta v_{Codqr}^{s} = \Delta v_{Codqr}^{c} - F_{Co}(s).\Delta v_{Sdq}^{s} \quad (35)$$

$$\Delta v_{Codq}^{s} = K_{PWM}.G_{d}(s).I.\Delta v_{Codqr}^{s} \quad (36)$$

Where

$$F_{co}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s)V_{Lq}^{s}}{s+G_{PI}(s)V_{S}} \\ 0 & -\frac{G_{PI}(s)V_{Lq}^{s}}{s+G_{PI}(s)V_{S}} \end{bmatrix}, \begin{bmatrix} V_{Cod}^{s} \\ V_{Cod}^{s} \end{bmatrix}$$
$$= \begin{bmatrix} (V_{S0} - \omega L_1 I_{Lq}^{s}) & /K_{PWM} \\ \omega L_1 I_{Lq}^{s}\left(1 - \frac{V_{S0}}{V_S}\right) & /K_{PWM} \end{bmatrix}$$

Consequently, the grid current's expression in the C-UPQC is represented as

$$\Delta i_{sdq}^{s} = G_4(s)\Delta v_{sdq}^{s} + \Delta v_{Ldq}^{s} + G_6(s)\Delta v_{Ldq}^{s} \quad (37)$$

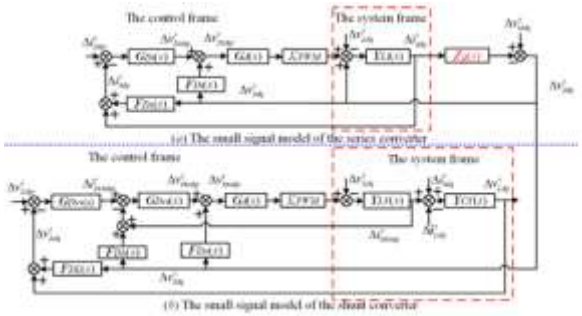


FIGURE7. The dq-axis small signal model of the D-UPQC.

$$G_{LG}(s) = \frac{\Delta v_{Ldq}^{s}}{\Delta v_{Gdq}^{s}} = \left[\boldsymbol{I} - \boldsymbol{JK^{-1}G_5(s)}\right]^{-1} \left[\boldsymbol{G_{LG}(s)} + \boldsymbol{JK^{-1}G_4(s)}\right]$$
$$G_{LL}(s) = \frac{\Delta v_{Ldq}^{s}}{\Delta v_{Gdq}^{s}} = \left[\boldsymbol{I} - \boldsymbol{JK^{-1}G_5(s)}\right]^{-1}\boldsymbol{JK^{-1}G_6(s)} \quad (38)$$

$$G_{LG}(s) = \frac{\Delta v_{Ldq}^{s}}{\Delta v_{Gdq}^{s}} = \left[\boldsymbol{I} - \boldsymbol{JK^{-1}G_5(s)}\right]^{-1} \left[\boldsymbol{G_{LG}(s)} + \boldsymbol{JK^{-1}G_4(s)}\right]$$
$$G_{LL}(s) = \frac{\Delta v_{Ldq}^{s}}{\Delta v_{Gdq}^{s}} = \left[\boldsymbol{I} - \boldsymbol{JK^{-1}G_5(s)}\right]^{-1}\boldsymbol{JK^{-1}G_6(s}$$

(39)

2) THED-UPQC SMALLSIGNALMODELING

The gridcurrent-loop control block diagram of these converters for the D-UPQC is displayed in Fig. 7(a). The gridcurrent loop PI controller's output is visible as

$$\Delta v_{Didqr}^{C} = G_{Di}(s).I.\left(\Delta i_{Sdqr}^{c} - \Delta i_{Sdqr}^{c}\right) \quad (40)$$

$$G_{Di}(s) = k_{Dip} + k_{Dii}/s \quad (41)$$

where the grid current PI controller's gains are denoted by kDip and kDii.

The connection between vc Didqr and vs Didq is stated as

$$\Delta v_{Didqr}^{s} = \Delta v_{Didqr}^{s} - F_{Di}(s).v_{Sdq}^{s} \quad (42)$$
$$G_{Di}(s) = K_{PWM}.G_d(s).I.\ \Delta v_{Didqr}^{s} \quad (43)$$

Consequently, the grid current's expression in the D-UPQC is expressed as

$$\varphi_1(s) = \Delta v_{sdq}^{s} + \varphi_2(s)\Delta v_{Ldq}^{s} + \varphi_3(s)]G_{sdqr} \quad (44)$$

where

FCs(s)=FDs(s).

Figure 7(b) shows the dual closed-loop control block diagram of the D-UPQC's shunt converter. The output of the outervoltageloop is shown in Fig. 7(b).

$$\Delta i_{Dshdqr}^{s} = G_{Dvv}(s).I.\left(\Delta v_{Ldqr}^{c} - \Delta v_{Ldq}^{c}\right) \quad (45)$$

$$G_{Dvv}(s) = k_{Dvvp} + k_{Dvvi}/s \quad (46)$$

where kDvvp and kDvvia are the gains, and GDvv(s) is the output loop PI controller's transfer function.

TABLE1.Main circuit parameters for the UPQC-QAB.

Symbol	Description	Value
v_{Gm}	Grid voltage (line-to-line)	380V
ω	Grid angular frequency	314rad/s
L_Y	Filter inductance of the LC filter	6mH
C_Y	Filter capacitance of the LC filter	80μF
L_I	Filter inductance of the L filter	4mH
v_m	Port voltage of series DC-link	400V
v_d	Port voltage of shunt DC-link	800V
C_m	Capacitance of DC port *m*	1e3μF
C_d	Capacitance of DC port *d*	4e3μF

The output of the inner current loop P controller is shown in Fig. 7(b).

$$\Delta v_{Dodqr}^{c} = G_{Dvi}(s).I.\left(\Delta i_{Dhdqr}^{c} - \Delta i_{Dshdq}^{c}\right)$$

(47)

$$G_{Dvi}(s) = k_{Dvip}$$

(48)

where the P controller's gain is Dvip.
According to (14), the variable's association with ic Dshdq is stated as

$$\Delta v_{Dodq}^{c} = \Delta v_{Dshdq}^{s} + F_{Dh}(s).v_{Sdq}^{s}$$

(49)

The connection between the shunt converter's control output and system input is then described.

$$\Delta v_{Dodq}^{s} = \Delta v_{Dshdq}^{c} + F_{Dh}(s).v_{Sdq}^{s}$$

(50)

$$\Delta v_{Dodq}^{s} = K_{PWM}\,.G_{d}(s).I.\Delta v_{Sdq}^{s}$$

(51)

According to Fig. 7(b), the load voltage in the D-UPQC is expressed as

$$\Delta v_{sLq}^{s} = \varphi_4(s) = \Delta v_{sdq}^{s} + \varphi_5(s)\Delta v_{Ldq}^{s} + \varphi_6(s) + \varphi_7(s)\Delta i_{sdq}^{s}$$

(52)

with, as indicated by the formula at the bottom of the following page, where FDL(s)=FCL(s).

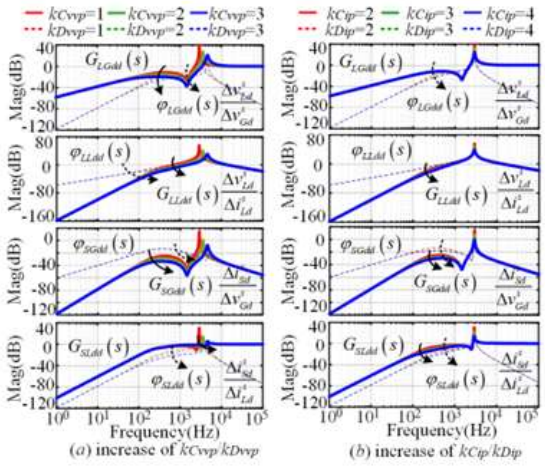


FIGURE 9. Frequency response of TFs under different control parameters.

V. UPQC CONTROLL PERFORMANCE ANALYSIS

Section IV provides a detailed deduction of the C- and D-UPQC's dq-axis small signal models. The performance of the load voltage and grid current in the C and D-UPQC will be further compared and examined in this part based on the models mentioned above. Furthermore, the system engineering design technique is used to create the UPQC's control parameters [23]. Both strategies make use of dual closed-loop PI control for the load voltage controllers. In general
The outer voltage loop's bandwidth should be less than 1/10 of the inner current loop's bandwidth, while the inner current loop's bandwidth should not exceed $0.1*2\pi*fsw$ (fsw is the switching frequency). Consequently, both of the methods make use of the PI control for the grid current controllers.
The load voltage controller can be referred to as the grid current loop's parameter design. Tables 1 and 2 display the UPQC's electrical and control parameters. The transition

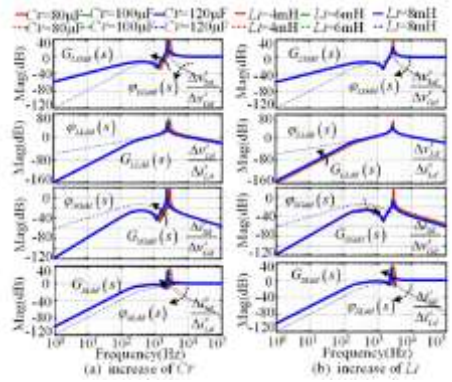


FIGURE 10. Frequency response of TFs under different circuit parameters.

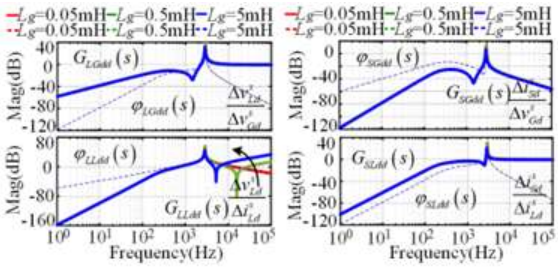


FIGURE 11. Frequency response of TFs under different grid impedance.

The frequencies for the QAB, shunt, and series converters are 20 kHz, 20 kHz, and 50 kHz, respectively.

A. VOLTAGE/CURRENT HARMONICS' INFLUENCE

1) PERFORMANCE OF LOAD VOLTAGE TRACKING

First, the topologies' performance in tracking load voltage is examined. The load voltage in the C-UPQC performs poorly in reducing the high-frequency grid voltage harmonics because the capacitive reactance of the LC filter is inversely proportional to the frequency. Furthermore, the shunt L filter's inductive reactance is proportional to the

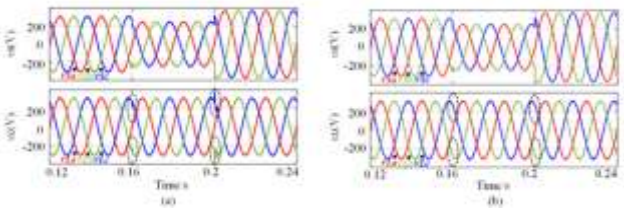


FIGURE 12. The simulation waveforms under grid voltage sag and swell: (a) C-UPQC, (b) D-UPQC.

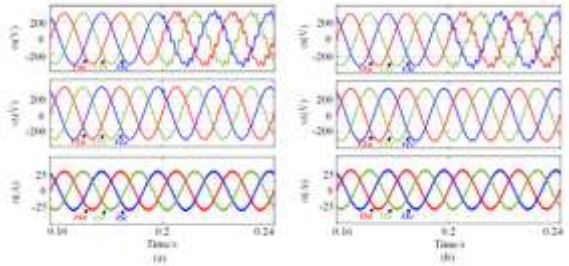


FIGURE 13. The simulation waveforms under grid voltage harmonics distortion: (a) C-UPQC, (b) D-UPQC.

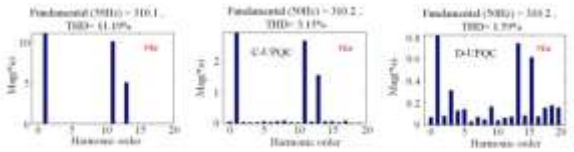


FIGURE 14. The spectrum analysis of vSa and vLa under grid voltage harmonics distortion.

frequency, hence the C-UPQC's shunt converter tends to suppress the load currents' high frequency components. It causes high frequency current harmonics to enter the electrical system, which has an impact on load voltage and grid current. However, because the capacitor CDshm has a lower capacitive reactance in the D-UPQC, high-frequency load current harmonics tend to pass through it. As a result, in the D-UPQC, the load current harmonics mostly influence the load voltage.

Second, the small signal model ((38) and (53)) is used to analyze the load voltage tracking performance. The d-axis coordinate system is used as an example for convenience.

Figure 8(a)(c) provides an example for drawing the pertinent TF bode diagrams. The bode diagram for G3dd(s) and ϕ5dd(s) (G3(s) = ϕ5(s)) is displayed in Fig. 8(a). As can be observed, the load voltages vs. Ld in the C- and D-UPQC enable error-free tracking of the reference signal vs. Ldr. The amplitude of GLGdd(s) is typically greater than that of ϕLGdd(s), as seen in Fig. 8(b); in particular, the amplitude of GLGdd(s) is equal to 0dB in the high frequency range. In Fig. 8(c), the amplitude of GLLdd(s) is smaller than that of ϕLLdd(s) in the low frequency region, and the load voltage is unable to counteract the influence of the grid current harmonics (1~10kHz). Consequently, the grid voltage

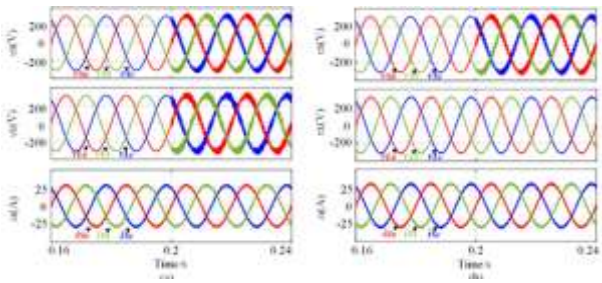


FIGURE 15. The simulation waveforms under high-frequency grid voltage harmonics distortion: (a) C-UPQC, (b) D-UPQC.

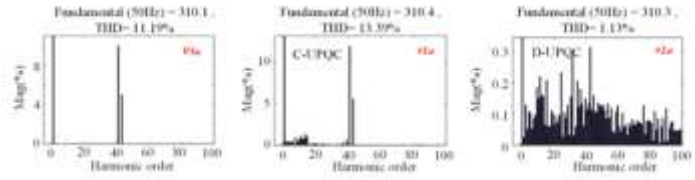


FIGURE 16. The spectrum analysis of vSa and vLa under high-frequency grid voltage harmonics distortion.

The load voltage in the C-UPQC is mostly distorted by harmonics; in two schemes, the load voltages are distorted by the load current harmonics.

2) GRID PERFORMANCE IN TRACKING CURRENTLY

Due to its stronger inductive reactance in the high frequency band, the D-UPQC topology performs better than the others at preventing load current harmonics from entering the power grid. The high frequency load current harmonics are blocked by the shunt converter in the C-UPQC.

The TF bode diagrams of the d-axis grid current loop in the C- and D-UPQC are then displayed in Fig. 8(d)-(f) based on the small signal models ((39) and (54)). The reference signal in Fig. 8(d) (G7dd(s) = ϕ3dd(s)) can be tracked error-free in both systems when the gird current is Sd.

The amplitude of ϕSGdd(s) and GSGdd(s) is always less than 0dB, as shown in Fig. 8(e), even if the amplitude of ϕSGdd(s) is larger than that of GSGdd(s) in the low frequency range. The amplitude of GSLdd(s) is always greater than that of ϕSLdd(s) in Fig. 8(f); in the high frequency range, in particular, the amplitude of GSLdd(s) equals 0dB. Consequently,

The C-UPQC's current quality is impacted by load current harmonics, and the impact of grid voltage harmonics on grid current is not immediately apparent in two plans.

TABLE 3. Load parameters in the simulations.

Load 1	$Ra = 10\Omega$; $La = 10mH$ $Rb = 10\Omega$; $Lb = 10mH$ $Rc = 10\Omega$; $Lc = 10mH$
Load 2	Rectifier load: $R = 10\Omega$; $L = 10mH$

B. IMPACT OF CIRCUIT AND CONTROL PARAMETERS

The control performance of the UPQC is examined in this subsection under various control and circuit parameters (kDvvp, kCvvp, kDip, kCip, CV, and LI).

The associated TF bode diagrams of the C and D-UPQC under various control parameters are displayed in Fig. 9. when can be observed, all of the TF amplitudes tend to drop when kDvvp/kCvvp and kDip/kCip (the bandwidth of the load voltage and grid current loop) grow. This indicates that in both approaches, improving the bandwidth of the outer load voltage and grid current loop contributes to better load voltage and grid current quality. Fig. 10 displays the associated TF bode graphs under various filter parameters. It is demonstrated that the amplitudes of the TFs in the D-UPQC typically decrease when CV or LV rises, but these amplitudes in the C-UPQC typically increase. In other words, raising the filter's inductance and

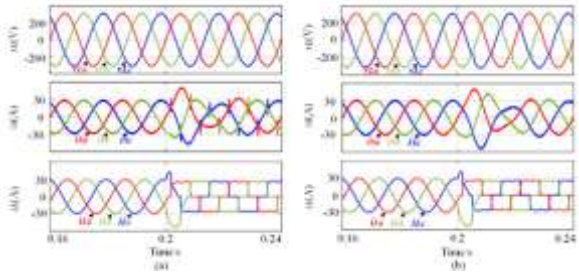


FIGURE 17. The simulation waveforms under different loads: (a) C-UPQC, (b) D-UPQC.

In the D-UPQC, capacitance can enhance the grid current quality and load voltage.

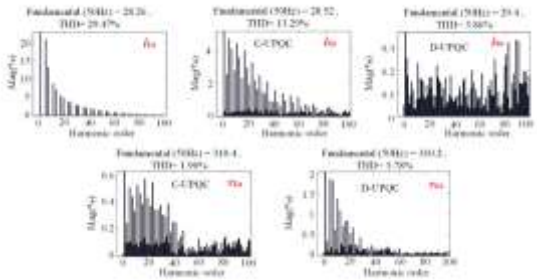


Figure 18. The spectrum analysis of iLa , iSa and vLa under different loads.

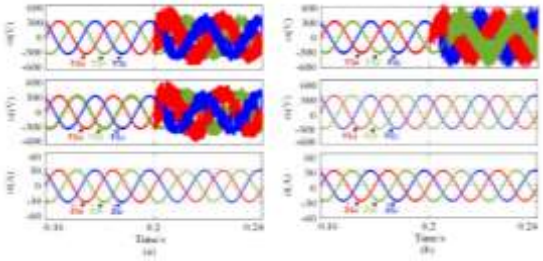


Figure 19. The simulation waveform under different grid impedance: (a)c-UPQC, (b) D-UPQC.

IV Design and Operation of Multi-UPQC for Distributed Power Quality Improvement

The **Multi-UPQC (Unified Power Quality Conditioner)** is an integrated system designed to address a wide range of power quality issues in modern electrical distribution systems. It combines multiple UPQC units strategically deployed across the network to provide coordinated and enhanced compensation for voltage sags, swells, interruptions, and harmonics. Each UPQC unit in the system consists of two main parts: a **shunt converter** and a **series converter**, both typically implemented using Voltage Source Inverters (VSIs). The **shunt VSI** is responsible for injecting or absorbing reactive power to maintain the current profile and suppress load-side harmonics, while the **series VSI** is used to inject a compensating voltage in series with the supply to maintain constant load voltage under abnormal grid conditions.

To achieve effective control and dynamic response, the **dq0 transformation**

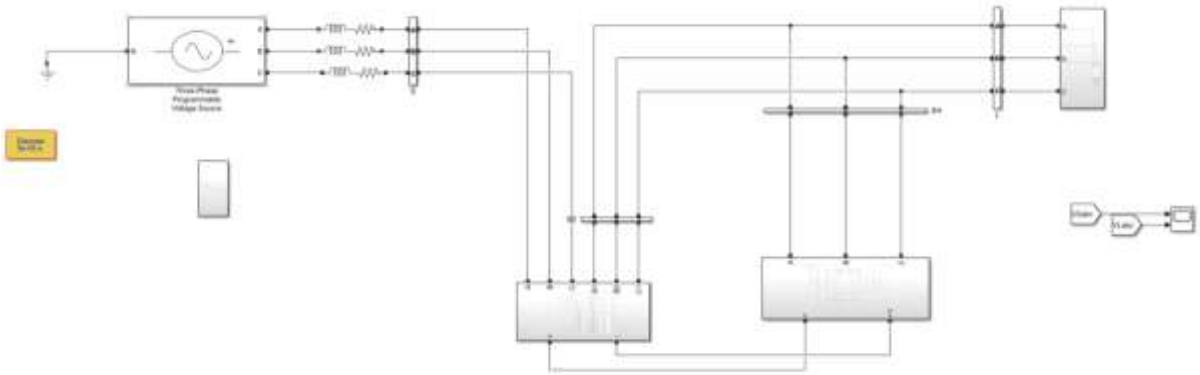


Figure 20. Configuration of three-phase Multi level UPQC

technique is used to convert the three-phase voltages and currents into a synchronous rotating reference frame. This allows for easier separation of the fundamental components from the harmonics and better control under unbalanced conditions. A **Phase-Locked Loop (PLL)** is utilized in each UPQC module to accurately track the phase angle and frequency of the grid voltage, ensuring proper synchronization between the compensating signals and the actual supply.

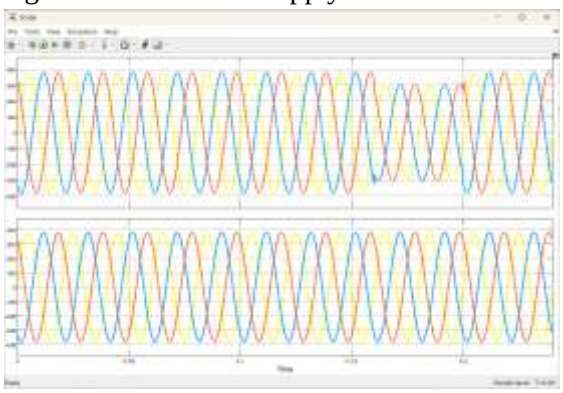


Figure 21: The simulation waveforms under grid voltage sag and swell: Multi upqc

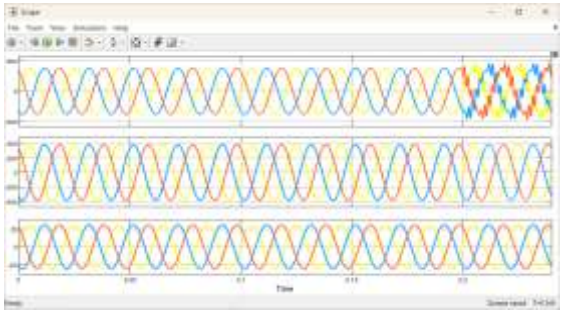


Figure 22: The simulation waveforms under grid voltage harmonics distortion: Multi upqc

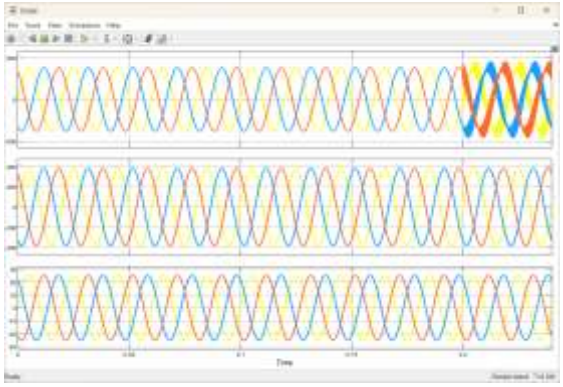


Figure 23. The simulation waveforms under high-frequency grid voltage harmonics distortion: Multi upqc

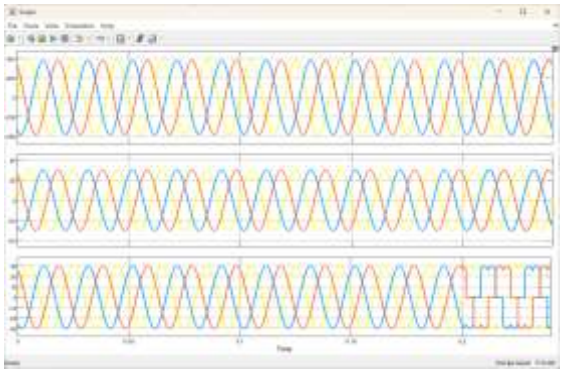


Figure 24. The simulation waveforms under different loads: Multi upqc.

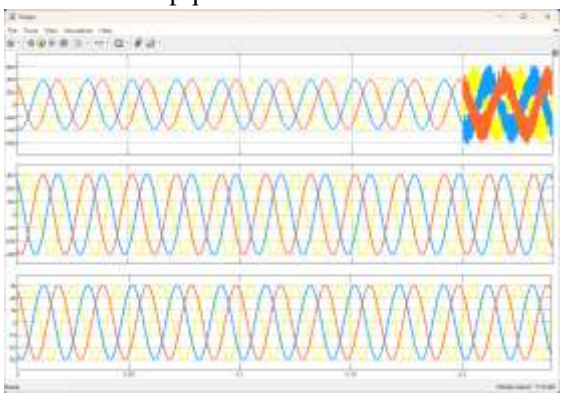


Figure 25. The simulation waveform under different grid impedance: Multi UPQC.

In contrast to conventional single-UPQC systems, the **Multi-UPQC architecture** offers several key advantages. By placing multiple UPQC units at different buses or feeders and interlinking them via communication or coordinated control, the system is able to provide **wide-area compensation**, thereby improving the power quality across an entire distribution segment rather than just at a single point of common coupling (PCC). This not only enhances the effectiveness of voltage compensation during sags or swells but also ensures that harmonic distortions and unbalanced loads are effectively addressed throughout the network. The cooperation between multiple units leads to better utilization of compensating resources, increased redundancy, and more robust protection against faults and voltage disturbances.

When comparing with **Conventional UPQC (C-UPQC)** and **Dual UPQC (D-UPQC)**, the Multi-UPQC exhibits significantly improved performance. The C-UPQC is generally simpler in design but suffers from limited effectiveness in dynamic and unbalanced scenarios, particularly under variable grid impedance. The D-UPQC improves upon this with better dynamic voltage compensation and faster response, especially under sudden load or grid changes. However, both are localized in their compensation range. The Multi-UPQC, on the other hand, extends this capability to multiple points in the network, making it more suitable for modern **distributed generation systems**, **renewable energy grids**, and **critical load applications** where continuous voltage regulation and power quality are essential.

In simulation and experimental validations, the Multi-UPQC has demonstrated a strong ability to maintain voltage levels within acceptable limits during severe disturbances, such as single-phase and three-phase voltage sags, swells, and even short interruptions. It effectively reduces the Total Harmonic Distortion (THD) and balances the voltage profile across the system. The system's scalability and coordination make it highly beneficial for future smart grid applications where demand-side management and distributed energy resources require precise voltage and power quality control. Thus, the Multi-UPQC represents a significant advancement in power quality technology, combining high performance, flexibility, and network-wide protection capabilities without relying on complex controllers or artificial intelligence-based strategies.

Conclusion

The Multi-UPQC system presents a comprehensive and scalable solution for improving power quality in modern electrical distribution networks. Unlike conventional UPQC configurations, the Multi-UPQC offers wide-area compensation by deploying multiple units across the system, ensuring enhanced voltage regulation, harmonic mitigation, and fault tolerance. By utilizing dq0 transformation and PLL-based synchronization, it effectively handles grid disturbances such as sags, swells, harmonics, and impedance variations. Simulation results confirm its superior dynamic response and reliability under diverse operating conditions. Without relying on complex control algorithms or intelligent systems, the Multi-UPQC proves to be a robust, efficient, and adaptable approach suitable for smart grid and renewable-integrated power systems.

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