

# Advanced Multilevel Inverter Design for Grid-Tied PV Systems

### Mr. G. Reshwanth <sup>1</sup>, Mr. K. Sai kumar <sup>2</sup>, Mr. P. Gopi<sup>3,</sup> Mr. R. Balu<sup>4</sup>

<sup>1</sup>Department of Electrical and Electronics Engineering, School of Engineering, Anurag University, Hyderabad <sup>2</sup>Department of Electrical and Electronics Engineering, School of Engineering, Anurag University, Hyderabad <sup>3</sup>Department of Electrical and Electronics Engineering, School of Engineering, Anurag University, Hyderabad <sup>4</sup>Department of Electrical and Electronics Engineering, School of Engineering, Anurag University, Hyderabad

Abstract - Power Renewable energy sources (RES) have gained significant importance in recent decades due to their sustainability, zero emissions, and ease of deployment. Among various RES technologies, photovoltaic (PV) systems are widely utilized owing to their lightweight design, environmental friendliness, and straightforward installation. PV cells generate inherently direct current (DC)electricity, necessitating a suitable power conversion system to transform DC into alternating current (AC) before integration into the power grid. Multilevel inverters (MLIs) are commonly employed for DC-AC conversion in grid-connected renewable energy systems. However, conventional MLI topologies present several limitations. For instance, diode-clamped MLIs require additional diodes alongside active switches, flying capacitor MLIs demand extra and exhibit complex capacitors control challenges as the voltage levels increase, and cascaded H-bridge MLIs necessitate multiple isolated DC sources, restricting their practical application. This paper introduces a novel multilevel inverter topology that achieves DC-AC conversion with a reduced switch count compared to conventional MLIs. The proposed inverter is designed to facilitate seamless PV system integration into the grid while ensuring compliance with key grid parameters such as synchronization, phase angle frequency stability, and voltage amplitude matching. To validate the effectiveness of the proposed topology, seven-level and thirteen-level inverter configurations are modelled and simulated in the MATLAB/Simulink environment, with comprehensive results presented in this study.

*Key Words*: Grid Integration, Photovoltaic (PV) System, Multilevel Inverter (MLI), Renewable Energy Sources (RES).

\_\_\_\_\_

### **1.INTRODUCTION**

Renewable energy sources (RES) have emerged as viable alternatives to conventional fossilbased energy sources such as coal, oil, and natural gas, which are finite and subject to depletion [1]. Various RES technologies exist, including solar. wind, biomass, hydro, geothermal, and ocean energy [2]. Among them, photovoltaic (PV) systems have gained significant attention due to their clean and sustainable nature, as well as their minimal environmental impact [3]. The fundamental component of a PV system is the solar cell, which directly converts sunlight into electrical energy in the form of direct current (DC) [4]. A typical PV cell consists of a p-n junction semiconductor, similar in structure to a diode, as depicted in Figure 1 [5]. Efficient grid integration of PV-generated low-voltage DC requires an appropriate power conversion system to transform it into alternating current (AC) [6]. Traditional H-bridge inverters produce a square wave output that contains an infinite series of odd harmonics, resulting in high dv/dt stress [7]. While conventional pulse-width modulation (PWM) inverters help reduce total harmonic distortion (THD), they suffer from high switching losses and are primarily restricted to low-power applications [8]. In recent decades, multilevel inverters (MLIs) have gained prominence due to their ability to synthesize high-quality AC waveforms with lower harmonic distortion, making them ideal

Τ



for high-power and high-voltage applications [9].

MLIs are broadly categorized into three main types:

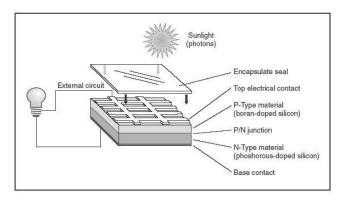


Fig. 1. Basic Structure of a Solar cell

**Diode-Clamped MLIs** – These require a large number of clamping diodes as voltage levels increase, leading to circuit complexity [10].

**Flying Capacitor MLIs** – These offer better voltage balancing but suffer from poor switching utilization, reduced efficiency, and an increased number of capacitors, resulting in higher costs and complexity [11].

**Cascaded H-Bridge MLIs** – These are widely adopted in high-power applications due to their simplified DC bus regulation; however, they necessitate multiple isolated DC sources, and their structural complexity increases significantly with higher voltage levels [12].

# 2. Proposed System Modeling

The layout of the proposed multilevel inverter is shown in Figure 2.

The system comprises a single H-bridge inverter and 'N' cascaded cells, each with a DC rating of Vdc. The total number of levels is determined by the formula:

## Number of Levels = [0 (0+1) +1]

where n represents the number of cascaded cells, excluding the H-bridge. To generate +Vdc, switches S1 and S2 must be turned on. For -Vdc, switches S3 and S4 should be activated. To achieve zero voltage, either S1 and S3 or S2 and S4 must be switched on.

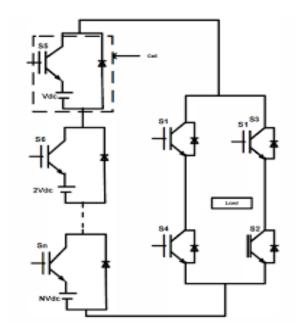


Fig.2. General Structure of Proposed new Multilevel Inverter

## Seven Level Proposed Multilevel Inverter :

The proposed seven-level inverter utilizes only six switches, whereas the cascaded H-bridge inverter requires ten switches and three separate DC sources. However, in the proposed inverter, only two separate DC sources are needed, resulting in lower switching losses. By employing an appropriate switching sequence, the proposed circuit generates seven levels in the output voltage [7].

Table I: Switching Sequence for the Proposed Seven-Level Multilevel Inverter

SW 1	SW2	SW3	SW4	SW5	SW6	Load Voltage
ON	ON	OFF	OFF	ON	OFF	Vdc
ON	ON	OFF	OFF	OFF	ON	2Vdc
ON	ON	OFF	ON	ON	ON	3Vdc
OFF	ON	OFF	ON	OFF	OFF	0
OFF	OFF	ON	ON	ON	OFF	-Vdc
OFF	OFF	ON	ON	OFF	ON	-2Vdc
OFF	OFF	ON	ON	ON	ON	-3Vdc



Table I presents the switching sequence used to produce seven distinct output voltage levels:  $\pm 3$ Vdc,  $\pm 2$ Vdc,  $\pm$ Vdc, and 0. The circuit diagram of the proposed sevenlevel multilevel inverter is illustrated in Figure 3.

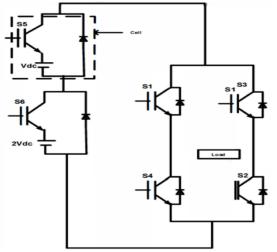


FIG .3.Circuit Diagram of seven level Propose Inverter

To achieve seven levels, the inverter incorporates two cells, consisting of two switches and two diodes, in addition to a single H-bridge. The ideal output voltage waveform for the seven-level inverter is depicted in Figure 4.

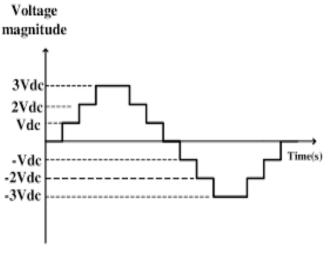


FIG.4. Ideal Seven Level Output Voltage Waveform

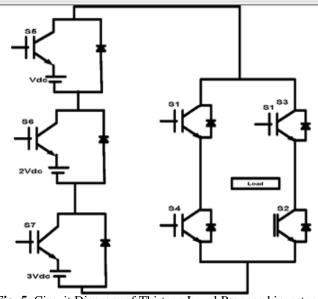
# Thirteen Level Proposed Multilevel Inverter

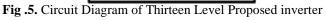
The proposed thirteen-level inverter requires only seven switches, significantly reducing the component count compared to the cascaded H-bridge inverter, which utilizes twenty-four switches and six separate DC sources. In contrast, the proposed inverter operates with just three separate DC sources, resulting in lower switching losses. By employing an optimized switching sequence, the circuit effectively generates seven levels in the output voltage. Table II illustrates the switching sequence used to achieve thirteen levels in the output voltage.

Table I: Switching Sequence for the Proposed thirteen-
Level Multilevel Inverter

Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	V
							Load
On	On	Off	Off	On	On	On	6Vdc
On	On	Off	Off	Off	On	On	5 Vdc
On	On	Off	On	On	Off	On	4 Vdc
On	On	Off	Off	Off	Off	On	3 Vdc
On	On	Off	Off	Off	On	Off	2 Vdc
On	On	Off	Off	On	Off	Off	Vdc
Off	On	Off	On	Off	Off	Off	0
Off	Off	On	On	On	Off	Off	- Vdc
Off	Off	On	On	Off	On	Off	-2
							Vdc
Off	Off	On	On	Off	Off	On	-3
							Vdc
Off	Off	On	On	On	Off	On	-4
							Vdc
Off	Off	On	On	Off	On	On	-5
							Vdc
Off	off	On	On	On	On	On	-6
							Vdc

Circuit diagram of proposed thirteen level multilevel in inverter is shown in figure 5.







Volume: 09 Issue: 04 | April - 2025

SJIF Rating: 8.586

ISSN: 2582-3930

The output waveform has 13 levels:  $\pm$  6Vdc,  $\pm$  5Vdc,  $\pm$  4Vdc $\pm$  3Vdc,  $\pm$  2Vdc,  $\pm$  Vdc and 0.The output voltage waveform of the ideal thirteen level inverter is shown in fig6.

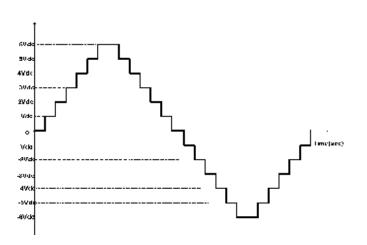


FIG .6. Ideal Thirteen Level Output Voltage Waveform

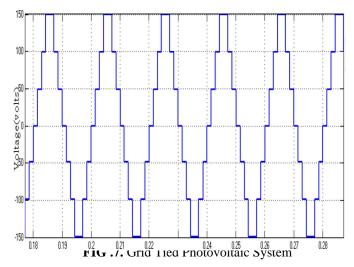
Table III presents a comparison between the proposed multilevel inverter (MLI) and conventional multilevel inverters, highlighting the advantages of the proposed design.

#### TABLE III: COMPARISON BETWEEN DIFFERENT TOPOLOGIES

TOPOLOGY	NUMBER OF SWITCHES FOR 7 -LEVEL	NUMBER OF SWITCHES FOR 13-LEVEL
DIODE CLAMPED MLI	12	24
FLYING CAPACITOR MLI	12	24
CASCADED H- BRIDGE MLI	12	24
PROPOSED MLI	6	7

### Grid-Connected Photovoltaic (PV) System

The block diagram of the proposed grid-connected PV system is shown in Figure 7. It comprises a photovoltaic (PV) system and a proposed multilevel inverter, which facilitates the interface with the grid.



As depicted in Figure 7, the PV cell directly converts solar energy into electrical power in the form of DC [8]. The obtained DC voltage is then converted into AC using the proposed inverter. Finally, the inverter is connected to the power grid while ensuring compliance with grid requirements, including phase angle, frequency, and amplitude of the grid voltage.

#### **Simulation Outcomes**

The following Figures 8 and 9 illustrate the MATLAB/Simulink diagram of the proposed sevenlevel MLI and its corresponding output voltage waveform.

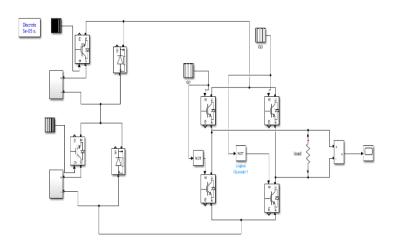
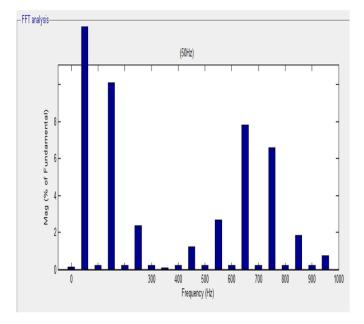


FIG.8 MATLAB/Simulink Diagram of the Proposed Seven-Level MLT





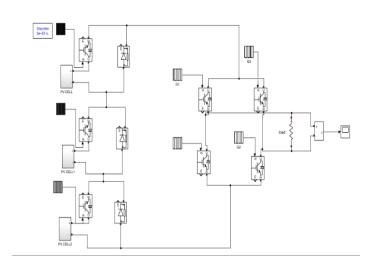


FIG.11 MATLAB/Simulink Diagram of the Proposed Thirteen-Level MLT

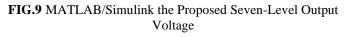
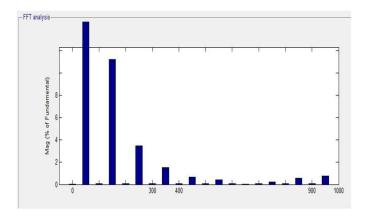


Figure 9 shows that the proposed MLT produces a seven-level output voltage using six switches and two diodes. Figure 10 presents the spectrum analysis of this seven-level output voltage.



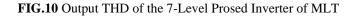
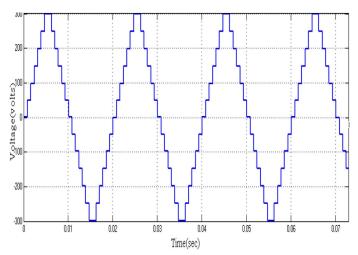


Figure 10 indicates that the Total Harmonic Distortion (THD) of the proposed seven-level inverter is 17.22%. Figures 11 and 12 display the MATLAB/Simulink diagram of the proposed thirteen-level MLI and its corresponding output voltage waveform.



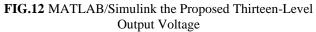


Figure 12 illustrates that the proposed MLI generates a thirteen-level output voltage using seven switches and three diodes. Figure 13 presents the spectrum analysis of the seven-level output voltage.

#### **3. CONCLUSIONS**

This paper introduces a grid-connected PV system utilizing a novel multilevel inverter with a reduced number of switches. By minimizing the number of switches, the proposed inverter lowers switching losses and overall cost compared to conventional MLIs. Increasing the number of output voltage levels helps reduce lower-order harmonics and total harmonic distortion (THD). Eliminating lower-order harmonics is desirable, as filtering them is challenging. The results show that the grid voltage and grid-connected current remain in phase with each other.



#### ACKNOWLEDGEMENT

We extend our sincere gratitude to our mentors and faculty members for their valuable insights and guidance throughout this research. We also thank our peers for their support and collaborative efforts in testing and improving the system.

#### REFERENCES

[1] H. Abu-Rub, M. Malinowski, and K. Al-Haddad, *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*, John Wiley & Sons, 2014.

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, 2002.

[3] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. Prats, "The age of multilevel converters," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28-39, 2008.

[4] F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509-517, 1996.

[5] S. Khomfoi and L. M. Tolbert, "Multilevel power converters," in *Power Electronics Handbook*, 2nd ed., M. H. Rashid, Ed., Butterworth-Heinemann, 2007, pp. 451-482.

[6] B. Wu, *High-Power Converters and AC Drives*, John Wiley & Sons, 2006.

[7] K. Hasegawa and H. Akagi, "Low-modulation-index operation of a five-level diode-clamped PWM inverter with a DC-voltage-balancing circuit for a motor drive," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3495-3505, 2012.

[8] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197-2206, 2010.

[9] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A complete solution to the harmonic elimination

problem," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 491-499, 2004.

[10] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 809-815, 2002.

[11] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1628-1636, 2009.

[12] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4-17, 2015.

L