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ADVANCEMENT IN NANOSCALE ELECTRONICS IN MOSFET

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Abstract —

This research explores a novel approach for designing Cylindrical Surrounding Double-Gate (CSDG) MOSFETs with nanometer-scale precision through a layer-by-layer fabrication technique. Traditional top- down methods, such as photolithography and ion beam deposition, are widely used for semiconductor design but present challenges in creating complex heterostructures. In response, this study proposes an alternative method focusing on cylindrical structures to develop high-resolution morphological designs of CSDG MOSFETsThe research emphasizes the versatility of the proposed method, allowing the design of various cylindricalstructures with distinct properties, including periodic and non-periodic arrangements, symmetric and asymmetric configurations, and nanometer-scale gaps/dots. The focus is on the development of a symmetricCSDG MOSFET concerning the center core, providing valuable insights for fabricating structures over thecore of 2D Electron Gas (2DEG).

Keywords—

Cylindrical Surrounding Double-Gate MOSFET, Fabrication Steps Layer-by-Layer Approach Semiconductor Devices,Nanoscale Electronics ,Transistor Design ,Oxidation Process, Scalability, Simulation ,Oxidant Concentration.

Introduction -

The miniaturization of transistors, the workhorses of modern electronics, has reached a critical juncture. Aswe push the boundaries of Moore's Law, conventional planar MOSFETs face limitations such as short- channel effects (SCEs) and gate leakage currents. To overcome these hurdles and continue the exponentialgrowth of computing power, novel device architectures are urgently needed. Enter the Cylindrical Surrounding Double-Gate MOSFET (CSDG MOSFET). This innovative design boasts a unique cylindricalstructure with two concentric gates enveloping a central channel. This configuration offers several advantages over traditional planar MOSFETs: Enhanced

gate control: The surrounding gates provide superior electrostatic control over the channel, leading to improved subthreshold swing and reduced SCEs. Reduced gate leakage: The larger physical separation between the gates and the channel minimizes leakagecurrent, a major concern in scaled devices. . High-κ dielectric integration: High-κ dielectric materials can bereadily incorporated between the gates and the spacer, further suppressing leakage and improving device performance. However, fabricating such complex three-dimensional structures presents a significant challenge. : The layer-by-layer build ensures perfect alignment and concentricity of the cylindrical gates, crucial for optimal device performance. Scalability: This approach is inherently scalable, paving the way for future miniaturization and integration of CSDG MOSFETs in complex circuits.

DEVELOPMENT OF CYLINDRICAL DESIGN

In recentyears, lithographic methods have played a pivotal role in patterning semiconductor materials for MOSFETs, facilitating the transition from micrometer to nanometer regimes with enhanced performance. This advancement is crucial for designing transistors employed in electronic gadgets and mobile phones. Silicon wafers are patterned to accommodate various components, emphasizing the utility of nanophotonics in creating circuits with optoelectrical properties. While Silicon remains a dominant material, there's a growing exploration of arbitrary alloys to overcome its limitations. Chemical growth methods, cost-effective alternatives to lithography, are gaining prominence, demonstrating potential in device design. Researchers have utilized innovative methods, including rapid depressurized Gold (Au) deposition and Gallium Phosphide – Gallium Arsenide compounds, showcasing possibilities for constructing CSDG MOSFETs with arbitrary alloys. These findings represent significant progress in semiconductor technology, providing avenues for designing advanced devices with improved characteristics and novel structures. Thetext discusses the use of arbitrary semiconductor alloys in novel cylindrical structure designs for low RF (Radio Frequency) design, enhancing selectivity in removing GaAs segments

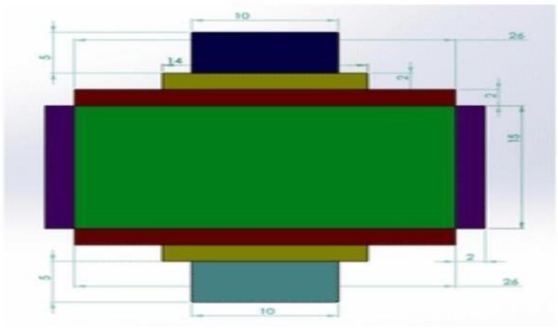


Fig:2-D structure of CSDG mosfet

In this intricate process, specific attention is given to the introduction of a high-dielectric material positioned strategically between the spacer and the gate terminals.The selected high-dielectric material serves a crucial purpose in enhancing the overall performance of the CSDG MOSFET. Placed between the spacer and gate terminals, this material acts as a vital component influencing the electrical properties of the device. Its introduction aims to improve the efficiency of electron buildup within the channel, a fundamental aspect of MOSFET operation. Additionally, this material plays a key role in facilitating the distribution of charge carriers, contributing to the overall functionality of the device. Particular emphasis is placed on the

incorporation of nanomaterial within the spacer. This nanomaterial, chosen with precision, exhibits favorable electrical properties that positively impact the performance of the electron buildup within the channel. The careful selection of nanomaterial aims to harness its unique characteristics for optimal device functionality.

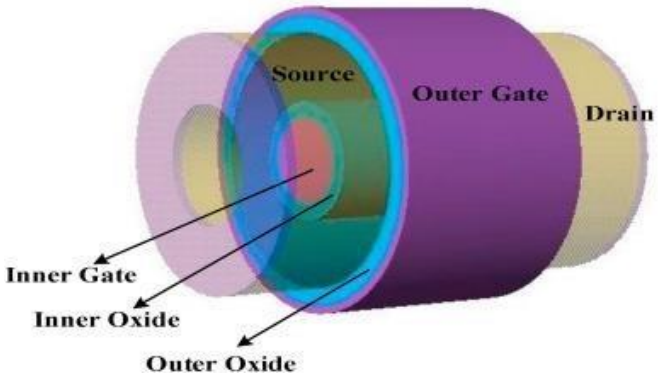


Fig:CSDG mosfet

The analysis of this electron buildup provides valuable insights into the performance and efficiency of the Optional outcomes .The platform chosen for the fabrication process incorporates bottom concentric rings within the chamber. The use of concentric rings of varying diameters introduces a layered structure, allowing for a systematic and controlled growth process.The fabrication process unfolds with the creation of the first layer, known as the core. This initial layer is carefully designed and undergoes an etching process to ensure a uniform deposition of materials. Etching is a crucial step in achieving precision and uniformityin the layering process, paving the way for subsequent layers to be added systematically.

Fabricating a Cylindrical Surrounding Double-Gate (CSDG) MOSFET involves a series of complex steps, including material selection, lithography, deposition, and etching. Below is a generalized overview of the fabrication steps for a CSDG MOSFET:

Material selection:

Choose a suitable semiconductor material for the MOSFET. Consider the electrical and thermalproperties, as well as the specific requirements of the application.

Substrate Preparation:

prepare a semiconductor substrate, commonly made of Silicon, by cleaning and treating the surface to ensure optimal adhesion of subsequent layers.

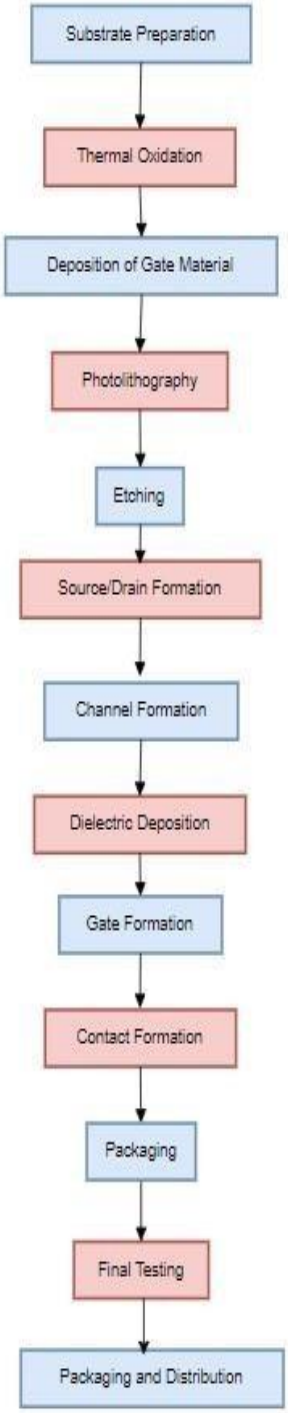
Gate Oxide Formation:

The gate oxide serves as an insulating layer between the gates and the semiconductor substrate.Grow a thin layer of gate oxide on the substrate using thermal oxidation or chemical vapor deposition (CVD).

Lithography:

Use lithography techniques to define the patterns on the substrate. This involves coating the substrate with a photoresist, exposing it to light through a mask, and developing the pattern.In photolithography, a photoresist material is applied to the substrate (usually a silicon wafer).

FABRICATION VISION OF THE CSDG MOSFET



Testing and Characterization:

After fabrication, perform comprehensive testing and characterization of the CSDG MOSFET device to ensure it meets the desired specifications and performance criteria.

Packaging:

Finally, package the CSDG MOSFET device to protect it from external influences and facilitate connection to external circuits

Improved Control Over the Channel:

The CSDG MOSFET's unique double-gate structure provides enhanced electrostatic control over the channel. This enables better modulation of the current flow, leading to improved performance in terms of speed and power consumption.

Reduced Subthreshold Swing:

CSDG MOSFETs can achieve a lower subthreshold swing compared to traditional MOSFETs. A lower subthresholdswing is critical for applications requiring low-power operation, such as in mobile devices and IoT sensors.

Enhanced Scaling and Miniaturization:

The CSDG MOSFET design is particularly advantageous for scaling down semiconductor devices to smaller nodes. Its structure allows for better scalability without significant degradation in performance, addressing challenges associated with miniaturization.

Low Leakage Current:

The improved gate control in CSDG MOSFETs helps reduce leakage current, making them suitable for applications where minimizing power consumption is essential, such as in battery-operated devices.Advanced Memory and Logic Applications:

CSDG MOSFETs are well-suited for advanced memory technologies and logic applications, where precisecontrol over the transistor behavior is crucial. This makes them valuable for the development of next- generation memory devices and performance processors.

High Performance in High-Frequency Applications:

The enhanced control over the channel and reduced parasitic capacitance make CSDG MOSFETs suitablefor high-frequency applications, such as in communication systems and high-speed data processing.

Potential for Neuromorphic Computing:

The unique characteristics of CSDG MOSFETs make them promising candidates for neuromorphic computing, a field that aims to mimic the structure and functionality of the human brain. The precise control over the transistor behavior aligns with the requirements of neuromorphic systems.

Innovation in Semiconductor Technology:

The development and adoption of CSDG MOSFETs contribute to the ongoing innovation in semiconductor technology. As traditional transistor designs face challenges at smaller scales, novel designs like CSDG MOSFETs pave the way for advancements in electronics.

Energy-Efficient Electronics:

Due to their improved control and reduced power consumption, CSDG MOSFETs have the potential to contribute to the development of energy-efficient electronic devices, supporting sustainability goals and reducing the environmental impact of electronics.

Exploration of Emerging Technologies:

CSDG MOSFETs open up possibilities for exploring and integrating with emerging technologies such asquantum computing and other advanced computing paradigms. Their unique structure may find applicationsin these cutting-edge areas. the importance of CSDG MOSFETs lies in their ability to overcome challenges associated with traditional transistor designs, offering improved control, reduced power consumption, and enhanced performance in a variety of applications

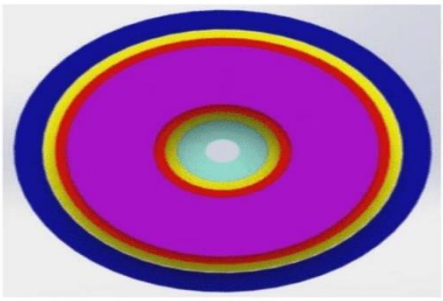


fig: side view of csdg mosfet

Silicon Substrate:

Color: Light or medium gray.

Gate Material (Polysilicon or Metal):

Color: Darker shade of gray, black, or a color distinct from the substrate (e.g., brown).

Gate Oxide Layer:

Color: Blue, green, or another color distinct from the substrate and gate material.

Cylindrical Surrounding Structure (Concentric Layers):

Different layers may be represented using different shades of a single color (e.g., different shades of blueor green) or using different colors altogether

Interlayer Dielectric (ILD):

Color: Another distinct color or pattern to indicate insulation between layer.

High-k Dielectric Material:

Color: Blue or green.

Outer Gate Material:

Color: Light gray or a contrasting color.

Inner Gate Material:

Color: Dark gray or black

In nanoscale diagrams, color coding is often used to distinguish different materials for visual clarity. Whilethere is no strict universal standard, and color conventions may vary, here's a conceptual suggestion for color coding in a diagram representing a Cylindrical Surrounding Double-Gate (CSDG) MOSFET at the nanoscale:

The Cylindrical Surrounding Double Gate MOSFET (CSDG MOSFET) and the conventional MOSFET (Metal-OxideS emiconductor Field-Effect Transistor) are both types of transistors, but they differ in their structure and characteristics. Here's a brief comparison:

Structure:

MOSFET: Typically has a planar structure with a single gate.

CSDG MOSFET: Features a cylindrical structure with double gates surrounding the channel.

Gate Control:

MOSFET: Controlled by a single gate.

CSDG MOSFET: Controlled by two gates, one on the inner surface and one on the outer surface of the cylindrical channel.

Channel Control:

MOSFET: Controls the channel by applying a voltage to the gate, influencing the flow of current.

CSDG MOSFET: The dual gates in a cylindrical configuration provide enhanced control over the channel, potentially offering improved performance in terms of speed, power consumption, and leakage current.

Benefits of CSDG MOSFET:

Potential for Improved Performance: The cylindrical structure may offer advantages such as betterelectrostatic control, reduced short-channel effects, and enhanced scalability.

Applications:

MOSFET: Widely used in various electronic devices and integrated circuits.

CSDG MOSFET: Primarily designed to address some of the limitations of traditional MOSFETs, potentiallyleading to improved performance in similar applications.

Challenges:

MOSFET: Well-established and widely used, but faces challenges related to scaling down to smaller sizes.

CSDG MOSFET: While promising, it may face challenges in terms of fabrication complexity and integration into existing semiconductor manufacturing processes.

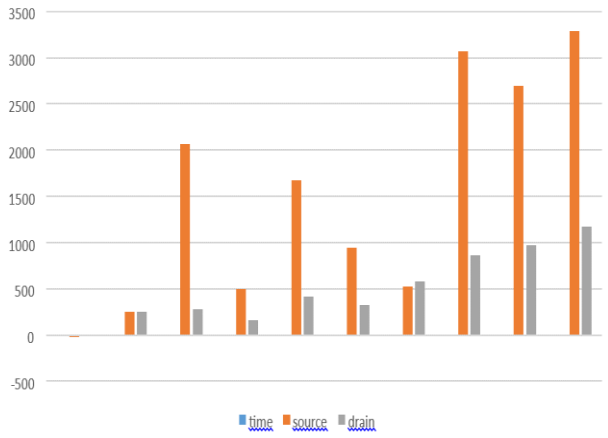


Fig:Source-Drain Electron Accumulation Contrast

The diagram presents simulation outcomes for the CSDG MOSFET, emphasizing the duration forelectron accumulation from source to drain along the channel. Electron buildup time is pivotal for device observability and control. Initially, during biasing, the source terminal lacks over time, the drain terminal accumulates enough to control the device, as depicted.The simulation of Cylindrical Surrounding Double- Gate (CSDG) MOSFETs provides crucial insights into device characteristics. The variation in dopant concentrations and diffusion is essential for achieving uniformity in the device structure. The utilization ofa combined Deal-Grove and Massoud oxidation model is noteworthy, contributing to enhanced surface oxidation and defect reduction. The observed variations in maximum oxidant concentrations based on orientations and oxidation modes underscore the nuanced effects of the fabrication process. The simulation,spanning 600 minutes, demonstrates optimal oxidation effects and rates, emphasizing scalability and uniform device performance. Designing a CMOS inverter using Cadence tools involves a systematic process within the Cadence design suite. Initially, the schematic of the CMOS inverter is created using the Cadence schematic editor, configuring NMOS and PMOS transistors appropriately.

Cadence" typically refers to Cadence Design Systems, a company that provides electronic design automation (EDA) software, hardware, and services. Cadence tools are widely used in the semiconductor industry for designing integrated circuits (ICs), printed circuit boards (PCBs), and other electronic systems. Cadence offers a range of tools and solutions to support various stages of the design and verification process.

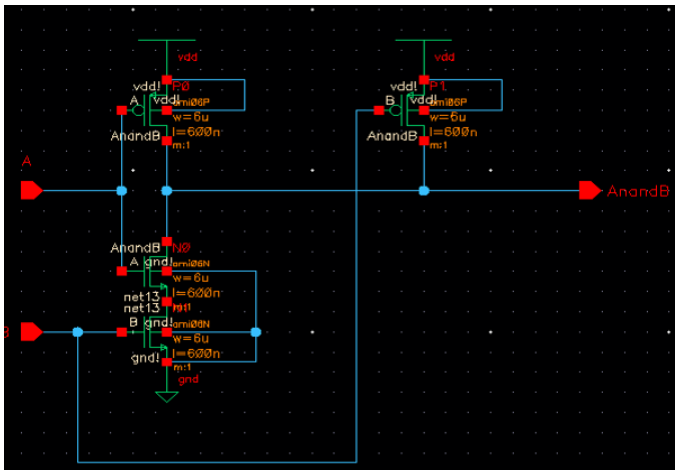


Fig:schematic of cmos

Subsequently, simulations using tools like Spectre or HSPICE help analyze the inverter's behavior under diverse conditions. The design is then translated into a physical layout using Cadence layout tools, placing transistors and establishing connections based on the schematic. Extraction of parasitic elements is critical for accurate simulation. Post-layout simulations validate the circuit's performance considering the physical layout.

Verification against specifications, design rule checks, and layout versus schematic comparisons ensure the design meets requirements. Finally, the design is prepared for fabrication through tape-out, involving the generation of files for the semiconductor foundry. This comprehensive process ensures the successful design and realization of a CMOS inverter with optimal performance characteristics.

Creating a schematic of a CMOS Complementary MetalOxideSemiconductor circuit using Cadence tools involves several steps. Below, I'll provide a simplified guide using the Virtuoso tool from Cadence. Keep in mind that the actual process may vary based on the specific version of the Cadence tools you're using.

Open the Cadence Virtuoso Design Environment.Create a new library where you will store your CMOS schematic.Open the Schematic Composer within Virtuoso.

Place NMOS and PMOS transistors on the schematic canvas. Use the 'Add Instance' or a similar option to add components.

Connect the transistors to create the desired CMOS circuit configuration.Add power supplies (Vdd and Gnd) to your schematic.

Cmos applications:

Microprocessors and Microcontrollers:

CMOS technology is extensively used in the fabrication of microprocessors and microcontrollers, serving as the core processing unit in computers, embedded systems, and other digital devices.

Memory Devices:

CMOS is employed in the design of various types of memory, including static random-access memory (SRAM) and dynamic random-access memory (DRAM). CMOS-based memory is widely used in computers and other electronic systems.

Digital Integrated Circuits:

CMOS is the dominant technology for the implementation of digital integrated circuits, such as logic gates, flip-flops, and other digital building blocks. These circuits are fundamental to the operation of digital systems.

Analog Integrated Circuits:

CMOS technology is also used for analog and mixed-signal integrated circuits, including operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and voltage regulators.

Image Sensors:

CMOS image sensors are widely used in cameras, smartphones, webcams, and other imaging devices. They offer advantages such as low power consumption and integration of additional functions on the same chip.

Radio-Frequency (RF) Circuits:

CMOS technology is increasingly used in RF circuits for wireless communication applications. RF CMOS circuits are found in devices such as mobile phones, Wi-Fi modules, and Bluetooth devices.

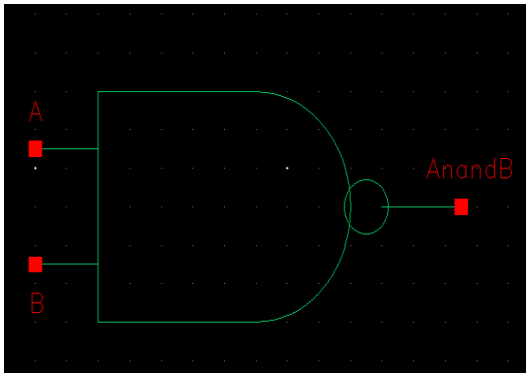


Fig:symbol of nanad gate

Designing the symbol for a NAND gate in Cadence involves utilizing the schematic editor within the tool. Firstly, a new schematic cell is created, serving as the canvas for the NAND gate representation. Symbols for NMOS and PMOS transistors are then strategically placed to reflect the internal logic of a NAND gate. Precise connections between these transistors are established to mirror the gate's logic. Inputs and outputs are appropriately labeled to signify the function of the NAND gate. Once the schematic is crafted, it is saved, compiled, and integrated into the desired library. The final symbol, encapsulating the NAND gate's logical structure, is now ready for use in larger digital designs. This process ensures the accurate and efficient incorporation of a NAND gate into Cadence-based circuit designs.Using a NAND gate symbol in Cadence Virtuoso involves placing the symbol in your schematic and connecting it to other components as needed. Here's a step-by-step guide:Launch the Cadence Virtuoso Design Environment.

Create a new schematic or open an existing one where you want to use the NAND gate.In the schematic editor, locate the library that contains the NAND gate symbol. This could be a library where you created the symbol or a pre-existing library.Use the "Place > Instance" or a similar option to place the NAND gate symbol onto your schematic.Connect the input and output pins of the NAND gate to other components in your circuit.Use the wire tool to draw connections between the pins of the NAND gate symbol and other components in your schematic.If the inputs and outputs of your NAND gate symbol are not labeled, use the "Label" or "Net Name" tools to add labels for clarity.Verify that all connections are correct by visually inspecting the schematic.

Ensure that the NAND gate is properly integrated into your circuit.If you want to simulate your circuit, you can use tools like Spectre. Set up simulation parameters and run a simulation to verify the functionality of your circuit.

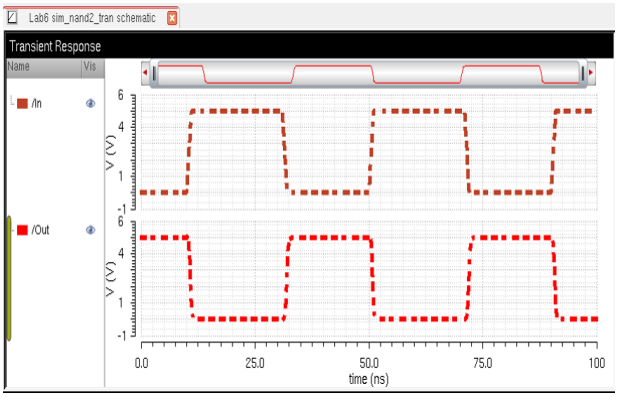


Fig: output waveform of cmos

The output waveform of a CMOS inverter provides insight into its dynamic behavior during different logic transitions. As the input signal transitions from low to high (logic 0 to 1), the NMOS transistor turns on, connecting the output to ground and allowing the output voltage to drop rapidly. Conversely, during a high to low transition (logic 1 to 0), the PMOS transistor turns on, connecting the output to the supply voltage and causing the output

voltage to rise swiftly. This transition behavior results in a characteristic square wave output. However, due to the finite rise and fall times and propagation delays inherent in physical systems, the output waveform may exhibit slight distortions, such as rise and fall time delays or voltage overshoot. Understanding and analyzing these characteristics is crucial for optimizing circuit performance and ensuring reliable digital signal processing in CMOS inverter-based Design. The output of a CMOS (Complementary Metal-Oxide-Semiconductor) circuit depends on its specific configuration and the input signals applied to it. CMOS circuits are commonly used in digital logic design for implementing various functions, such as logic gates, flip-flops, and other digital building blocks.Here's a general explanation of what the output of a CMOS circuit might represent based on its functionality:In the case of logic gates (e.g., AND, OR, NAND, NOR), the output typically represents the result of the logical operation performed on the input signals.For example, in a 2-input NAND gate, the output is high (logical 1) unless both inputs are high, in which case the output is low (logical 0).

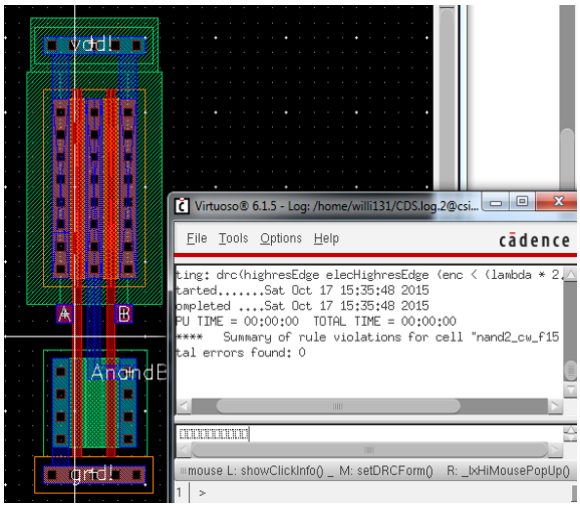


Fig:drc of cmos

Design Rule Checking (DRC) is a crucial step in the CMOS (Complementary Metal-Oxide-Semiconductor) fabrication process, ensuring that the layout adheres to the manufacturing rules and specifications. The DRC process involves several key steps. Initially, it examines the layout for violations against predefined design rules, such as minimum feature sizes, spacing requirements, and metal layer constraints. DRC also verifies that the layout aligns with the technology node's guidelines, helping prevent issues like shorts or open circuits. The tool identifies potential manufacturing problems that could compromise the functionality and reliability of the CMOS circuit. Engineers often run DRC iteratively, refining the layout to address flagged issues until compliance is achieved. Successful DRC ensures that the CMOS layout is manufacturable, minimizing the risk of defects and enhancing the overall yield and performance of the integrated circuit.

Design Rule Checking (DRC) in the context of CMOS (Complementary Metal-Oxide-Semiconductor) technology is a critical step in the integrated circuit (IC) design and manufacturing process. DRC ensures that the layout of the CMOS circuit adheres to the specific rules and constraints set by the fabrication process to ensure proper functionality and manufacturability. Here are some common aspects of DRC for CMOS technology:Ensure proper spacing between adjacent features (e.g., transistors, metal layers) to prevent short circuits.Specify minimum and maximum widths for different layers to ensure proper functionality and manufacturability.Define rules for the overlap between different layers to prevent issues such as leakage currents.Specify minimum and maximum sizes for vias,

which are used to connect different metal layers.Ensure that contacts between different layers are properly sized and aligned for reliable connections.

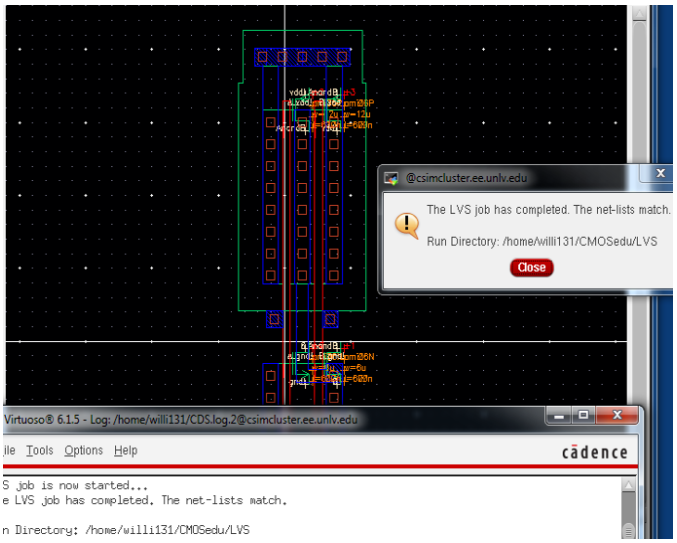


Fig: lvs of cmos

Layout vs. Schematic (LVS) is a critical step in the CMOS (Complementary Metal-Oxide-Semiconductor) design process, ensuring that the physical layout of the circuit matches its schematic representation. LVS involves several key procedures. Initially, it compares the netlist extracted from the layout with the original schematic to detect any discrepancies. This process helps identify issues such as missing or extra connections, ensuring the accuracy of the physical layout. LVS also verifies that the parasitic elements extracted from the layout match the expected values, providing insight into the circuit's performance. Engineers iteratively refine the layout based on LVS results to achieve consistency with the schematic. Successful LVS is paramount for verifying the functionality and correctness of the CMOS circuit layout before moving to the fabrication stage, minimizing the risk of errors and ensuring a successful semiconductor manufacturing process.

CONCLUSION

The Layer-by-Layer Cylindrical Surrounding Double-Gate MOSFET design, coupled with detailed fabrication steps, showcases advancements in semiconductor technology. This research provides a foundation for enhanced device performance and practical applications in the evolving landscape of electronic devices. The study digs into the novel design and manufacture of a Cylindrical Surrounding Double-Gate MOSFET using a Layer-by-Layer Approach, with the goal of improving semiconductor technology. The study delves intocrucial data that indicate significant gains made possible by the suggestedMOSFET architecture. The paper's meticulously documented Layer-by-Layer Approach emerges as a critical component in achieving precision and control throughout manufacture. The simulation of Cylindrical Surrounding Double-Gate (CSDG) MOSFETs provides crucial insights into device characteristics. The variation in dopant concentrations and diffusion is essential for achieving uniformity inthe device structure. The utilization of a combined Deal-Grove and Massoud oxidation model is noteworthy, contributing to enhanced surface oxidation and defect reduction. The observed variations in maximum oxidant concentrations based on orientations and oxidation modes underscore the nuanced effects of the fabrication process. The simulation, spanning 600 minutes, demonstrates optimal oxidation effects and rates, emphasizing scalability and uniform device performance.

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[3PATTUNNARAJAM PARAMASIVAM1 , NAVEENBALAJI GOWTHAMAN 2 , (Senior Member, IEEE), AND VIRANJAY M. SRIVASTAVA 2 , (Senior Member, IEEE) 1Department of Electronics and Communication Engineering, Prince Shri Venkateshwara Padmavathy Engineering College, Chennai 600127, India 2Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban 4041, South Africa

[4] Subthreshold Behavior Models for Nanoscale Short-Channel Junctionless Cylindrical Surrounding-Gate MOSFETs Cong Li, Member, IEEE, Yiqi Zhuang, Member, IEEE, Shaoyan Di, and Ru Han, Member, IEEE