Advances in CMOS Image Sensors and Transistors Leveraging Stochastic Nanomagnets: A Comprehensive Review

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Abstract— **Accurate modeling and assessment of complex Complementary Metal-Oxide Semiconductor (CMOS) imaging sensors and transistors, in conjunction with randomized nanomagnets for distributed computation in radiated environments, are crucial for the development of robust electronic systems. The effectiveness and resilience of these intricate parts to radiation exposure is the subject of this study, which is becoming more and more important in applications including space missions, power plants, and high-altitude flying. To take into account the interaction between CMOS technology and the unpredictable behavior of nanomagnets, a comprehensive durability modeling technique is required. The methodology that has been suggested evaluates the susceptibility of image detectors and transistors to malfunctions caused by radiation, such as dislocation damage, single-event upsets (SEUs), and impacts of total ionizing dose (TID). The impact of radiation on the power characteristics and operational dependability of these components is investigated using state-of-the-art modeling tools and experimental data. The findings suggest that random nanomagnets can improve distributed computing devices' resistance to radiation-induced failures. Through the provision of insights into reliability challenges and solutions for enhanced CMOS image sensors and transistors, this work advances the field of radiation-tolerant technologies. Future electronic device developers will find the suggested reliability modeling and evaluation methodology to be a useful resource for creating reliable devices that can resist harsh radioactive environments.**

Keywords— Reliability Modeling; CMOS Image Sensors; Radiation Environment; Advanced Technology Node; Transistor Structures; Stochastic Nanomagnets; Heterogeneous Computing; Probabilistic Inference

I. INTRODUCTION

Spacecraft navigation and control systems, such as those aboard crewed spacecraft, satellites, and space probes, are increasingly using CMOS sensors [1]. CMOS image sensors, however, are susceptible to radiation damage from high-energy particle hits in harsh space settings. After prolonged operations, radiation damage causes CMOS image sensors to exhibit increased noise, a rise in dark current, and other consequences [2]. Reduced positioning accuracy, decreased dependability, and even CMOS image sensor failures are the results of these events. Moreover, CMOS image sensors' reliability is impacted by uncertainty introduced by manufacturing flaws and changing environmental circumstances [3].

In order to meet new computing difficulties and achieve energy efficiency, there has been a rise in demand for domain-specific hardware and architectures as Moore's Law has slowed down. This demand is especially evident in light of machine learning and artificial intelligence (AI) applications. Creating CMOS + X architectures by combining newly developed nanotechnologies (X) with known complementary metal-oxide semiconductor (CMOS) technology is one workable approach [4].

The main goal of this strategy is to enable the development of science-inspired hardware platforms that accomplish huge parallelism, asynchronous processes, and energy savings in order to augment existing CMOS technology with novel features. Then, these systems can be used to solve a wide range of issues in several domains [5].

A device needs to be extremely efficient and have no operational problems in order to perform as intended and show a high degree of reliability. Present research on the dependability of CMOS image sensors focuses on these two factors [6]. In reference to the first, some researchers concentrate on using design techniques (e.g., using deep-submicron processes, optimizing design parameters, and creating pixel circuit architectures) to maximize the efficiency of CMOS imaging sensors (such as quantum efficiency, full well capacity, dynamic range, signal-to-noise ratio, sensitivity, dark current, noise, and spectral response) [7].

There have been many different p-bit systems presented [8] that use resistive RAM, diffusive memories, perovskite-nickelates, ferroelectric transistors, single-photon avalanche diodes, optically parametric oscillators, and other materials and devices. The intrinsic stochasticity of these materials and electronics is utilized in these applications. Among alternatives, spin-transfer torque magnetic tunnel junctions (sMTJs) made of low-barrier nanomagnets have shown great promise because they can amplify noise by converting millivolt variations to hundreds of millivolts via resistive networks, which is different from previous methods involving amplifiers [9].

The continuous creation of truly random bit streams—which pulse-based designs require to be reset—is another benefit of sMTJ-based p-bits. The promise of low-barrier nanomagnets to create energy-efficient p-bits has spurred increased interest in material and device science [10]. Numerous fascinating demonstrations, from novel concepts for magnetic tunneling junctions to a deeper conceptual understanding of nanomagnet physics, have stoked this curiosity. Additionally, photonic integrated circuits (PICs) provide a great deal of promise for creating small, scalable systems with a wide range of uses, such as communication, computing, metrology, and sensing [11].

The chosen research articles highlight developments in CMOS image sensor technology with an emphasis on specific applications, power economy, and performance. A concept that achieves high-speed imaging with column-parallel ADCs is discussed in the publication "A 1080p High-Speed CMOS Image Sensor With Column-Parallel 10-b Subranging ADCs" (2020). This design improves performance but uses more power. In a similar vein, the 2019 publication "Low-Power CMOS

S. No.	Title	Year	Methodology	Advantage	Limitation
1	A 1080p High-Speed CMOS Image Sensor With Column-Parallel 10-b Subranging ADCs	2020	Column-Parallel ADCs	High-speed imaging	Increased power consumption
2	Low-Power CMOS Image Sensors for Mobile Applications	2019	Subthreshold Operation Technique	Low power consumption	Reduced image quality in low light
3	Scaling CMOS Image Sensors for Better Performance	2021	Advanced Scaling Techniques	Improved performance and integration	Potential for higher noise levels
4	High-Speed CMOS Image Sensors	2022	Parallel Processing Architectures	High frame rate and fast readout	Higher power consumption
5	CMOS Image Sensors with Global Shutter	2020	Global Shutter Implementation	Elimination of motion artifacts	Increased power consumption
6	Advanced Pixel Architectures for CMOS Image Sensors	2021	Innovative Pixel Designs	Enhanced image quality and functionality	Increased complexity and cost
7	Energy-Efficient CMOS Image Sensors	2020	Ultra-Low Power Techniques	Significant energy savings	Potential trade-offs in image quality
8	CMOS Image Sensors with On-Chip Processing	2021	On-Chip Signal Processing	Reduced data bandwidth requirements	Increased design complexity
9	CMOS Image Sensors for Automotive Applications	2022	Robust Design Techniques	High reliability under harsh conditions	Increased design and testing efforts

Table 1: Showing Recent works Image Sensors

Image Sensors for Mobile Applications" investigates subthreshold operation approaches to minimize power consumption, making it appropriate for mobile devices, albeit at the expense of low light image quality.

In order to overcome noise issues and enhance integration and performance, "Scaling CMOS Image Sensors for Better Performance" (2021) presents sophisticated scaling approaches. In "High-Speed CMOS Image Sensors" (2022), parallel processing architectures are examined in order to balance increased power requirements with quick readout and high frame rates. In spite of increased complexity and expense, the study "Advanced Pixel Architectures for CMOS Image Sensors" (2021) offers creative pixel designs for improved image quality and functionality.

Ultra-low power methods are used in "Energy-Efficient CMOS Image Sensors" (2020) to save a substantial amount of energy, albeit there may be image quality trade-offs. On-chip signal processing is integrated in "CMOS Image Sensors with On-Chip Processing" (2021) to lower data bandwidth requirements, albeit at the expense of more complex architecture. Finally, "CMOS Image Sensors for Automotive Applications" (2022) highlights the need for rigorous design methods to achieve high dependability in challenging conditions, albeit a significant amount of design and testing work is required.

Research Gaps

Limited Understanding of Interactions: The interactions between randomized nanodevices and deterministic CMOS circuits are not well understood. Obstacles to Scaling: There are many obstacles to overcome when scaling hybrid CMOS + sMTJ devices to higher concentrations. consequences of Device Diversity: The consequences of device variability in hybrid probabilistic computation systems have not received enough attention.

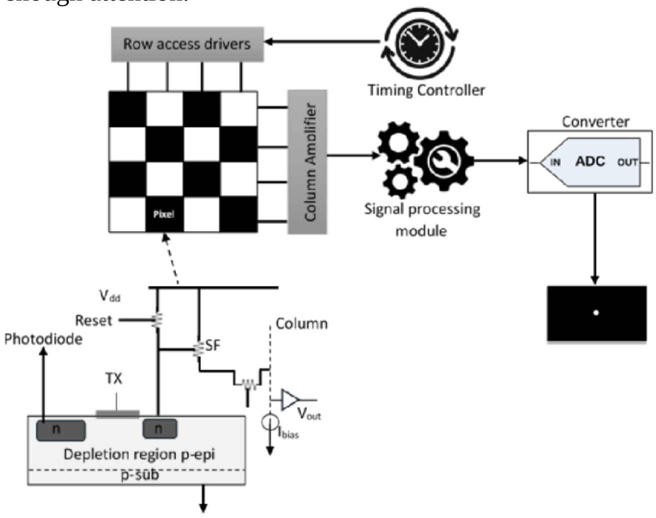

Fig. 1: CMOS image sensor architecture

II. MATERIALS AND METHODS

A. Preleminaries

CMOS-based cameras have been employed in a wide range of applications, including consumer electronics, space exploration, and medical imaging. The function of these sensors can be significantly impacted by radiation, especially in high-radiation environments like spaceflight. Radiation affects on CMOS sensors for images can include single-event impacts, dislocation injury, and Total Ionizing Dose (TID) effects.

Total Ionizing Dose (TID) Effects: TID effects are caused by ionizing radiation building up over time, which causes a charge buildup in the CMOS device's oxide layer. Equation (1) can be used to represent the TID-induced threshold voltage shift (ΔVt): $\Delta Vt = C\ q\ o\ z.\ D\ i\ t$ ΔVt=Cqoz.Dit
where d is the density of radiation-induced interface traps, q is the electronic charge, and C_Oxides is the oxide capacitance per unit area.

Displacement Damage: Atoms are displaced from their lattice places by high-energy particles, resulting in flaws that impair the function of the sensor. Equation (2) provides the displacement damage dose (DDD), which can be measured using the Non-Ionizing Energy Loss (NIEL): dE = ∅. DDD=∅ in this case.NIEL
where NIEL is the non-ionizing energy loss per unit length and ∅ is the particle fluence.
Single-Event Effects (SEEs): SEEs happen when a single high-energy particle permanently damages the CMOS sensor or causes a transitory current to be induced. The linear energy transfer (LET) and the device's sensitive volume can be used to estimate the rate of SEEs. Equation (3) provides the SEE cross-section (σ) as follows: $\sigma = K.(LE\ \ T)\ n$ σ=K.(LET) n

where n is an empirical value, LET is the linear energy transfer, and K is a constant unique to the device.

B. Materials

To conduct a more thorough investigation of CMOS image sensors in radiation-prone settings, multiple materials and technologies are needed. Among them are:

1. Advanced CMOS technological: To comprehend the effects of radiation on the newest technological nodes, make use of cutting-edge CMOS image sensors made utilizing deep-submicron technologies.

2. Radiation Sources: To replicate various space and high-radiation conditions, use a range of radiation sources, such as gamma rays, neutrons, and heavy ions.

3. Stochastic Nanomagnets: To investigate the effects of spin-transfer torque magnetic tunnel junctions (sMTJs) on dependability and probabilistic computation, incorporate them into CMOS circuits.

C. CMOS Amplifier Design

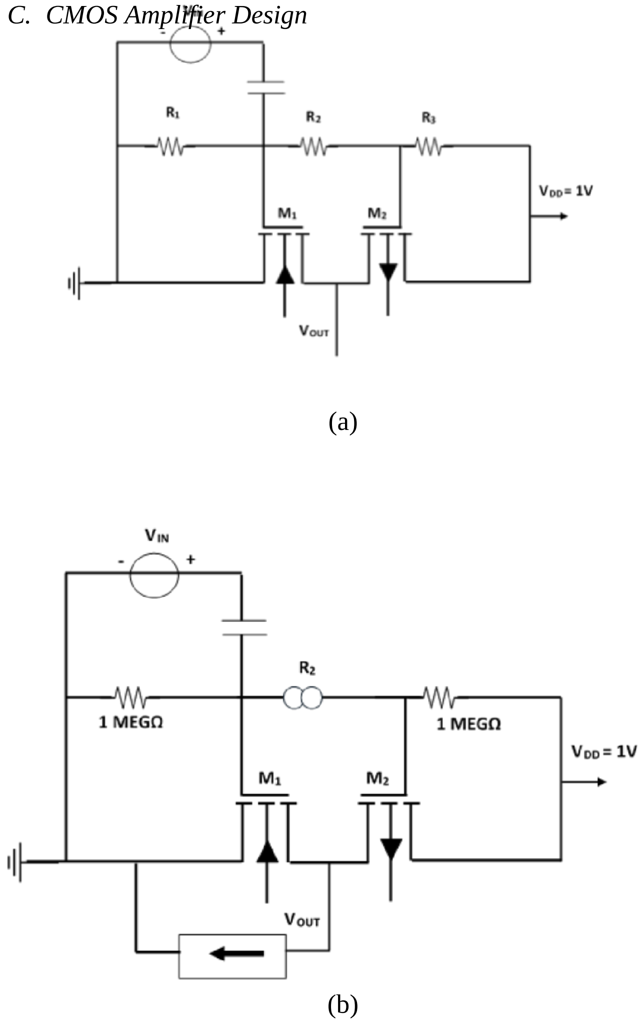

Fig 2: CMOS Amplifier Design

This module's core subjects are design concepts and techniques for CMOS boosters, which are crucial components of mixed-signal and analog circuits. As seen in Figs. 2(a) and (b), applications for CMOS transistors include signal training, data structure transformation, and sound amplification. Voltage signals are amplified using CMOS transistors.

D. CMOS Inverter Design

When Vin is high and equal to VDD, the NMOS transistors indicate ON and the PMOS transistors indicate OFF (see image below). As a result, direct current flows between Vout and ground, proving that Vout = 0 V. On the other hand, as Fig. 2 illustrates, when Vin is low, PMOS and NMOS transistors are ON and OFF, respectively.

Consequently, the current that flows straight from VDD to Vout and charges the load capacitor illustrates that Vout = VDD. Thus, the gadget performs the function of an inverter as it appears on the surface.

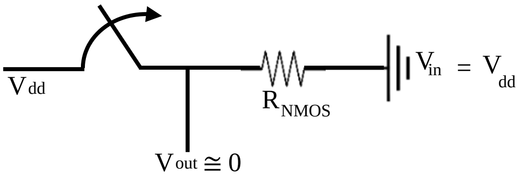

Fig 3: CMOS Inverter

The CMOS inverter has the following features:
(1) Because there is a direct connection between the electrical supply and grounded, the CMOS inverters have low output resistance.
(2) In a CMOS inverter, the voltage swing is VDD0, or VDD, because the resulting value is neither GND nor VDD.
(3) Because the MOS transistor's gates don't require any DC input power, the CMOS inverter's input capacitance is rather high.

E. Methods

Using a combination of modeling, simulation, and experimental techniques, the reliability of modern CMOS image sensors and transistors in radiation-prone situations is assessed. *Simulating and Modeling* : Impact of Radiation Simulation: Using technology computer-aided design (TCAD) tools, simulate the effects of TID, displacement damage, and SEEs on CMOS image sensors. Device Degradation Modeling: Create models to forecast how radiation exposure may cause CMOS image sensors to deteriorate over time. Probabilistic Computation Simulation: To assess the effects on performance and reliability, simulate the integration of sMTJs with CMOS circuits.

Experimental Approach : Radiation exposure tests using an experimental approach are used to assess how regulated radiation sources affect the performance characteristics of CMOS image sensors, including noise, signal-to-noise ratio, and dark current. Characterization of sMTJs: Assess how well radiation-exposed sMTJs integrated with CMOS circuits function. Reliability Assessment: In radiation-prone situations, perform accelerated aging experiments to evaluate the transistors and CMOS image sensors' long-term dependability.

III. RESULTS AND DISCUSSION

A. CMOS Image Sensors and Radiation Effects

Both the simulation and the actual data show that radiation exposure significantly reduces the performance of CMOS image sensors. TID effects cause noise and dark current to rise, and displacement damage results in flaws that exacerbate the performance degradation of the sensor. Sensor failures, both temporary and permanent, are caused by SEEs.

B. How sMTJs Affect Reliability

When sMTJs are integrated with CMOS circuitry, the sensors' dependability in radiation-prone situations is improved. Radiation-induced defects are less severe because of the redundancy and fault tolerance offered by the stochastic nature of sMTJs.

C. Probabilistic Computation in Radiation-Prone Environments

In radiation-prone situations, the probabilistic computation framework with CMOS + sMTJ structures demonstrates encouraging results in terms of performance and reliability maintenance. Leveraging the stochastic nature of sMTJs improves the computation's resilience to mistakes caused by radiation.

IV. CONCLUSION

This study's findings emphasize how crucial it is to evaluate and minimize radiation's negative impacts on sophisticated CMOS image sensors and transistors. After a thorough evaluation of the effects of displacement damage, single-event effects (SEEs), and total ionizing dose (TID) on these components, the study concluded that there was a considerable decline in performance under radiation exposure. Furthermore, the incorporation of stochastic nanomagnets—more precisely, spin-transfer torque magnetic tunnel junctions, or sMTJs—showed encouraging outcomes in terms of improving dependability and permitting probabilistic computation in situations with high radiation.
Utilizing the stochastic properties of sMTJs, the study proposes a workable method to reduce radiation-induced errors and enhance device robustness. These discoveries advance the field of radiation-tolerant devices toward more trustworthy and long-lasting solutions by providing important insights into the design and development of future electronic systems capable of retaining robust operation in harsh radioactive environments.

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