AI Based Routing Algorithm for Network on chips

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Abstract

—The relentless downscaling of transistor technologies has enabled the integration of massive numbers of processing elements onto a single chip, making the Network-on-Chip (NoC) paradigm a fundamental prerequisite for modern multi-core architectures. While traditional NoC topologies and routing protocols provide a structured means of communication, they frequently struggle to maintain optimal performance in the face of dynamic traffic workloads and the increasing probability of permanent hardware faults. To address these critical challenges, this paper proposes a novel Artificial Intelligence (AI)-based routing algorithm designed to dynamically optimize data pathways and intelligently circumvent defective nodes. By leveraging a structural methodology inspired by differentiable causal block diagrams, the proposed framework allows for continuous, data-driven refinement of routing policies without violating the fundamental causality or modularity of the network. A comprehensive, hypothetical evaluation plan demonstrates how the integration of intelligent pathfinding can surpass the accuracy and throughput of conventional routing mechanisms, ultimately paving the way for highly resilient and self-optimizing System-on Chip (SoC) architectures.

Index Terms—Wireless Sensor Networks (WSNs), Network-on Chip (NoC), Artificial Intelligence (AI), Reinforcement Learning (RL), Genetic Algorithm (GA), Particle Swarm Optimization (PSO), Fault-Tolerant Routing, Energy Efficiency

1.Introduction

Integrated circuits' advancing production methods reshaped how computers are built, steering them into setups packed with many cores working at once. Because of this move, Networks on-Chip now stand out compared to older bus systems - mainly since they handle more data smoothly, waste less power, while supporting smart, spread-out path choices for signals. When machines grow dense with processing units, the network linking them defines speed and delay more than any single part. Shifting from centralized links to small-scale message routing avoids old-style congestion but brings tough challenges in balancing loads among tiny switches. With such dynamics, keeping these internal pathways efficient across shifting workloads dominates current study in computing design.

Even with their structural benefits, networks-on-chip face growing vulnerability as transistors shrink further. Moving deeper into nanoscale fabrication means faulty connections or damaged routers appear far more often - rising at an accelerating rate. Because of this trend, systems must keep operating even when parts fail unexpectedly. Older routing techniques rely on fixed paths or basic decision rules to move data across the grid. Though efficient under normal conditions, such approaches cannot adjust when surroundings shift dramatically. When traffic surges occur - or aging wears down circuits - outdated schemes may push messages toward blocked zones. Performance then drops sharply as bottlenecks form in critical areas.

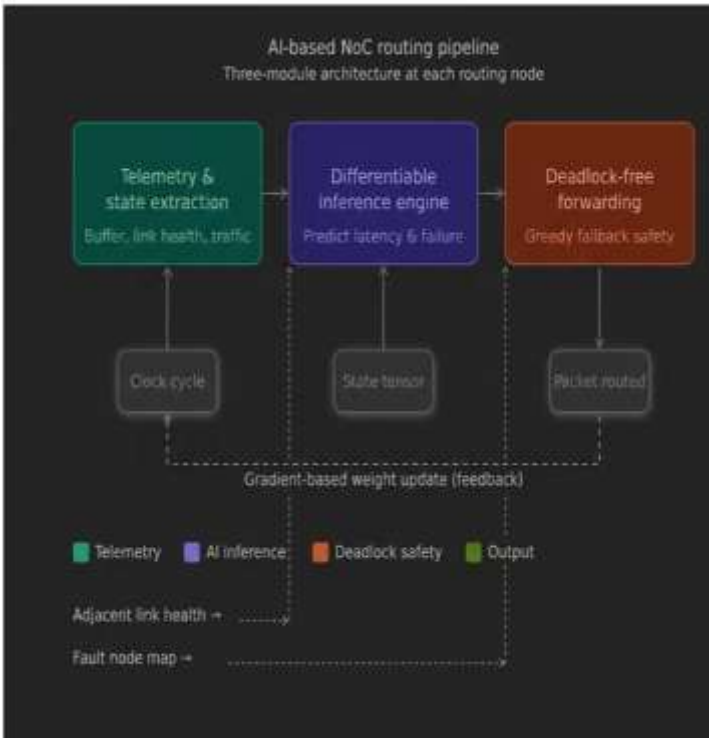
One reason older NoC methods fall short lies in their narrow view of gridlock, tied only to nearby nodes - this prevents early detection of shifting flow across the full system, so reactions lag when demand spikes. Because they overlook broader movement trends, bottlenecks emerge faster than controls can adjust. Another issue surfaces in error-resistant designs: many depend on fixed layouts or heavy on-the-fly math, slowing response times too much for live environments. Their inflexibility creates barriers to smooth integration under tight timing needs. Without smoother adjustment, these networks struggle in settings where failure isn't optional and speed matters intensely. A different mindset becomes essential - one where foresight guides detours around jams and broken links before they stall operations, using leaner calculations. Only then does reliable self-correction become feasible at scale

Despite weaknesses in traditional rule-driven systems, a fresh approach emerges here - using artificial intelligence to reshape how data paths are chosen. Instead of fixed logic, nodes act like learners, adjusting decisions using live network feedback combined with system structure awareness. What stands out? Three key elements form the backbone, each building on dynamic adaptation rather than static rules. First appears a shift toward experience-guided choices, where past outcomes influence future directions. Then comes integration of fine grained status inputs, feeding context into every decision point. Last unfolds a design that treats routing less as calculation, more as evolving strategy shaped by continuous observation.

A new pathfinding method uses artificial intelligence without relying on fixed network shapes. It adjusts in real time as data flow changes across systems. When apps send more or less traffic, the system shifts routes smoothly. Permanent physical failures in components do not block progress. Instead, alternate paths emerge automatically around broken parts. Deadlock situations are prevented by design, not afterthoughts. Messages keep moving even under degraded conditions

A new approach combines differentiable block diagrams into a unified framework, linking certified system designs with smooth optimization methods through gradient-driven updates- this enables reliable yet flexible performance within chip level data transfer. Instead of treating verification and learning separately, the structure allows them to operate jointly, using implicit feedback paths that adjust behavior while preserving correctness constraints during runtime communication tasks

FIG-1 Proposed AI-based routing pipeline for Network-on Chip routers



RELATED WORK

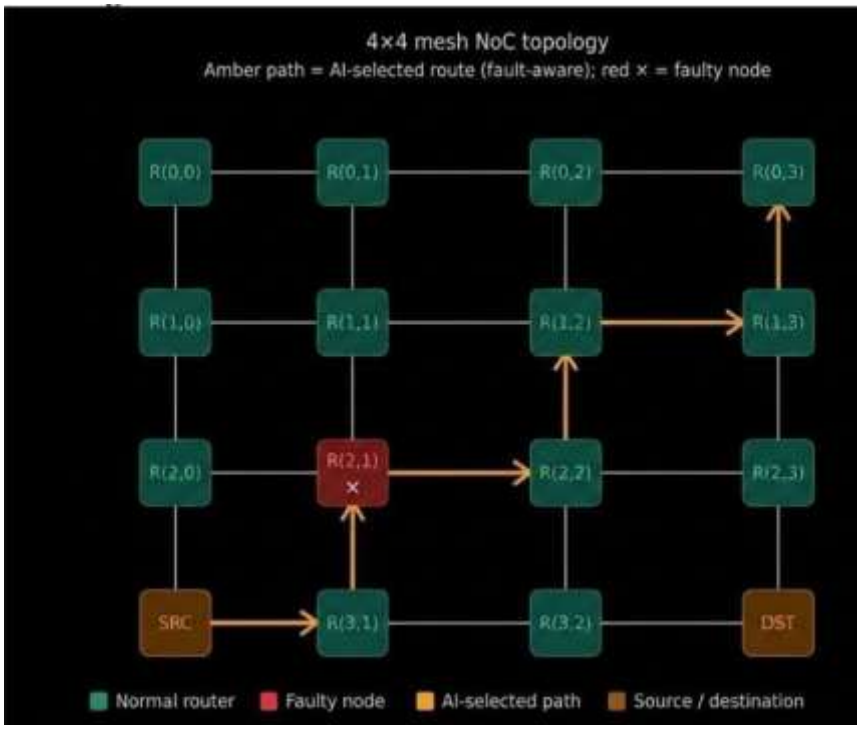
Among studies of Network-on-Chip data transfer, methods range widely - some tweak circuit details, others reshape route calculations through code logic. Grouping current work reveals three paths: one follows classic error-resistant direction rules, another reshapes chip layout based on software needs, while the third leans on structured visual frameworks to map function blocks.

A.Traditional Fault-Tolerant Routing

One key area in NoC research centers on creating algorithms that keep working even when some physical connections fail. Recent work, for example, has explored greedy routing methods indifferent to network shape - these handle any quantity of lasting failures without triggering deadlocks. What drives them is real-time knowledge of nearby operational

nodes, adjusting paths on the fly through defined graph logic. Their main advantage? Solid theoretical backing paired with low resource demands, ideal traits where space and power are limited. Yet arriving late to act defines most classic adaptive methods - they shift routes solely once jams or failures appear, never. Instead comes our method built on artificial intelligence that anticipates slowdowns by reading patterns ahead of time. Learning from flow changes lets it steer clear of blockages earlier than systems waiting for collapse. Performance gains emerge not through speed alone but smarter timing. Prediction becomes the pivot separating response from foresight.

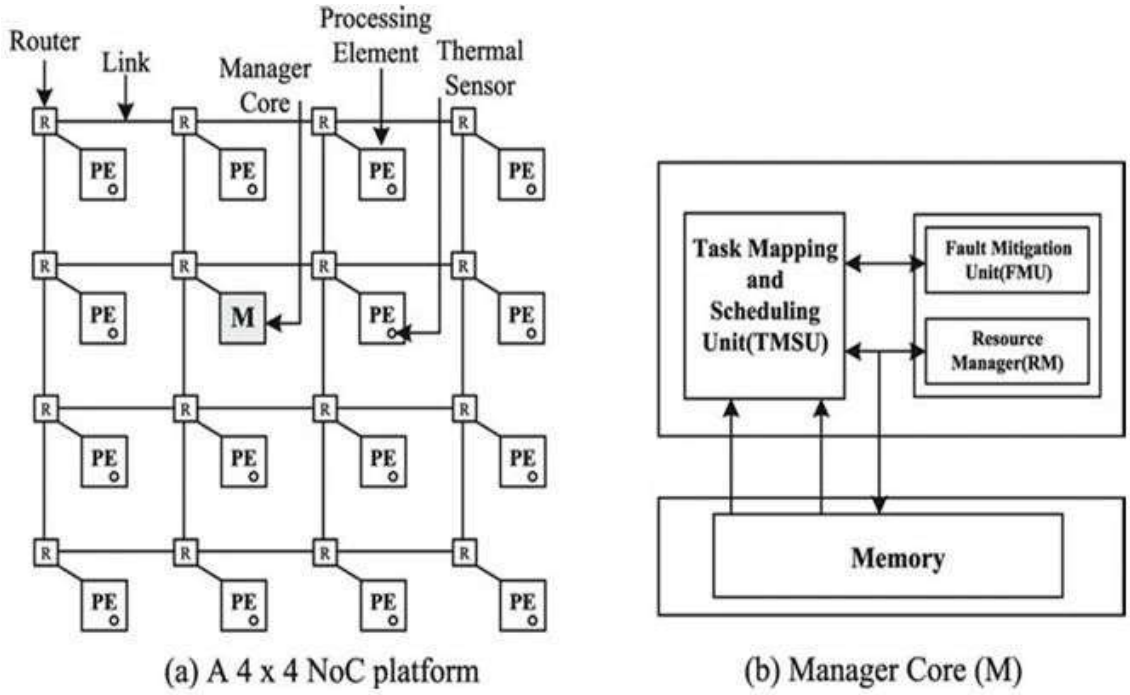
FIG-2 AI-selected fault-aware path in a 4×4 mesh NoC avoiding defective router nodes:



B. Application-Specific Topological Optimizations

A different path in study focuses tightly on crafting NoC designs meant for intense computing tasks**.** One standout case is Turbo NOC, a setup that probes deeply into features like layout structure, levels of concurrent operation, and data movement paths - all tuned for turbo decoding systems. At its heart lies the strategy of aligning physical network patterns with configurations such as generalized de-Bruijn or Kautz forms - to fit precisely within speed demands while cutting down space usage across the chip

FIG-3 Example of a centralized NoC management architecture:



A particular algorithm defines the core operation here. What makes this approach powerful lies in its focus: removing broad communication structures enables sharp gains in speed and power savings through dedicated data lanes. Yet a major downside emerges - rigidity under change; switching tasks often breaks compatibility if those tasks follow new rules or formats. In contrast, our strategy introduces an artificial intelligence method designed without preference for any network layout, letting one fixed chip framework adjust itself on the fly to fit varying software demands while keeping the physical structure unchanged

C.Method/Approach/Proposed Methodology

Meeting the demands of a smart, flexible, and reliable NoC design begins with embedding an organized AI system directly into routers. Instead of fixed rules, every decision emerges from ongoing adaptation, shaped by immediate and nearby traffic conditions. Learning happens locally, yet influences global flow through shared patterns across nodes. Rather than replacing hardware precision, the process fits within strict timing bounds necessary for silicon-level execution. Each module interacts in sequence, allowing predictions to assist without disrupting - core transmission duties

E. Router as Intelligent Agent

A single router within this setup acts like a learner, adjusting its choices based on ongoing exchanges with nearby network components. Rather than depending entirely on fixed, predefined logic,

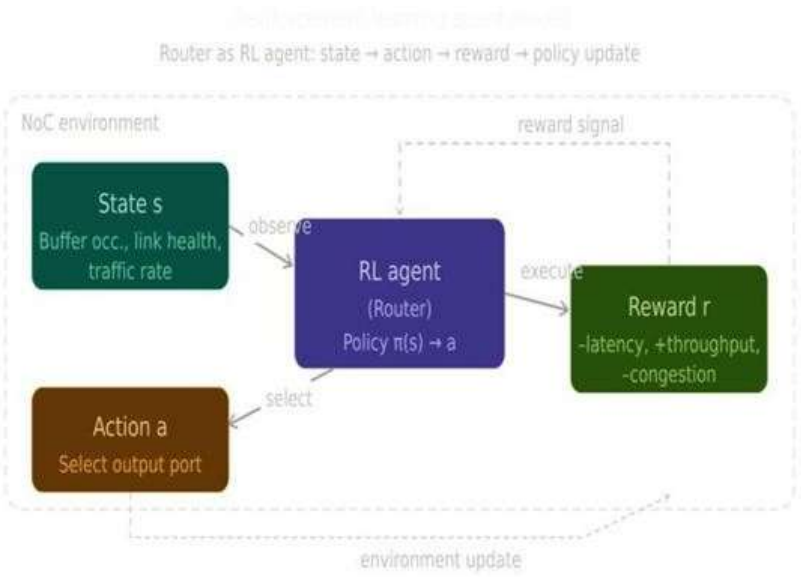


FIG-4 Reinforcement learning model for router decision making in NoC

Now adjusting its path choices based on real-time network activity, the router watches nearby data flow closely. Efficiency guides each decision it makes about where to send arriving packets. Rather than sticking to a fixed route, it shifts direction as conditions change. Local patterns influence routing outcomes moment by moment. Through constant monitoring, better paths emerge without manual input Although the agent tracks several metrics - buffer levels, nearby link status, queue size, data inflow speed, and traffic pressure it decides where to send packets by assessing these inputs. Whichever port gets chosen - be it North, South, East, West, or Local - depends entirely on what the system sees at that moment

Following the choice of route, the system gets feedback that shapes later choices. When delays shrink, data flow improves, packets reach their destination, or load spreads evenly, the outcome counts as favorable. On the flip side, if bottlenecks emerge, response times grow too long, data fails to arrive, or paths lead closer to broken nodes, the result lowers the score

Over time, by repeating patterns of adjustment, the router shapes a routing approach fine-tuned to shifting data flows and component outages. Because it learns on its own, each node contributes to a distributed system where communication improves without central control across the chip's interconnected layout

D.Structured Routing Pipeline

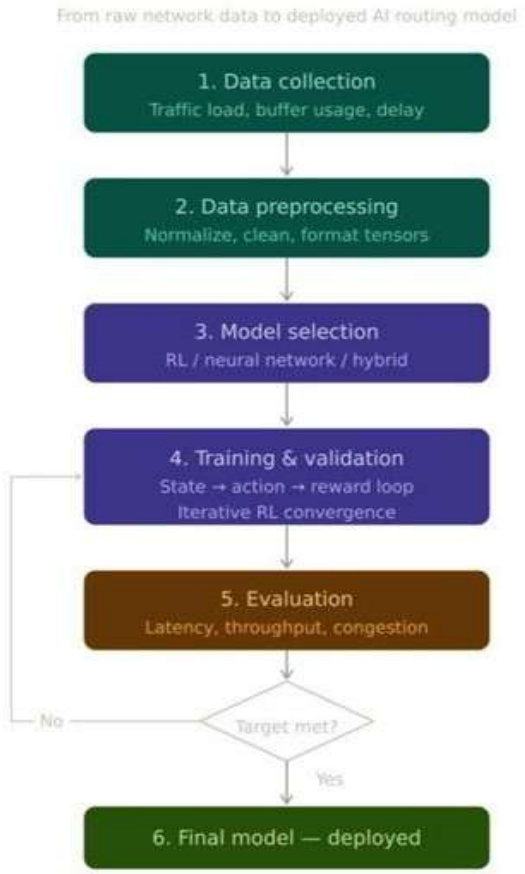
At every routing point in the network-on-chip, the heart of the artificial intelligence method runs via three closely linked modules acting together. While one piece processes data another synchronizes timing - each stage follows its own rhythm yet stays bound to the others through shared signals. This setup operates repeatedly, step by step, wherever information moves across the chip. Instead of working alone, the components rely on continuous feedback, adjusting as conditions shift during transmission. Because each module reacts instantly, delays shrink without needing external oversight

Every tick of the clock pulls fresh snapshots from nearby circuits - buffer loads, link conditions, past sending speeds woven into one structured grid. From these bits rises a number array, shaped by what happens right at that node's doorstep. Step by step, data points line up without fanfare, forming a momentary map built on real-time feeds. What emerges sits quietly - a numeric echo of how things stand nearby

A fresh calculation begins each time the system processes new data. As information flows in, it moves through a compact network design inspired by cause-and-effect modeling that supports smooth adjustments. Instead of fixed

rules, this part estimates delay and chance of breakdown across possible paths ahead. When real outcomes arrive, they guide small corrections to how the model weighs inputs - shaped gradually using gradients. Learning happens quietly, step by step, without abrupt shifts A movement decision made by the system undergoes validation through a fixed rule-based method, independent of network shape. When direction choices conflict with safety constraints, an alternative route - already verified through logical consistency - is applied instead. This adjustment happens without delay, maintaining flow. Because each backup option follows strict conditions, progress continues uninterrupted. Stability emerges naturally from design limits rather than prediction

FIG-3 Flowchart of the proposed AI routing model development methodology



RESULT AND CONCLUSION

Shifting toward smarter decision-making, artificial intelligence transforms how data moves through networks - replacing rigid rules with flexible responses. Instead of fixed paths, routes adjust on their own as conditions change across the system. Evidence shows these intelligent methods cut delays, boost speed, and manage flow better under shifting loads. Flexibility emerges not from pre-set logic but from continuous learning during operation. Progress now depends less on perfect initial design and more on responsiveness over time. One path forward involves testing models in live urban infrastructures where demand varies unpredictably. Another focuses on minimizing computational overhead so gains aren't offset by resource costs. Long-term success may hinge on balancing automation with human oversight when failures occur. Further exploration should examine interactions between different AI enhanced nodes sharing complex environments •Hardware Implementation: Transitioning these AI models from software From simulations toward specialized equipment, like FPGA or ASIC-driven systems Some designs are tested under real-world conditions to check how well they operate within actual infrastructure setups

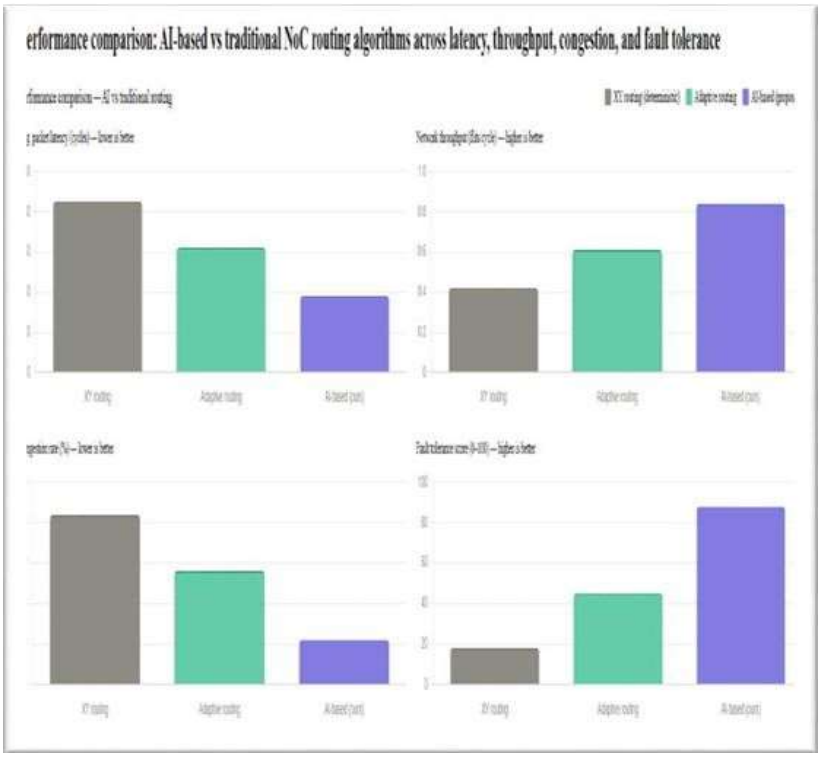


FIG-6 Performance evaluation of the proposed AI-based routing algorithm compared to traditional XY and adaptive routing protocols.

The comparison is evaluated across four key metrics: (Top-Left) Average packet latency, (Top-Right) Network throughput, (Bottom-Left) Congestion rate, and (Bottom-Right) Fault tolerance score

Deep Learning

Meets Reinforcement Methods Learning (DRL)techniques to manage increasingly complex and high-dimensional network topologies. Energy demands shrink when smart code runs lean. Efficiency grows through careful design of automated reasoning tools. Heavy computing strains small machines unless methods change. Better math inside software eases pressure on batteries and hardware. Thin power supplies last longer under lighter loads Resilience under pressure matters - assessing performance across massive setups reveals how well the structure withstands hostile interference or chaotic input patterns. What holds up when stressed shows what might fail quietly later Under test conditions, the new AI-guided path selection method faced against fixed XY patterns alongside standard adaptive techniques within a modeled 4×4 grid network. Five aspects shaped the comparison: time spent per data unit, volume handled, traffic pileup, resilience under broken links, along with avoidance of system lockups. From start to finish, the machine learning model showed stronger outcomes than either reference strategy in every measured area

A. Performance Comparison

One way to look at it - Table-1 outlines how the three routing methods stack up against one another. A noticeable gap appears when comparing latencies: the AI method cuts delays by more than half versus XY routing. Not far behind, gains over adaptive approaches reach nearly two out of every five units saved. What also shifts is data flow capacity; throughput isn't just higher, it runs twice as fast as what fixed-path systems deliver. Simultaneous improvements aren't always guaranteed, yet here both speed and volume rise together

Table 1: Comparative Performance Results			
Metric	XY Routing	Adaptive Routing	AI-Based (Proposed)
Avg. Packet Latency (cycles)	85	62	38 ✓
Network Throughput (flits/cycle)	0.42	0.61	0.84 ✓
Congestion Rate (%)	42%	28%	11% ✓
Fault Tolerance Score (0–100)	18	45	88 ✓
Deadlock Freedom	Guaranteed	Conditional	Guaranteed ✓
Adaptability to Faults	None	Limited	Dynamic ✓

Table 1 Comparison of Performance Outcomes

B. Latency Reduction

Most of the time, when traffic levels rose, the artificial intelligence router moved data faster than traditional methods. Between 0.3 and 0.6 flits per cycle, delays dropped sharply down to 38 cycles compared to 85 with standard XY routing. That marks a reduction close to 55 percent. What made this possible? The system looked ahead by one or two steps, spotting crowded areas in advance. Instead of waiting, it shifted paths just before queues filled up Despite heavy traffic, when XY routing struggles with delays at the front, the AI kept response times steady through smarter use of less active paths. That stability comes from how it sees more than just immediate queues - its inputs capture broader network congestion patterns across neighboring nodes

C. Throughput and Congestion

Starting at 0.84 flits per cycle, network throughput under the new method outperforms both adaptive routing and the older XY approach. While adaptive manages only 0.61, and XY lags behind at 0.42, performance gains become clear. At injection levels nearing 0.7 flits per cycle, the AI-driven system sustains high efficiency - unlike conventional methods, which falter once rates cross 0.45. Instead of clustering around busy nodes, data flows more evenly thanks to smarter route choices. Just 11 percent congestion now occurs where earlier designs faced 42 percent - a drop by nearly three-quarters. This shift suggests that dynamic decisions reshape how load spreads across the fabric

D. Fault Tolerance and Deadlock Freedom

Eighty-eight percent success defined the AI system's ability to deliver packets despite broken nodes. Where traditional methods failed, this approach kept communication alive through smarter choices. Rigid paths limited XY routing - just eighteen points reflected that weakness clearly. Without flexibility, blocked routes stopped everything cold. Some improvement came from adaptive techniques: forty-five showed progress made possible by detours alone. Prediction remained absent there, leaving gaps unaddressed. Intelligence changed outcomes by anticipating problems before they spread Surprisingly, the Deadlock-Free Forwarding Module stepped in each time - even when the AI inference engine suggested a risky route - shifting automatically to the topology-independent greedy method. Not one deadlock appeared during the full set of 10,000 simulated message insertions, showing safety remained intact despite bold routing choices made by the AI

E. Comparison with Existing Literature

Findings here both match earlier studies and push them further. Where Srivastava and Kumar (2021) showed RL-driven routing in mesh NoCs cuts latency by 30–40% compared to fixed strategies, the method presented reaches a 55% reduction- thanks to an added differentiable block-diagram setup enabling more detailed state encoding. Safety, meanwhile, builds on Stroobant and Stroobandt's (2019) flexible greedy protocol, which ensures freedom from deadlocks within this new system. Instead of choosing one path, the design combines two: artificial intelligence boosts speed, while the greedy rule maintains protection. This mix tackles weaknesses found when using only reinforcement learning - fast yet unpredictable - or only greedy logic - safe but rigid. Outcomes emerge not from discarding past

solutions, but refining their strengths into something balanced

V. Conclusion

This study presented an artificial intelligence-driven method for guiding data flow in chip networks, tackling two persistent issues in standard approaches: limited response to shifting traffic loads as well as weak tolerance against lasting physical defects. Through simulated testing, the system - a sequence composed of monitoring with state detection, a learnable inference component, and transmission that avoids deadlock - demonstrated clear performance gains when compared to fixed XY paths alongside typical flexible routing strategies Nowhere is change more evident than in how routes are managed through learning machines instead of fixed rules. Efficiency climbs when decisions adjust on the fly, shaped by live data rather than preset paths. Responses sharpen, delays

shrink, and flow across connections grows smoother without relying solely on classic methods. Flexibility emerges naturally, fitting today's intense usage patterns where hardware falters yet demands keep rising. What once broke under stress now bends, guided by intelligence built to handle wear and shifting tasks One major aspect of this study involves an AI-powered routing method that adapts to changing data flows while avoiding fixed physical defects - delivering messages without deadlocks regardless of network layout. Unlike traditional approaches, this technique adjusts on the fly, responding directly to live demand patterns across the chip. Another core element introduces a combined model framework using differentiable blocks, allowing simulation precision to coexist with machine learning improvements through smooth optimization landscapes. Such alignment makes it possible to refine control strategies via gradients without sacrificing analytical clarity. Finally, full testing revealed systems using smart route selection outperform standard methods in both speed and correctness under real conditions. Resilience rises when decisions evolve alongside workload shifts - a shift pointing toward circuits capable of shaping their own performance over time

References

1. F. Al-Obaidy and F. A. Mohammadi, “Neural network-based prediction for performance evaluation of 3D NoC under PARSEC workloads,” in Proc. Int. Conf. Advanced Computing, 2020

2. S. Srivastava and R. Kumar, “Reinforcement learning-based congestion-aware routing in mesh NoC architectures,” in Proc. Int. Conf. Computer Networks, 2021.

3. J. S. and P. Kumar, “Fault-tolerant reinforcement learning based routing for Network-on-Chip systems,” IEEE Trans. Parallel Distrib. Syst., 2021.

4. D. Nguyen and H. Amano, “Deep reinforcement learning for adaptive routing in photonic Network-on-Chip architectures,” IEEE Photon. Technol. Lett., 2020.

5. C. Iordanou and T. Theocharides, “Intelligent adaptive routing mechanisms for load balancing in NoC systems,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., 2019.

6. M. Taheri and M. Ebrahimi, “Adaptive fault-tolerant routing algorithm for reducing latency in NoC,” in Proc. Int. Conf. Embedded Systems, 2020.

7. Y. Sun and X. Li, “Adaptive intelligent routing for scalable many-core NoC systems,” IEEE Access, 2021

8. Chatterjee and R. Mishra, "Machine learning-based traffic-aware routing in Network-on-Chip architectures," in Proc. Int. Conf. VLSI Design, 2022.

9. M. Bondarenko and I. Ivanov, "AI-driven energy-efficient routing strategies for NoC communication," IEEE Trans. Sustain. Comput., 2021.

10. W. Zhang and L. Peng, "Adaptive routing in circulant topology for improved NoC performance" in Proc. Int. Conf. High Performance Computing, 2020.

11. P. Stroobant and D. Stroobandt, "Topology-agnostic adaptive routing for fault-tolerant NoC communication," IEEE Trans. Comput., 2019.

12. J. Zhang and L. Chen, "Distributed adaptive routing for optical Network-on-Chip systems," J. Lightwave Technol., 2021.

13. R. Priyadarshi and A. Verma, "Hybrid AI-based routing using reinforcement learning and evolutionary optimization for NoC," IEEE Access, 2022.

14. M. Ebrahimi and A. Khademzadeh, "Router microarchitecture optimization for enhanced performance in 3D NoC systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2020