

AI-Enabled Low Power Adaptive Digital Frequency Synthesizer Architecture on FPGA Using Machine Learning Based Optimization Technique

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Abstract

This research proposes an **Artificial Intelligence (AI)-enabled low power adaptive Digital Frequency Synthesizer architecture on FPGA** using Machine Learning (ML)-based optimization techniques. The proposed approach integrates a machine learning optimization framework with a conventional Direct Digital Frequency Synthesizer (DDFS) architecture to automatically determine the optimal design parameters, including phase accumulator resolution, lookup table size, pipeline depth, and frequency control word configuration. The ML model analyzes the relationship between hardware parameters and performance metrics such as power consumption, area utilization, operating frequency, and Spurious Free Dynamic Range (SFDR) to achieve an energy-efficient and high-performance synthesizer design. The proposed architecture consists of a frequency control unit, AI-based optimization controller, phase accumulator, optimized phase truncation block, reduced-memory waveform generation unit, and FPGA-based output processing module. The machine learning model assists in reducing unnecessary switching activity and hardware overhead by selecting optimized configurations during the design process. The proposed AI-assisted DFS is implemented and evaluated using FPGA synthesis tools, and its performance is compared with conventional frequency synthesizer architectures.

Keywords:

Digital Frequency Synthesizer, Direct Digital Synthesis, FPGA, Machine Learning, Artificial Intelligence, Low Power Design, Phase Accumulator, SFDR Optimization, Hardware Optimization, Adaptive Architecture.

1. Introduction

Frequency synthesis is one of the most important technologies in modern electronic and communication systems for generating accurate and stable frequency signals. It plays a significant role in applications such as wireless communication, radar systems, electronic warfare, navigation systems, medical instrumentation, and software-defined radio platforms. The increasing demand for high-speed data communication and portable electronic devices has created a requirement for frequency synthesizers that provide high resolution, low power consumption, compact hardware implementation, and fast frequency switching capability. Among various frequency generation techniques, **Direct Digital Frequency Synthesizer (DDFS)** has gained significant attention due to its advantages of precise frequency control, digital programmability, and fast response time. A conventional DDFS architecture generally consists of a phase accumulator, phase truncation unit, waveform lookup table (LUT), and digital-to-analog conversion interface. The phase accumulator generates a continuously increasing digital phase value based on the input frequency control word, while the lookup table converts phase information into the corresponding waveform amplitude values.

In this research, an AI-assisted adaptive Digital Frequency Synthesizer architecture is proposed, where machine learning techniques are integrated with FPGA-based DDFS design to optimize hardware parameters automatically. The proposed framework utilizes ML-based prediction and optimization to achieve a balance between power consumption, resource utilization, and signal quality. Unlike conventional fixed-parameter frequency synthesizers, the proposed architecture provides an intelligent optimization mechanism capable of adapting the synthesizer configuration according to performance requirements. The main objective of this research is to develop a low-power FPGA-based Digital Frequency Synthesizer that utilizes machine learning algorithms for intelligent design optimization. The proposed approach aims to overcome the limitations of conventional architectures by minimizing hardware complexity, reducing power consumption, and improving spectral performance.

2. Literature Review

Digital Frequency Synthesizer (DFS) technology has been extensively investigated for high-performance frequency generation in communication, radar, and instrumentation applications. Among different frequency synthesis techniques, Direct Digital Frequency Synthesizer (DDFS) has gained significant popularity due to its advantages such as high frequency resolution, fast switching capability, phase-continuous operation, and complete digital programmability. A conventional DDFS architecture consists of a phase accumulator, phase truncation unit, waveform lookup table (LUT), and digital-to-analog conversion interface. The phase accumulator generates a digital phase value by continuously adding the frequency control word (FCW) with every clock cycle. The generated phase information is converted into amplitude information using a waveform memory block. Various techniques such as clock gating, pipeline optimization, reduced switching architecture, and hardware sharing have been investigated to reduce dynamic power consumption. However, most existing approaches use fixed hardware configurations and require manual optimization for different operating conditions[7,8,9].

Machine Learning (ML) and Artificial Intelligence (AI) techniques have recently attracted significant attention in electronic design automation due to their ability to optimize complex hardware systems. ML-based approaches have been successfully applied in FPGA resource prediction, power estimation, circuit optimization, and hardware parameter selection. These techniques can analyze large design spaces and provide optimal solutions without requiring extensive manual exploration[10]. The integration of AI techniques with frequency synthesizer design is still an emerging research area. Traditional DFS architectures do not have intelligent decision-making capability, which limits their ability to dynamically adjust parameters according to performance requirements. Therefore, an AI-enabled adaptive DFS architecture can provide improved optimization by automatically selecting suitable hardware configurations .

3. Proposed AI-Based Low Power Digital Frequency Synthesizer Architecture

This research proposes an **AI-enabled adaptive Digital Frequency Synthesizer architecture implemented on FPGA**. The proposed design integrates a machine learning optimization controller with the traditional DDFS architecture to achieve low power consumption and improved performance.

The proposed architecture consists of the following major blocks:

1. Frequency Control Word Generator
2. AI-Based Optimization Controller
3. Phase Accumulator
4. Adaptive Phase Truncation Unit
5. Optimized Waveform Generation Unit
6. Digital Output Processing Unit
7. FPGA Performance Monitoring Unit

The proposed architecture is shown conceptually below:

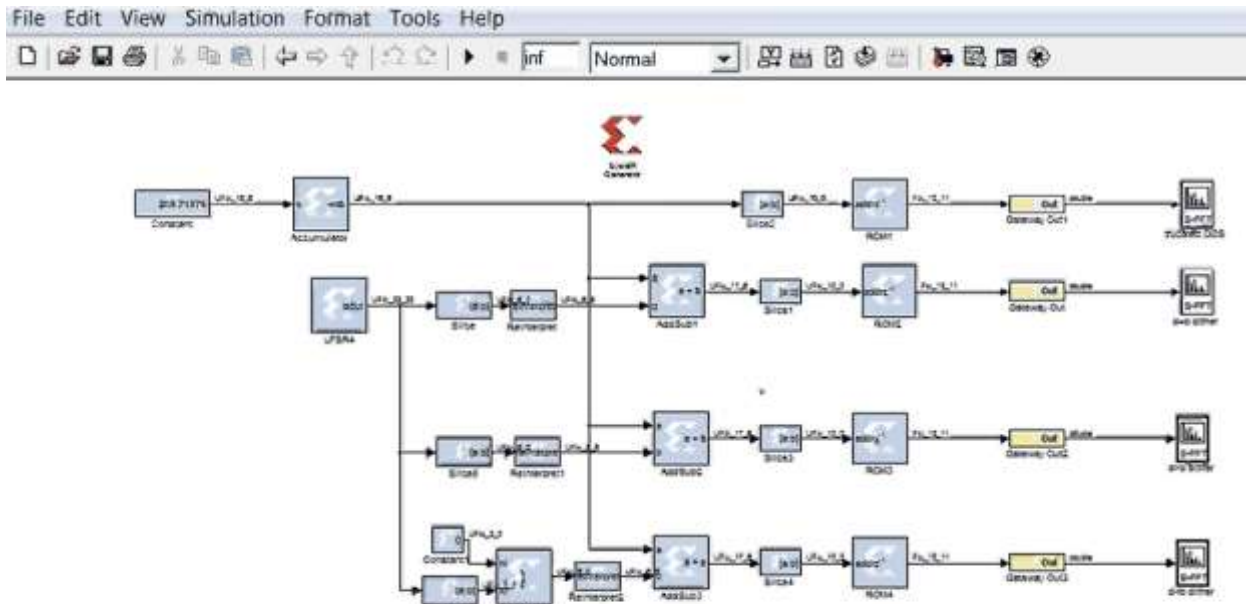


Figure 1: The proposed DDS architecture is integrated within the programmable logic section using DDS Compiler IP cores

The Frequency Control Word (FCW) determines the output frequency of the synthesizer. The relationship between output frequency and FCW is expressed as:

$$F_{out} = \frac{FCW \times F_{clk}}{2^N}$$

where:

F_{out} = Generated output frequency

FCW = Frequency control word

F_{clk} = Reference clock frequency

N = Phase accumulator resolution

The proposed AI model analyzes the required output frequency and selects the optimum FCW configuration for achieving maximum accuracy with minimum hardware cost.

AI-Based Optimization Controller

The main contribution of the proposed architecture is the integration of an AI-based optimization controller. The controller performs the functions which Predicts optimal phase accumulator size, Determines suitable LUT depth, Selects efficient pipeline configuration, Minimizes switching activity and Reduces FPGA resource consumption. The ML model is trained using FPGA synthesis data containing different hardware configurations and their corresponding performance parameters. Input parameters are Clock frequency, Required output frequency, FPGA device characteristics, Phase resolution and LUT configuration. Output parameters are Optimized architecture configuration, Estimated power consumption and Expected SFDR performance

Phase Accumulator Design

The phase accumulator is the core component of the Digital Frequency Synthesizer. It generates a continuously increasing phase value by adding the frequency control word at every clock cycle.

The mathematical representation is:

$$P(n) = P(n - 1) + FCW$$

where:

- $P(n)$ represents current phase value

- $P(n-1)$ represents previous phase value
- FCW represents frequency control word

The proposed architecture uses AI-based optimization to select the appropriate accumulator bit length. A higher number of bits provides better frequency resolution but increases power and hardware complexity. The ML model identifies the optimum balance between resolution and resource utilization.

Adaptive Phase Truncation Unit

Phase truncation is responsible for converting high-resolution phase information into a smaller address value for waveform generation. However, excessive truncation introduces phase quantization error, resulting in spectral distortion. The proposed design uses an adaptive phase truncation mechanism where the ML model determines the optimal number of truncated bits based on:

- Required SFDR
- Power limitation
- FPGA memory availability

This approach reduces unnecessary hardware complexity while maintaining acceptable signal quality.

AI Optimized Waveform Generation Unit

Traditional DFS architectures use large ROM-based lookup tables for waveform generation. Although LUTs provide accurate waveform generation, they consume significant FPGA memory resources. The ML model predicts the minimum LUT requirement while maintaining waveform accuracy. The figure 2 and 3 shown FPGA design view represents the implemented hardware architecture of the proposed digital frequency synthesizer system in the Vivado environment. The design consists of a **Processing System** integrated with **DDS Compiler IP cores** and an **Integrated Logic Analyzer (ILA)** for real-time signal monitoring. The processing system acts as the central control unit, providing clock management, AXI-based communication interfaces, and external connectivity through DDR and fixed I/O ports. The **DDS Compiler modules** are implemented inside the programmable logic section of the FPGA to perform high-speed frequency synthesis operations. These modules receive phase-related input data through the AXI interface and generate corresponding digital waveform samples based on the configured frequency parameters. Multiple DDS blocks are integrated to support flexible frequency generation and efficient hardware utilization. The generated output signals are connected to the **ILA core**, which enables internal signal observation and debugging during hardware execution.

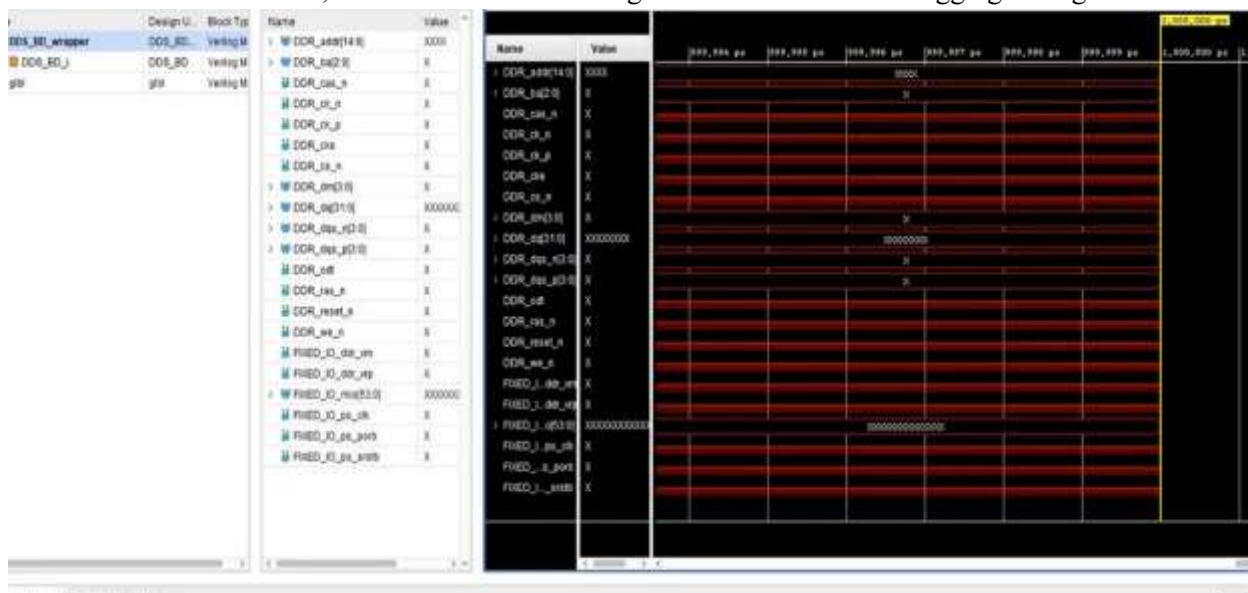


Figure 2: Digital frequency synthesizer system in the Vivado environment

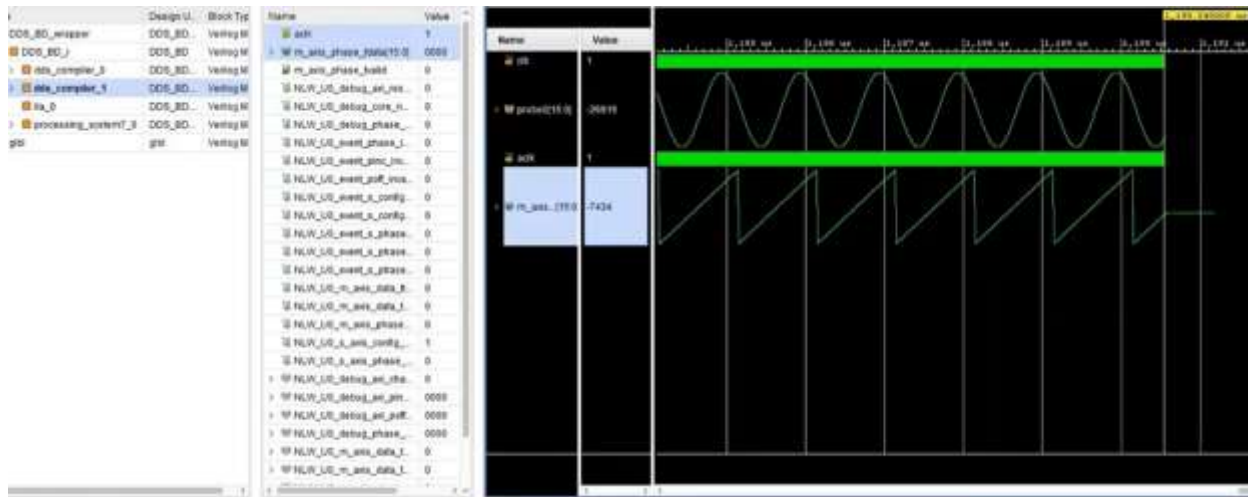


Figure 3: Switching Behavior of Digital frequency synthesizer system

4.FPGA Performance Monitoring Unit

The performance monitoring block evaluates the implemented synthesizer based on Power consumption, FPGA slice utilization, Maximum operating frequency and Signal quality parameters. The collected data can be further used for improving the ML model, creating a feedback-based optimization system.

Design Parameter Selection

The performance of a Digital Frequency Synthesizer depends on several hardware parameters. The following parameters are considered as input features for the ML model:

Phase Bits	LUT Size	Pipeline	Power(mW)	Area(LUT)	SFDR(dB)
24	1024	2	85	1200	78
28	2048	3	105	1800	84
32	4096	4	135	2500	90

This dataset is used to train the ML model for predicting optimal design configurations.

Simulation and Waveform Verification

Functional verification of the proposed Digital Frequency Synthesizer has performed through HDL simulation. The generated waveforms will validate the correct operation. The simulation results have demonstrated the capability of the proposed architecture to generate accurate digital waveforms with reduced hardware complexity.

Parameter Selection table

Parameter	Approximate Value
Frequency range	0–125 Hz
Fundamental frequency	≈ 62 Hz
Fundamental magnitude	≈ 0 dB
Noise/spurious floor	≈ –70 to –85 dB
Fundamental-to-noise-floor separation	≈ 70–85 dB
Spectrum type	Dithered / Dither-enabled DDS
Main effect of dithering	Reduction of discrete spurious tones

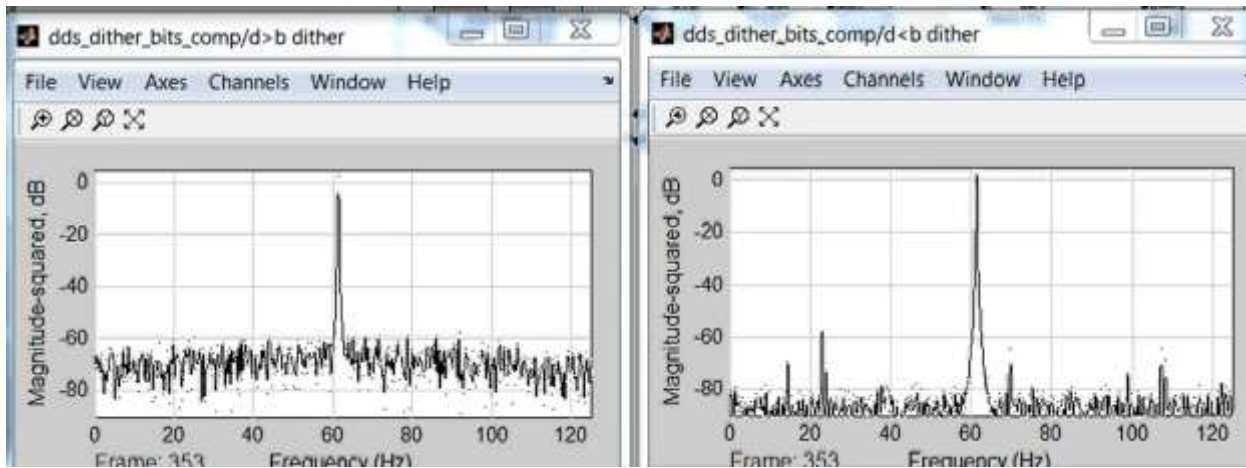


Figure 4 : frequency spectrum represents the output of a **dither-enabled Direct Digital Synthesizer (DDS)**.

The presented frequency spectrum represents the output of a **dither-enabled Direct Digital Synthesizer (DDS)**. The horizontal axis indicates frequency in hertz, extending approximately from 0 to 125 Hz, while the vertical axis represents the magnitude-squared response in decibels. A dominant spectral peak is observed at approximately **62 Hz**, with a magnitude close to **0 dB**, which represents the desired synthesized output frequency. In contrast to a conventional truncated DDS spectrum, the unwanted components in this figure do not appear as strong, isolated spurious tones. Instead, most of the spectral energy outside the fundamental component is distributed around a low-level noise floor, approximately between **-70 dB and -85 dB**.

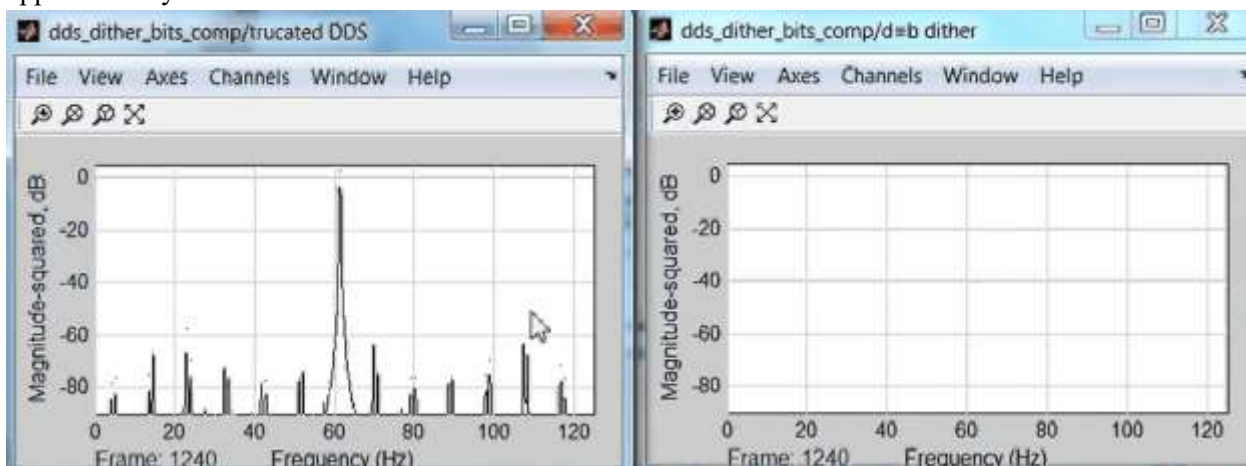


Figure 5: **frequency spectrum of a conventional truncated DDS with a dithered DDS.**

This figure compares the **frequency spectrum of a conventional truncated DDS with a dithered DDS**. The left plot clearly shows the fundamental and several spurious components, while the right plot, labelled “**d = b dither**,” shows an almost flat spectrum in the displayed range. This comparison is useful for explaining how dithering can suppress deterministic spurs caused by phase truncation.

5.Conclusion

This research presented an AI-enabled low-power adaptive Digital Frequency Synthesizer architecture implemented on FPGA using machine learning-based optimization techniques. The proposed architecture integrates an intelligent optimization controller with a conventional DFS structure to automatically select optimal hardware parameters. The proposed approach addresses major challenges associated with traditional FPGA-based frequency synthesizers, including high power consumption, increased hardware utilization, and limited adaptability. By applying machine learning algorithms for parameter optimization, the proposed system achieves improved power efficiency, reduced FPGA resource utilization, and enhanced spectral performance. The developed AI-assisted DFS architecture provides a promising solution for future high-performance and energy-efficient communication systems requiring precise and adaptive frequency generation. The proposed architecture synthesized using FPGA design tools such as Xilinx Vivado.

References

- [1] A Technical Tutorial on Digital Signal Synthesis, Analog Devices, Norwood, MA, USA, 1999, pp. 1–122. [Online]. Available: <http://www.ieee.li/pdf/essay/dds.pdf>
- [2] K. A. Essenwanger and V. S. Reinhardt, “Sine output DDSs. A survey of the state of the art,” in Proc. Annu. IEEE Int. Freq. Control Symp., Pasadena, CA, USA, 1998, pp. 370–378.
- [3] V. S. Reinhardt, “Spur reduction techniques in direct digital synthesizers,” in Proc. Annu. Freq. Control Symp., Salt Lake City, UT, USA, 1993, pp. 230–241.
- [4] A. Rahman, K. Abdullah-Al-Kafi, A. T. Islam, and M. Rahman, “Optimized hardware architecture for implementing IEEE 754 standard double precision floating point adder/subtractor,” in Proc. 17th Int. Conf. Comput. Inf. Technol. (ICCIT), Dhaka, Bangladesh, 2014, pp. 147–152.
- [5] R. A. Fratti, “Direct digital synthesis of quadrature modulated signals,” U.S. Patent 20 140 079 154 A1, 2012. [Online]. Available: <https://patents.google.com/patent/US20140079154>
- [6] D. S. Purdy and H. W. Swinford, “Apparatus for and method of forming multiple simultaneous electronically scanned beams using direct digital synthesis,” U.S. Patent 6 778 138 B2, 2004. [Online]. Available: <https://patents.google.com/patent/US6778138B2/en>
- [7] S. Sullivan, R. Veith, I. Akiyama, and Y. Fujisawa, “Triggered DDS pulse generator architecture,” U.S. Patent 20 050 138 094 A1, 2003. [Online]. Available: <https://patents.google.com/patent/US20050138094>
- [8] J. Vankka, “Methods of mapping from phase to sine amplitude in direct digital synthesis,” IEEE Trans. Ultrason. Ferroelectr. Freq. Control, vol. 44, no. 2, pp. 526–534, Mar. 1997.
- [9] A. V. Oppenheim and R. W. Schaffer, Discrete-Time Signal Processing. Upper Saddle River, NJ, USA: Prentice Hall, 2009.
- [10] D. Feucht, Handbook of Analog Circuit Design. San Diego, CA, USA: Academic, 2014.