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AN ANALYSIS OF THE SYMMETRICAL MULTILEVEL INVERTERTOPOLOGY FOR SOLAR SYSTEMS WITH MINIMAL SWITCHING

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A B S T R A C T

In general, multilevel inverters (MLIs) are regarded as advanced power conversion systems required for medium-voltage and high-power applications. The purpose of this article is to provide an overview of recently investigated MLI topologies classified into various categories based on the transformer requirement such as the transformer less (TL-MLI) and transformer-based (T-MLI) with single and multi-source topologies of symmetric, asymmetric, hybrid and single DC sources for renewable energy applications. For the previous few decades, multiple new variants of each group have been developed. The design and functioning of each topology, as well as each group, are examined in this study. T-MLI topologies of H- bridge, three-leg inverter-based, and other T-MLI configurations are discussed from a configuration standpoint. Each topology's state-of-the-art of both MLI configurations and problems are treated separately. Furthermore, the disadvantages and benefits of each topology have been thoroughly addressed. Finally, a comparison of existing topologies is conducted to determine the optimal topology based on several performance characteristics and the cost evaluation has been presented. This article provides a comprehensive overview of recently developed multilevel inverters and provides a solution for developing the MLIs for future research on renewable energy applications.

Keywords: Multilevel inverters (MLI),Transformer less MLI (TL-MLI),Transformer-based MLI (T-MLI),Cost function (CF),Renewable energy applications

I. INTRODUCTION

Multilevel inverters are utilized generally in the regular applications due to the high voltage capacity and it delivers the multilevel with low composition with least concern in the exchanging gadgets. Contrasted with the traditional single scaffold inverter the multilevel inverter lessens the music due to the multi exchanging. The multilevel inverter produces distinctive voltage levels by shifting the exchanging grouping of the inverter. In multilevel inverter as the quantity of voltage levels expanded the sounds delivered in the yield waveform diminishes moderately. The straightforwardness of fell H connect multilevel inverter has a tendency to utilized as a part of numerous applications discussed in [1].The function and great execution of the anticipated multilevel inverter have been checked by the reenactment aftereffects of a solitary stage nine-level symmetric and 17-level asymmetric multi level inverter and trial consequences of a nine-altitude and 17- stage inverter. Subsequently the recommended structure prompts diminishment of establishment territory and cost and has straightforwardness of control strategy represented in [2].This topology can build the quantity of yield energy stage by utilizing lesser amount of energy electronic gadgets, for example, switch, thyristor family, driver circuit and dc electrical energy sources that prompt decrease in establishment gap and rate of the inverter with various Calculation explained in [3]. Proposed SOP method licenses multilevel inverter to work at a normal gadget changing recurrence constrained to evaluated key recurrence without trading off on consonant twisting are discussed in [4]. This survey considers accomplishing the base aggregate symphonious mutilation (THD) or recurrence biased THD (WTHD) of the stairway -regulated yield voltage of single-stage multilevel inverters are explained in [5].This survey deals with the suitable balance plot has likewise been proposed for low exchanging recurrenceoperation of the proposed topology. In addition, a 15- level inverter with awry source setup has been likewise examined for charge adjust control utilizing the proposed tweak plot is mentioned in [6].Expanding requests for control supplies have added to the number of inhabitants in high recurrence air conditioning (HFAC) control conveyance framework (PDS), and keeping in mind the end goal to build the power limit, multilevel inverters (MLIs) often times filling in as the highrecurrence (HF) source-organize have acquired a conspicuous improvement was discussed in [7].Fell multi level inverter (MLI). Every module is comprised of H-and semi extensions, two detached equivalent dc source and a two directional assistant track. One crutch of the H- connect and the half -connect are hack and the comparing incurable are associated with the two finishes of an equivalent divide dc source are represented in [8].In this survey , it has been outlined the upside of incorporating into the controller plan of a hilter kilter nine-level inverter, when consonant current moderation targets are sought after, a point by point investigation of its non-direct unique conduct. discussed in [9].The commitment can be separated into three sections, specifically, For three-stage lattice associated applications, PV confuses may present uneven provided control, prompting unequal framework current. To illuminate this issue, a control conspire with adjustment pay is additionally proposed. A trial three-stage 7-level fell H-connect inverter has been fabricated using 9 H- connect modules are represented in [9].

II. PROPOSED METHODOLOGY

In this topology is built using the combination of power semiconductor devices. The proposed multilevel inverter topology is shown in Fig 1a. The switches and DC voltage source combination is in parallel with the bypass diode. It has two operating modes. When the switch T1 is on state, voltage appears across the diode D1 is Vdc1. Hence the value of output voltage is 2Vdc

(Vdc1+Vdc2). When the switch T1 is in off state, the bypass diodes are conducts to generate the Vdc output voltage.

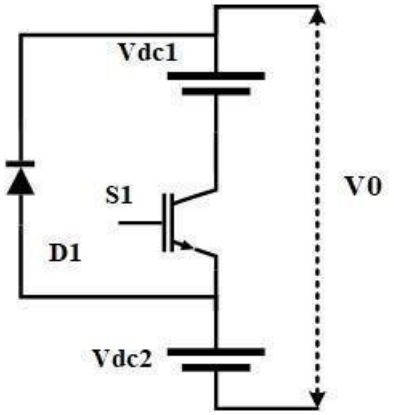

Fig 1a: Basic Structure of proposed topology

For generating the output voltage, the highest number of cascading connection of multilevel inverter levels is needed. When compared to asymmetric inverter, symmetric inverters produce minimum level of the output voltage. Figure1b shows the proposed topology of multilevel inverter for generating a 63-level output voltage. The binary sequence ratio is 1:2:4:8.The desired output voltage level is produced by a combination of H-Bridge inverter and reduced switch configuration. The generalized formula for multilevel inverter configuration is shown in Table I. The proposed topology for generating 63-level output voltage in both positive and negative sequences is shown in Table2.

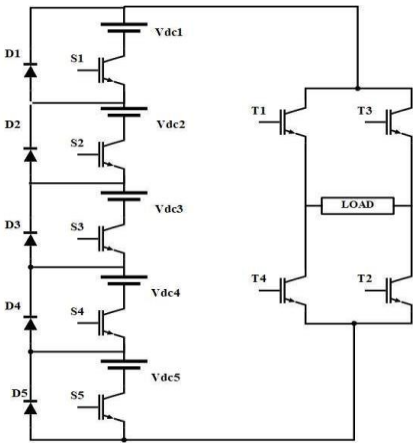

Fig 1b: Proposed Configuration

TABLE I Different parameters used for proposed multilevelinverter

Quantity	**Values**
Dc Sources	2n where n = 0, 1, 2...
Ratio of DC Sources	1:2:4:8
Number of Switches	k + 4
Number of DC Sources	k
Number of Diodes Driver Circuit	k + 4 Number of level2k+1 – 1

III. MODULATION TECHNIQUES

Pulse width modulation is an effective technique for controlling the multilevel inverter output voltage. Normally sinusoidal pulse width modulations are used to achieve the desired output voltage. The proposed topology switches are triggered by using the trapezoidal

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reference with a triangular carrier wave. This technique provides better performance output voltage compared with the sinusoidal pulse width modulation technique. The combination of two slopes and one horizontal line makes the trapezoidal reference waveform. Generally, triangular reference waveform attained by limiting the magnitude value of the waveform. The angle horizontal lineof the waveform will be

$$2\Phi = (1-\sigma)\,\pi \quad (1)$$

Where σ is called as the triangular factor.
If the triangular factor is σ=1, the waveform shape willbe triangular. The shape of the waveform is purely depending on the location of the slope angle (α). Fig 2shows the various angle of slope for the triangular waveform. A mathematical formula for calculating the different slope of a different order is given by

$$A_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} F(\theta)\sin n\theta\, d\theta$$

Where

$$F(\theta) = \begin{cases} \frac{1}{a} & 0 < \theta < 90 \\ 1 & \alpha < \theta < 90 \end{cases}$$

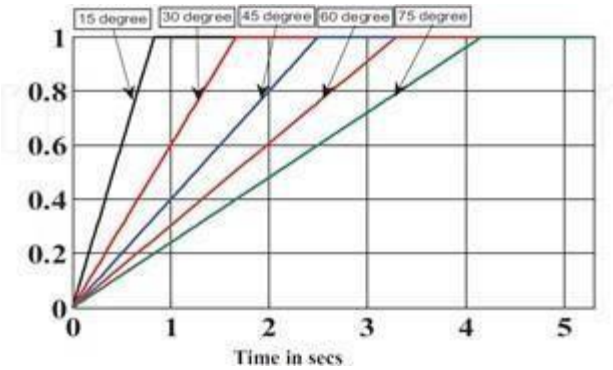


Fig 2: Trapezoidal References of Various slope angle

If the slope angle moves towards 90 degrees, the harmonic order value decreases. Fig 3 shows the different harmonic orders for different slope angles. In this paper, the slope angle will be considered as 60 degrees.

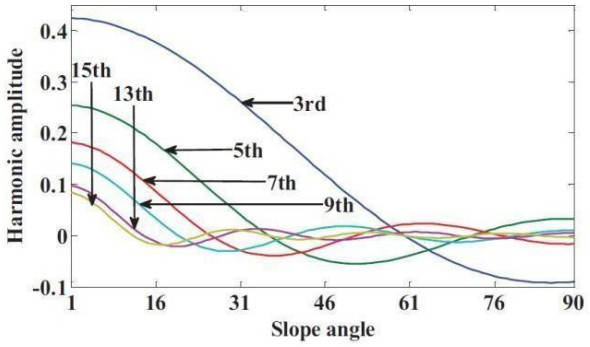


Fig 3: Different harmonic orders for different slope angles

In this paper unipolar reference is considered for generating the switching pulses.

Table II Switching states of the proposed configuration

Switching state	*S1*	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*S9*
$V_{dc}3$	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
$V_{dc}2$	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON
$V_{dc}1$	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	0FF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF
0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
$-V_{dc}1$	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON
$-V_{dc}2$	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON
$-V_{dc}3$	OFF	0FF	ON	OFF	OFF	ON	ON	OFF	OFF

IV. Proposed Simulink model

The proposed topology needs 3 separate DC sources to generate the output voltage, so the separate DC sources are replaced by the photovoltaic panel. In this paper, a 100W solar panel is considered. Fig 4.18 shows the proposed topology integrated with a solar panel.
For a conventional type solar panel integration requires high gain converters and separate MPPT technique for achieving the required output voltage. So, the system will be very bulky and complexity

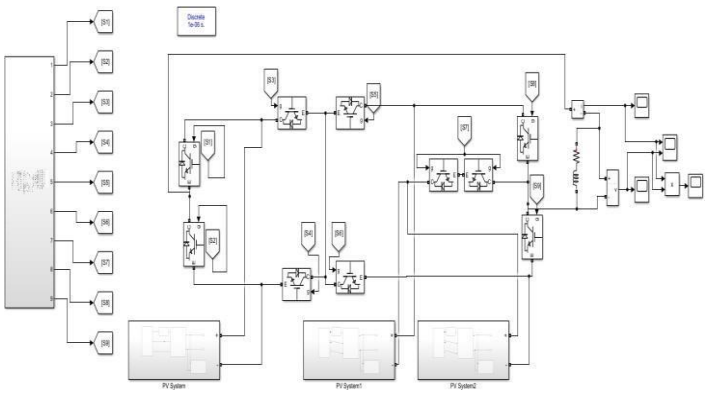


Fig4 Simulink model of proposed method

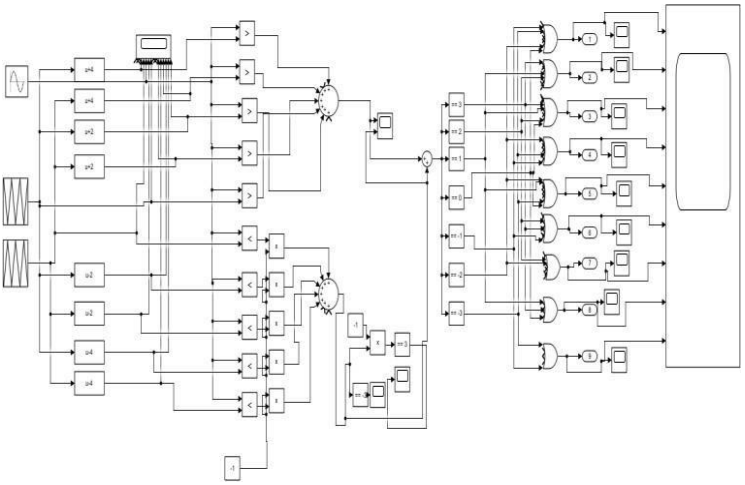


Fig 5 Pulse generator block

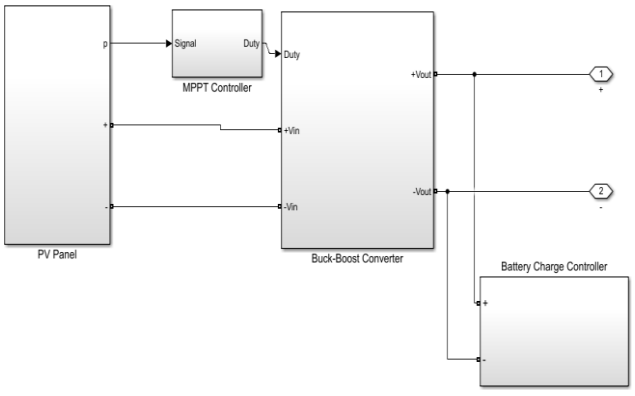


Fig 6 Solar Generation Block

V. Result

Designing of PV based symmetrical inverter system is done using MATLAB simulation. In this work in order to convert DC into AC 7 level inverter is used .By using higher level of inverter switching losses are reduced and the output obtained is in staircase form which is in 7 levels and hence it has less distortion and almost pure sinusoidal waveform can be extracted.

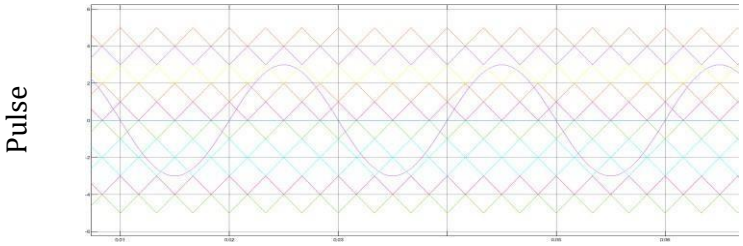
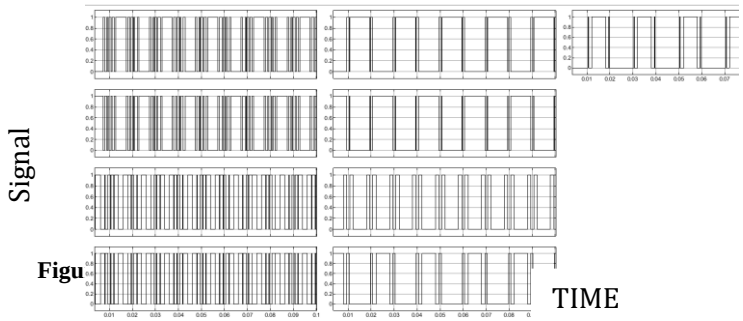


Figure 7 Repeating Logic e and create the PWM pulse



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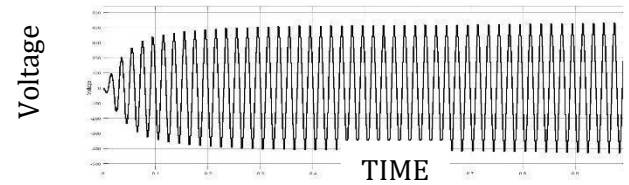

Figure 9 Voltage (V) vs Time (sec) plot

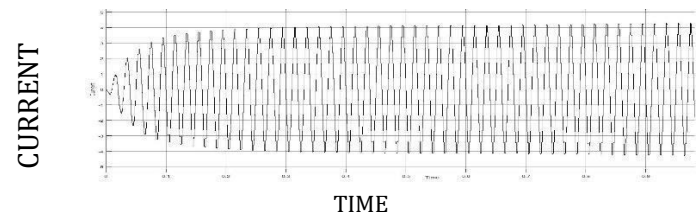

Figure 10: Current (A) vs Time (sec) plot

The figures 9 and 10 show the House hold supply voltage and current respectively fed to the system.

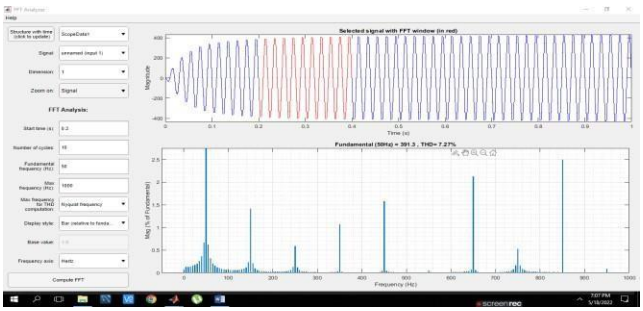

Figure 11 FFT analysis of multi-level inverter

Figure 11 shows the THD value of 7 level inverter whichcomes to 7.27% using FFT analysis.

In Comparison with our base paper Following areTHD value of base paper

Table III % THD of MLI

Level	Percentage of THD Content (%)
3	65.96
5	38.20
7	10.27

Table IV % THD of MLI

Level	Percentage of THD Content (%)
3	51.96
5	27.20
7	7.27

Above table shows that the value of THD is found to be reduced as the number of voltage level of MLI is increased. [30]. Hence the 7-level inverter has least valve of THD as compared to lower levels of MLI. Therefore, it will give more sinusoidal output waveform than the lower levels MLIs.

REFERENCES

[1] Youssef, Mohamed Z., Konrad Woronowicz, Kunwar Aditya, Najath Abdul Azeez, and Sheldon S. Williamson. "Design and development of an efficient multilevel DC/AC traction inverter for railway transportation electrification." IEEE Transactions on power Electronics 31, no. 4 (2015): 3036-3042.

[2] Samadaei, Emad, Mohammad Kaviani, and Kent Bertilsson. "A 13-levels Module (K-Type) with two DC sources for Multilevel Inverters." IEEE Transactions on

Industrial Electronics 66, no. 7 (2018): 5186-5196.

[3] Nallamekala, Kiran Kumar, and KeerthipatiSivakumar. "A fault-tolerant dual three-level inverter configuration for multipole induction motor drive with reduced torque ripple." IEEE Transactions on Industrial Electronics 63, no.3 (2015): 1450-1457.

[4] Jain, Sachin, and VenuSonti. "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems." IEEE Transactions on Industrial Electronics 64, no. 4 (2016): 2865-2875.

[5] Phanikumar, Chamarthi, Jibanesh Roy, and Vivek Agarwal. "A Hybrid Nine-Level, 1-φ Grid Connected Multilevel Inverter With Low Switch Count and Innovative Voltage Regulation Techniques Across Auxiliary Capacitor." IEEE Transactions on Power Electronics 34, no. 3 (2018): 2159-2170.

[6] Reddy, B. Prathap, and SivakumarKeerthipati. "A multilevel inverter configuration for an open-end-

winding pole-phase-modulated-multiphase induction motor drive using dual inverter principle." IEEE Transactions on Industrial Electronics 65, no. 4 (2017): 3035-3044.

[7] Kadam, Abhijit, and Anshuman Shukla. "A multilevel transformerless inverter employing ground connection between pv negative terminal and grid neutral point." IEEE Transactions on Industrial Electronics 64, no. 11 (2017): 8897-8907.

[8] Hasan, MdMubashwar, Ahmed Abu-Siada, Syed Mofizul Islam, and Mohamed SA Dahidah. "A new cascaded multilevel inverter topology with galvanic isolation." IEEE Transactions on Industry Applications 54, no. 4 (2018): 3463-3472.

[9] Zamiri, Elyas, NaserVosoughi, Seyed Hossein Hosseini, Reza Barzegarkhoo, and Mehran Sabahi. "A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components." IEEE Transactions on Industrial Electronics 63, no. 6 (2016): 3582-3594.

[10] Siddique, MarifDaula, SaadMekhilef, Noraisyah Mohamed Shah, AdilSarwar, Atif Iqbal, and Mudasir Ahmed Memon. "A New Multilevel Inverter Topology With Reduce Switch Count." IEEE Access 7 (2019): 58584-58594.

[11] Sheir, Ahmed, Mohamed Z. Youssef, and Mohamed Orabi. "A Novel Bidirectional T-Type Multilevel Inverter for Electric Vehicle Applications." IEEE Transactions on Power Electronics 34, no. 7 (2018): 6648-6658.

[12] Zeng, Jun, Jialei Wu, Junfeng Liu, and HuafangGuo. "A quasi-resonant switched-capacitor multilevel inverter with self-voltage balancing for single-phase high- frequency ac microgrids." IEEE Transactions on Industrial Informatics 13, no. 5 (2017): 2669-2679.

[13] Zhao, Hui, Tian Jin, Shuo Wang, and Liang Sun. "A real-time selective harmonic elimination based on a transient- free inner closed-loop control for cascaded multilevel inverters." IEEE Transactions on Power Electronics 31, no.2 (2015): 1000-1014.

[14] Nguyen, Nho-Van, Tam-KhanhTu Nguyen, and Hong-Hee Lee. "A reduced switching loss PWM strategy to eliminate common-mode voltage in multilevel inverters." IEEE Transactions on Power Electronics 30, no. 10 (2014): 5425-5438.

[15] Karasani, Raghavendra Reddy, Vijay BhanujiBorghate, Prafullachandra M. Meshram, HiralalMurlidharSuryawanshi, and SidharthSabyasachi. "A three-phase hybrid cascaded modular multilevel inverter for renewable energy environment." IEEE Transactions on Power Electronics 32, no. 2 (2016): 1070-1087.

[16] Hasan, MdMubashwar, Ahmed Abu-Siada, and Mohamed SA Dahidah. "A three-phase symmetrical dc- link multilevel inverter with reduced number of dc sources." IEEE Transactions on Power Electronics 33, no. 10 (2017): 8331-8340.

Nair, Viju, K. Gopakumar, and Leopoldo G. Franquelo. "A very high resolution stacked multilevel inverter topology for adjustable speed drives." IEEE Transactions on Industrial Electronics 65, no. 3 (2017): 2049-2056.

[17] Ruderman, Alex. "About voltage total harmonic distortion for single-and three-phase multilevel inverters." IEEE Transactions on Industrial Electronics 62, no. 3 (2014): 1548-1551.

[18] Hota, Arpan, Sachin Jain, and Vivek Agarwal. "An optimized three-phase multilevel inverter topology with separate level and phase sequence generation part." IEEE Transactions on Power Electronics 32, no. 10 (2017): 7414- 7418.

[19] Grandi, Gabriele, JelenaLoncarski, and ObradDordevic. "Analysis and comparison of peak-to-peak current ripple in two-level and multilevel PWM inverters." IEEE Transactions on Industrial Electronics 62, no. 5 (2014): 2721-2730.

[20] Sonti, Venu, Sachin Jain, and Subhashish Bhattacharya. "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid- connected cascaded multilevel inverter." IEEE Transactions on Power Electronics 32, no. 2 (2016): 1156-1169.

[21] Lee, June-Seok, Hyun-Woo Sim, Juyong Kim, and Kyo-Beum Lee. "Combination analysis and switching method of a cascaded H-bridge multilevel inverter based on transformers with the different turns ratio for increasing the voltage level." IEEE Transactions on Industrial Electronics 65, no. 6 (2017): 4454-4465.

[22] Shuvo, Shuvangkar, Eklas Hossain, Tanveerul Islam, AbirAkib, SanjeevikumarPadmanaban, and MdZiaur Rahman Khan. "Design and Hardware Implementation Considerations of Modified Multilevel Cascaded H- Bridge Inverter for Photovoltaic System." Ieee Access 7 (2019): 16504-16524.

[23] Hsieh, Cheng-Han, Tsorng-Juu Liang, Shih-Ming Chen, and Shih-Wen Tsai. "Design and implementation of a novel multilevel dc–ac inverter." IEEE Transactions onindustry applications 52, no. 3 (2016): 2436-2443.

[24] Behara, Siva, N. Sandeep, and Udaykumar R. Yaragatti. "Design and Implementation of Transformer-Based Multilevel Inverter Topology WithReduced Components."

IEEE Transactions on Industry Applications 54, no. 5 (2018): 4632-4639.

[25] Nguyen, Tam-KhanhTu, Nho-Van Nguyen, and Nadipuram Ram R. Prasad. "Eliminated common-mode voltage pulsewidth modulation to reduce output current ripple for multilevel inverters." IEEE Transactions on Power Electronics 31, no. 8 (2015): 5952-5966.

[26] Susheela, Nunsavath, Peddapalli Satish Kumar, and Sushil Kumar Sharma. "Generalized Algorithm of Reverse Mapping Based SVPWM Strategy for Diode-

capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches." IEEE Transactions on Power Electronics 31, no. 8 (2015): 5604-
5617.

[29] Huang, Qingyun, Alex Q. Huang, Ruiyang Yu, Pengkun Liu, and Wensong Yu. "High-Efficiency and High-Density Single-Phase Dual-Mode Cascaded Buck–Boost Multilevel Transformerless PV Inverter WithGaN AC Switches." IEEE Transactions on Power Electronics 34, no. 8 (2018): 7474-7488.

[30] Jacobina, CursinoBrandão, Alexandre Cunha Oliveira, Gregory Arthur de Almeida Carlos, and MaurícioBeltrão de RossiterCorrêa. "Hybrid modular multilevel DSCC inverter for open-end winding induction motor drives." IEEE Transactions on Industry Applications 53, no. 2 (2016): 1232-1242.

[31] Dhanamjayulu, C., and S. Meikandasivam. "Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads." IEEE Access 6 (2017): 738-746.

[32] Chang, Fengqi, Olga Ilina, Markus Lienkamp, and Leon Voss.

[33] Yadav, Apurv Kumar, K. Gopakumar, LoganathanUmanand, Kouki Matsuse, and Hisao Kubota. "Instantaneous Balancing of Neutral-Point Voltages for Stacked DC-Link Capacitors of a Multilevel Inverter for Dual-Inverter- Fed Induction Motor Drives." IEEE Transactions on Power Electronics 34, no. 3 (2018): 2505- 2514.

[34] Mohapatra, SoumyaRanjan, and Vivek Agarwal. "Model Predictive Controller with Reduced Complexity for Grid Tied Multilevel Inverters." IEEE Transactions on Industrial Electronics (2018).

[35] Raman, S. Raghu, KaWai Eric Cheng, and Yuanmao Ye. "Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution." IEEE Transactions on Power Electronics 33, no. 7 (2017): 5937- 5948.

[36] Amamra, Sid-Ali, Kamal Meghriche, AbderrezzakCherifi, and Bruno Francois. "Multilevel inverter topology for renewable energy grid integration." IEEE Transactions on Industrial Electronics 64, no. 11 (2016): 8855-8866.

[37] Wang, Lei, Q. H. Wu, and Wenhu Tang. "Novel cascaded switched-diode multilevel inverter for renewable energy integration." IEEE Transactions on

Clamped Multilevel Inverters." IEEE Transactions on IndustryApplications 54, no. 3 (2018): 2425-2437.

[27] Mohan, Deepu, Xinan Zhang, and Gilbert Hock Beng Foo. "Generalized DTC strategy for multilevel inverter fed IPMSMs with constant inverter switching frequency and reduced torque ripples." IEEE Transactions on Energy Conversion 32, no. 3 (2017): 1031-1041.

[28] Barzegarkhoo, Reza, Hossein MadadiKojabadi, ElyasZamiry, NaserVosoughi, and Liuchen Chang. "Generalized structure for a single phase switched- Energy Conversion 32,no. 4 (2017): 1574-1582.

[38] Siddique, MarifDaula, SaadMekhilef, Noraisyah Mohamed Shah, and Mudasir Ahmed Memon. "Optimal design of a new cascaded multilevel inverter topology with reduced switch count." IEEE Access 7 (2019): 24498- 24510.

[39] Sahoo, Saroj Kumar, and Tanmoy Bhattacharya. "Phase-shifted carrier-based synchronized sinusoidal PWM techniques for a cascaded H-bridge multilevel inverter." IEEE Transactions on Power Electronics 33, no. 1 (2017): 513-524.