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An Efficient Reconfigurable CAM and IMC Framework using Multistate RRAM Devices

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Abstract - The rapid growth of data-intensive applications has created a strong need for high-speed and energy-efficient memory architectures, as conventional CMOS-based CAM and von Neumann systems face limitations such as high power consumption, poor scalability, and data transfer latency. To overcome these issues, this work proposes a reconfigurable framework that integrates Content Addressable Memory (CAM) and In-Memory Computing (IMC) using multistate Resistive Random Access Memory (RRAM). By utilizing the multi-level resistance states of RRAM, the proposed design enables both data storage and computation within the same memory array, supporting parallel search and processing operations. This reduces data movement, improves computational speed, lowers energy consumption, enhances storage density, and provides adaptable functionality for different computing tasks.

Index Terms—RRAM, multistate, reconfigurable memory, content-addressable memory, in-memory computing.

1.INTRODUCTION

The growing demand for data-centric applications such as AI, machine learning, and big-data analytics requires high-speed and energy-efficient computing systems. Conventional von Neumann architectures suffer from the memory bottleneck, where frequent data transfer between processor and memory increases latency, power consumption, and reduces performance. In-Memory Computing (IMC) helps overcome this issue by performing computation directly within memory. Among emerging memory technologies, multistate Resistive Random Access Memory (RRAM) is highly promising due to its non-volatility, low power consumption, high speed, scalability, and ability to store multiple bits per cell.

Content Addressable Memory (CAM) enables fast parallel data search but traditional CMOS-based CAM designs consume high power and occupy large area. To address these limitations, this work proposes a reconfigurable framework that integrates CAM and IMC using multistate RRAM, enabling both search and computation within the same memory array while improving performance, reducing power consumption, and increasing storage efficiency.

2. LITERATURE SURVEY

The literature survey shows that RRAM, CAM, and IMC are promising technologies for high-speed and energy-efficient computing. Multistate RRAM provides high storage density, low power consumption, and non-volatility, while existing studies improve its performance through better programming, sensing, and hybrid memory techniques. However, challenges such as variability, endurance, sensing complexity, and power consumption still remain.

Most existing works study RRAM, CAM, and IMC separately rather than as a unified system. There is limited research on integrating multistate RRAM with both CAM and IMC in a reconfigurable and power-efficient manner. This creates the need for a new architecture that combines these technologies with effective power management to achieve better performance, reliability, and energy efficiency.

3. EXISTING METHOD

The existing Content Addressable Memory (CAM) architecture is mainly implemented using conventional CMOS- or SRAM-based circuits for high-speed parallel data search. In this system, each CAM cell stores data and compares it with the input search word simultaneously using bit lines, search lines, and match lines. During operation, the match line is precharged, and if the stored data matches the search input, it remains charged; otherwise, it discharges, indicating a mismatch. This parallel comparison makes CAM suitable for applications such as networking, cache memory, and pattern recognition. To improve density and reduce power, RRAM-based CAM has been introduced, where data is stored as resistance levels instead of voltage levels. RRAM-based CAM supports non-volatile storage, fast switching, and multistate operation, allowing multiple bits to be stored in a single cell and enabling higher memory density with lower area and power consumption.

However, both conventional and existing multistate RRAM-based CAM architectures still face several limitations. SRAM-based CAM suffers from high power consumption, large transistor count, reduced scalability, and leakage issues, while RRAM-based CAM introduces challenges such as resistance variability, sensing complexity, sneak path currents, and difficulty in accurately programming and distinguishing multiple resistance states. These issues affect reliability, accuracy, and large-scale integration, especially for modern applications such as artificial intelligence, in-memory computing, and real-time data processing. Therefore, a more efficient and improved system is needed to enhance sensing accuracy, reduce variability and noise effects, improve resistance state stability, and achieve better power efficiency, scalability, and overall performance for next-generation CAM and computing architectures.

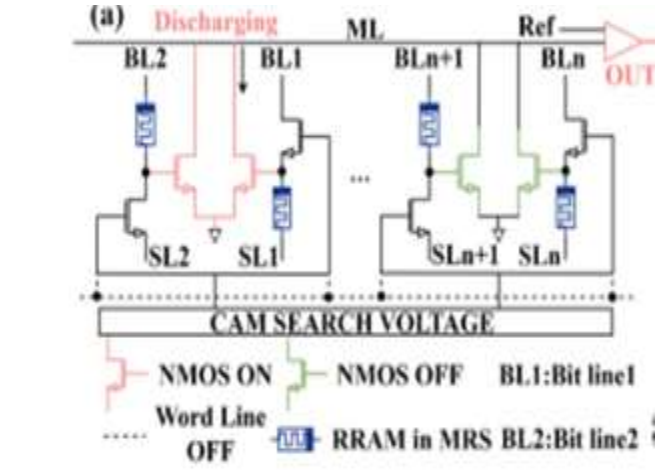

Fig. 1: 1-bit mismatch mechanism structure diagram when performing analog voltage search based on an array of 4T2R cells.

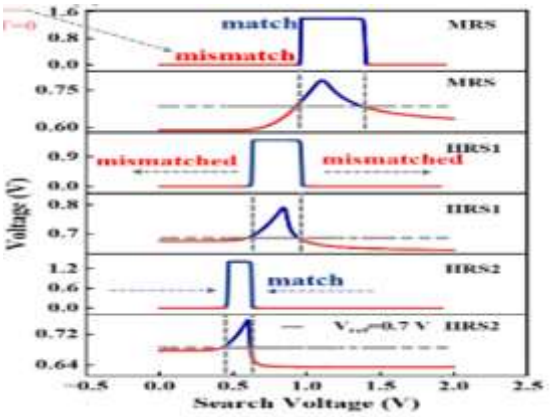

Fig. 2: The change of ML line potential and matching as the search voltage is scanned from 0V to 2.

4. PROPOSED METHOD

The proposed system integrates CAM and IMC using multistate RRAM and power gating to reduce power, latency, and sensing complexity in conventional CAM designs. Multistate RRAM enables high-density storage and parallel in-memory comparison, while match-line based sensing ensures fast operation. A PMOS sleep transistor minimizes leakage power during standby. Overall, the design achieves a high-speed, low-power, and scalable architecture suitable for modern data-intensive applications.

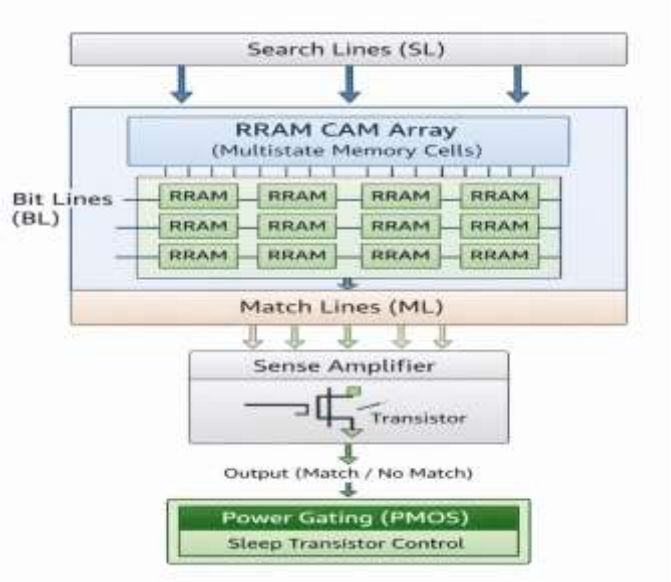

Fig. 4: Architecture of Multistate RRAM CAM with Sense Amplifier and Power Gating.

The fig. 4 illustrates the proposed multistate RRAM-based CAM architecture with sense amplifier and power gating. The search lines (SL) provide the input data to the RRAM CAM array, where multistate RRAM cells store and compare data in parallel. The bit lines (BL) are used to access and manage the stored information within the array, while the match lines (ML) indicate whether the input matches the stored data in each row. The match line outputs are then sent to a sense amplifier, which detects the match or mismatch condition and produces the final output (match / no match). To improve energy efficiency, a PMOS-based power gating block with sleep transistor control is included, which helps reduce leakage power by disconnecting inactive circuit blocks during standby mode.

5. RESULTS

Table 1: Extension Comparison Table

Technology	45nm	90nm
MOS count	15	15
Delay (sec)	$59.36e^{-12}$	$38.69e^{-12}$
Power (W)	$7.247e^{-6}$	$8.786e^{-6}$

CONCLUSION

Power gating is an important low-power design technique used in modern VLSI circuits to reduce leakage power, especially in deep-submicron technologies. It works by disconnecting inactive circuit blocks from the power supply using sleep transistors, such as PMOS header or NMOS footer transistors, which allow normal operation in active mode and isolate the circuit in standby mode to minimize leakage current. In addition to reducing standby power, power gating improves thermal management, enhances reliability, and extends device lifespan by lowering unnecessary heat generation. It can be applied at different levels of granularity and may include state retention techniques to preserve circuit data during sleep mode. Although it introduces some area overhead and wake-up delay, proper design can minimize these effects, making power gating a highly effective approach for improving energy efficiency in applications such as CAM, IMC, smartphones, IoT devices, wearable systems, and other next-generation low-power electronics.

DISCUSSION

Power gating is a highly effective technique for reducing leakage power in modern VLSI circuits, particularly as device dimensions continue to shrink in deep-submicron technologies. By using sleep transistors such as PMOS header or NMOS footer switches, inactive circuit blocks can be temporarily disconnected from the power supply during standby mode, thereby minimizing leakage current while still allowing normal operation during active mode. This not only reduces standby power consumption but also improves thermal performance, enhances circuit reliability, and extends device lifetime by lowering unnecessary heat dissipation. Power gating can be implemented at different levels depending on design requirements and can also be combined with state retention methods to preserve important data during low-power states. Although it introduces certain challenges such as additional area and wake-up delay, these can be effectively managed through careful design and optimization. As a result, power gating has become a key low-power strategy in advanced electronic systems such as CAM, IMC, IoT devices, smartphones, and other energy-efficient next-generation applications.

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