Analysis of Low power and high performance of mixed losgic line

Prof. Sachin Singh[1], Prof. Rakesh Mishra[2], Ekta Sahu[3]
[1]*Electronics &Communication Deptt , SRIST Jabalpur*
[2]*Electronics &Communication Deptt , SRIST Jabalpur*
[3]*Electronics &Communication Deptt , SRIST Jabalpur*

Abstract -—The decoders are widely used in the logical circuits, data transfer circuits and analog to digital conversions. A mixed logic design methods for the line decoders are used to combining the transmission gate logic, pass transistor logic, and complementary metal-oxide semiconductor (CMOS) technology provides desired operation and performance. A novel topology is presented for the 2 to 4 decoder requires a fourteen transistor topology aiming on reducing the transistor count and operating power and a fifteen transistor topology aiming on high power and low delay performance. The standard and inverting decoders are designed in each of the case, gives a total of four new designs circuits. All the proposed decoders have compact transistor count compared to their conservative CMOS technologies. Finally, a variety of proposed designs present a noteworthy improvement in operating power and propagation delay, outperforming CMOS in almost all the cases.

Key Words:Decoders, Mixed Logic design , Power and Delay Optimization I

1.*INTRODUCTION*

The CMOS technology is widely used in the Integrated Circuit design which includes starting from basic digital logic gates to a System on Chip (SoC)[2]. The complementary metal oxide semiconductor (CMOS) technology uses both n-channel enhancement mode metal oxide semiconductor field effect transistor (MOSFET) and p-channel enhancement mode MOSFET also NMOS transistor used as pull down network and PMOS transistor is used as pullup network to achieve the better fan-in and fanout capabilities. The CMOS logic circuits withstand against the different voltage scaling, it allows transistor channel sizing to a nanotechnology so that this technology can achieve high speed of operation as well as low power dissipation [3]. The pass transistor logic (PTL) was introduced in early 90's and different design methods are presented [4] to [6], targeting to generate other possibilities to achieve the high speed and occupies less area on the die by applying the inputs directly to the gates of the Transistors and drain –source terminals of the MOSFET. The transmission gate logic designs used either NMOS or PMOS transistors that are connected parallel pairs where as the pass transistor designs uses individual PMOS and NMOS transistors. The Decoders are widely used in the all digital circuits, input and output circuits, data transmission modules, memory devices and all fundamental digital circuits.

2. *DESIGN OF MIXED LOGIC CIRCUITS*

A. Conventional Design –

The fundamental digital module is the decoder which decodes the coded input which is generally used in the all types of memory devices.Most common decoder circuit is an n input to 2n outputbinary decoder. In the conventional design the CMOS technology is used to design the logic of any application.

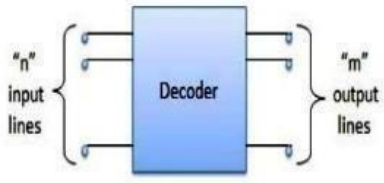

Fig.2.Block diagram of Decoder.

B. Pass Transistor Logic-

In electronics, pass transistor logic(PTL) describes several logic families used in the design of integrated circuits. It

reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance.

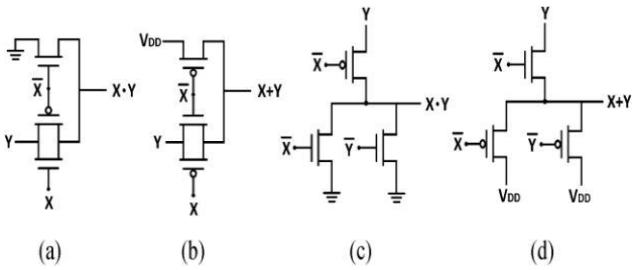

Fig. 2(B). Logic AND as well as OR Gates Circuits (3-transistor). (a) Transmission Gate Logic AND gate. (b) Transmission Gate Logic OR gate. (c) Dual Value Logic AND gate. (d) Dual Value Logic OR gate.

The above fig.2(B) (a) shows a transmission gate logic AND gate which operates when both X and Y are logic High [H,H] then only the output gives the logic high value otherwise the output is logic zero value. Similarly fig 2(B). (b) shows the OR gate which operate when either X or Y are at logic high then the output logic high otherwise the output is logic zero. Both the cases the circuits require only one transmission gate and one NMOS transistor. Fig 2(B) .(c),(d) shows dual value logics of the AND gate and OR gate which are required only 3-transistors when compared to conventional CMOS 6-transistors design.

C. Transmission Gate Logic –

The transmission gate logic has the advantage of maintaining the good output voltage value over the pass transistor logic that is why transmission gates are widely used. In the proposed design uses the transmission gate logic to realize the 14-transistor low power and low power inverted design, 15-transistor high power and high power inverted decoder designs to achieve the low power, high performance and less die area.

D. Mixed Logic Design-

In this mixed logic design technique combines the CMOS, PTL, and DVL logics to achieve the low operating power, low power dissipation, minimal die area, and high performance. In the proposed design uses mostly transmission gate logic and CMOS technologies to achieve the fundamental digital logic gates and 14-transistors low power and low power inverted designs,15-transistors high power and high power inverted designs to get the 2 to 4 decoders.

3. *PROPOSED ARCHITECTURE*–

PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed-topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results. We implemented four 4–16 decoders by using the four new 2–4 as pre decoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies Derived From This Combination Are The following:4–16LP[Fig.3(a)],which combinestwo2–4LPIpre decoderswithaNOR-basedpostdecoder;4–16HP[Fig.3(b)], which combines two 2–4HPI pre decoders with a NOR based post decoder; 4–16LPI [Fig. 3(c)], which combines two 2–4LP pre decoders with a NAND-based post decoder; and, finally, 4– 16HPI [Fig. 3(d)], which combines two 2–4HPpredecoders with a NAND-based post decoder. The “LP” topologies have a total of 92 transistors, while the “HP” ones have 94, as opposedto104 with pure CMOS.

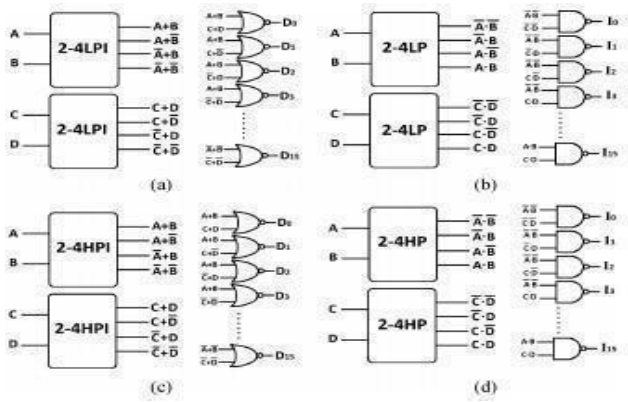

Figure. 3 New 4–16 line decoders. (a) 4–16LP. (b) 4–16LPI. (c) 4–16HP. (d) 4– 16HPI

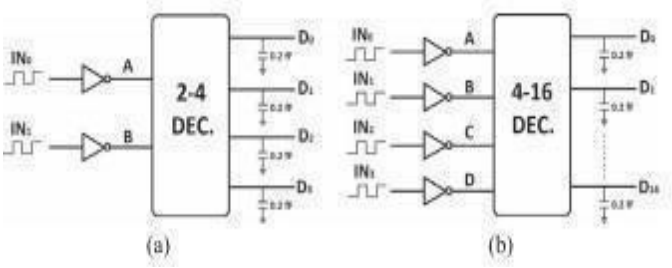

Figure. 3.1Simulation setup regarding input/output loading conditions.(a) 2–4 decoders.(b) 4–16 decoders.

We Perform A Variety Of BSIM4-based spice simulations on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional CMOS. The circuits are implemente dusinga32nm predictive technology model for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect [9]. For fair and unbiased comparison we use unit-size transistors exclusively (Ln=Lp=32nm,Wn= Wp = 64 nm) for all decoders.

4. *CONCLUSIONS*

This brief has presented an effective blended rationale plan for decoder circuits, joining TGL, DVL and static CMOS. By utilizing this approach, we created four new 2–4 line decoder geographies, in particular 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer diminished semiconductor tally and improved force defer execution comparable to ordinary CMOS decoders. Besides, four new 4–16 line decoder geographies were introduced, to be specific 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, acknowledged by utilizing the blended rationale 2-4 decoders as pre disentangling circuits, joined with post decoders actualized in static CMOS to give driving ability. An assortment of near flavor reenactments was performed at 32 nm, checking, as a rule, an unmistakable preferred position for the proposed plans. The 2–4LP and 4–16LPI geographies are generally appropriate for applications where region and force minimization is of essential concern.

REFERENCES

1. M. Suzuki et al., “A 1.5 ns 32b CMOS ALU in double pass-transistor logic,” in Proc. IEEE Int. Solid-State Circuits Conf., 1993, pp.90–91.

2. X. Wu, “Theory of transmission switches and its application to design of CMOS digital circuits,” Int. J. Circuit Theory Appl., vol. 20, no. 4, pp. 349–356, 1992. V.G. Oklobdzija and B. Duchene, “Pass-transistor dual value logic for low-powerCMOS,” in Proc. Int. Symp. VLSI Technol., 1995, pp. 341–344.

3. A. K. Mishra, D. P. Acharya, and P. K. Patra, “Novel design technique of address decoder for SRAM,” Proc. IEEE ICACCCT, 2014, pp.1032–1035.

4. M. A. Turi and J. G. Delgado-Frias, “Decreasing energy consumption in address decoders by means of selective precharge schemes,” Microelectron.J., vol. 40, no. 11, pp. 1590–1600,2009.

5. D. Markovic, B. Nikoli ´ c, and V. G. Oklobdžija, “A general method in syn- ´ thesis of pass-transistor circuits,” Microelectron. J., vol. 31, pp. 991–998,2000.

6.V. Bhatnagar, A. Chandani, and S. Pandey, “Optimization of row decoder for128× 128 6T SRAMs,” in Proc. IEEE Int. Conf. VLSI-SATA, 2015, pp. 1–4.

7. R. Zimmermann and W. Fichtner, “Low-power logic styles: CMOS versus pass transistor logic,” IEEE J. Solid State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

8. N. H. E. Weste and D. M. Harris, CMOS VLSI Design, a Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley,2011.

9. [Online]. Available: http://ptm.asu.edu/

10. M Madhusudhan Reddy, Krishna Veni Challa, B Srinivasa Raja, "An Energy Efficient Static Address Decoder for High-Speed Memory Applications", 2022 7th International Conference on Communication and Electronics Systems (ICCES), pp.50-53, 2022.

11. Alok Kumar Mishra, Shubham Sinha, D.D.V Subbarao, D. Vaithiyanathan, Baljit Kaur, "Study and Implementation of Low Power Decoder using DVL and TGL Logic", 2021 IEEE Madras Section Conference (MASCON), pp.1-6, 2021.