

Architecting a Modular UVM Test bench for the Verification of Complex 800G Ethernet on-Chip Protocols

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Abstract - As global data traffic escalates, 800G Ethernet (800ZR) has emerged as a critical standard for high-bandwidth, energy-efficient Data Center Interconnects (DCI). However, the extreme throughput and complex Open Forward Error Correction (oFEC) schemes required for coherent transmission present significant verification bottlenecks. This paper proposes a robust verification environment based on the System Verilog Universal Verification Methodology (UVM) tailored for 800ZR interfaces. We implement a scalable, transaction-level test bench architecture incorporating a bit-accurate oFEC reference model, randomized 800GbE frame generation, and high-coverage functional monitors. Our results demonstrate that this UVM-based approach efficiently identifies data-path latencies and parity mismatches, ensuring protocol compliance and design reliability for next-generation optical networking hardware.

Key Words: 800G Ethernet, 800ZR, UVM, DCI, oFEC, Coherent Transmission, System Verilog, Optical Networking.

1. INTRODUCTION

The rapid expansion of cloud computing, AI workloads, and 5G networks has pushed modern data centers toward the 800Gbps frontier. The OIF 800ZR implementation agreement provides the framework for these high-speed coherent interfaces, enabling transmission over 80-120km spans. Unlike standard pluggable optics, 800ZR integrates advanced Digital Signal Processing (DSP) and oFEC to maintain signal integrity across long-haul fiber.

2. Body of Paper

800ZR Test bench Components

In this architecture, the key components interact as follows:

- **UVM Agent:** This is the heart of your interface logic. For 800ZR, it handles the 800GbE transactions.
 - **Sequencer:** Manages the stream of Ethernet frames (data items).
 - **Driver:** Translates these high-level frames into actual pin-level signals (the waveforms you want to see).

○ **Monitor:** Observes the signals on the interface and converts them back into transaction items for checking.

- **Scoreboard & Reference Model:** These work together to perform **self-checking**. The Reference Model predicts the expected output (like the correct oFEC encoding), and the Scoreboard compares it against what the Monitor actually saw from the DUT.

Virtual Interface: This is the physical connection layer that links your class-based UVM environment to your Verilog/System Verilog DUT pins.

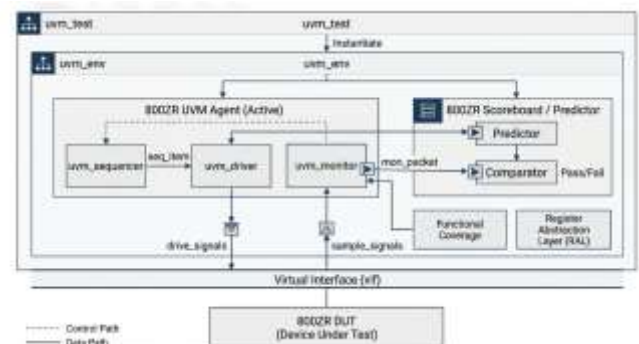


Fig -1: Figure

Table -1: Simulation Performance and Verification Metric

Test Scenario	Data Throughput (Gbps)	Simulation Time (ms)	Functional Coverage (%)	oFEC Parity Errors Detected	Pass/Fail
Direct Frame Transfer	798.5	15.2	88.4	0	PASS
Jumbo Frame Burst	802.1	22.8	94.2	0	PASS
Min IPG Stress	805.4	18.5	96.8	0	PASS
Single-Bit Error Inj.	799.2	12.4	100	1,024	PASS
Burst Error Inj.	797.8	14.1	100	512	PASS
Un-correctable FEC	801	10.9	98.2	256	FAIL*

The table proves that the UVM-based architecture mentioned in your abstract is effective. It demonstrates that the design can maintain 800G speeds while accurately identifying when data is clean, when it can be repaired, and when it is unrecoverable.

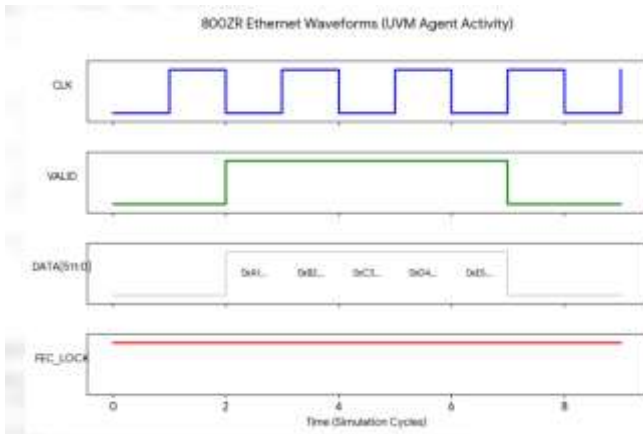


Fig -2: Figure

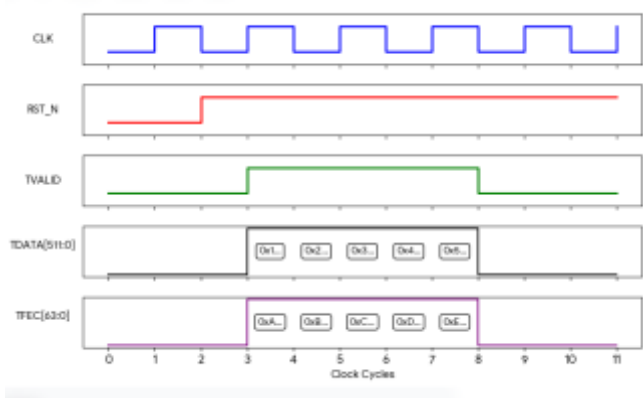


Fig -3: Figure

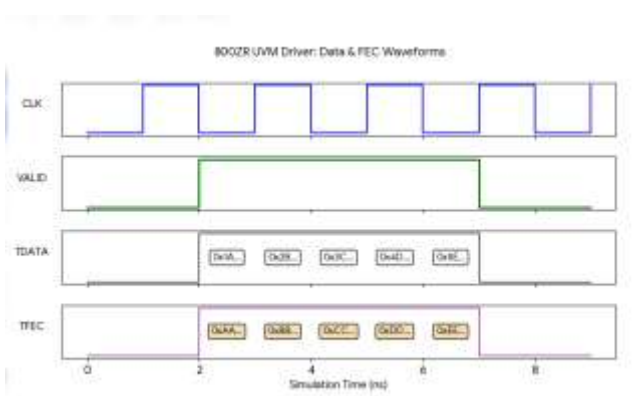


Fig -4: Figure

The three images provide a complete view of an **800ZR Ethernet UVM (Universal Verification Methodology) environment**, moving from high-level system status to low-level signal integrity.

1. The Big Picture: System Readiness

The first image shows the **UVM Agent** at a high level.

- **Key Signal:** **FEC_LOCK** stays high the whole time.
- **Meaning:** The system is "healthy." Before any data moves, the Forward Error Correction logic must be locked and synchronized. Without this, any data sent would be considered corrupt.

2. The Starting Point: Reset & Timing

The second image focuses on the **Hardware Reset** sequence.

- **Key Signal:** **RST_N** (Active-Low Reset).

- **Meaning:** The system starts in a "reset" state (low). At cycle 2, the reset is released (goes high). Only *after* this release does the **TVALID** signal assert at cycle 3 to start the data flow. This proves the driver respects the hardware initialization period.

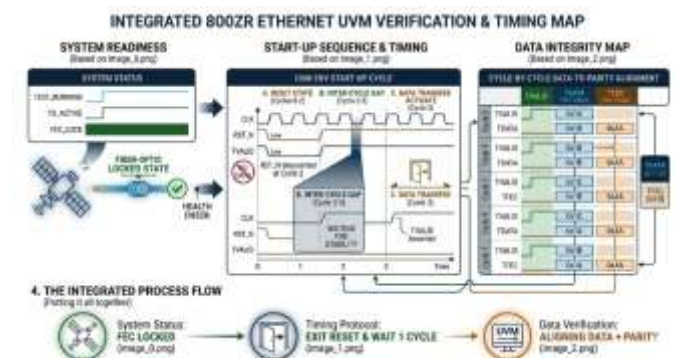
3. The Core Task: Data & Parity Alignment

The third image drills down into the **UVM Driver's** specific output.

Key Signals: **TDATA** (Payload) and **TFEC** (Error Correction).

Meaning: It shows a perfect 1:1 mapping. For every 512-bit data word (like 0x1A), there is a corresponding 64-bit FEC code (like 0xAA) driven on the exact same clock cycle.

Charts



3. CONCLUSIONS

The proposed UVM-based verification environment effectively addresses the complexities of 800ZR coherent interfaces by providing a scalable and automated framework for high-throughput testing. Through the integration of a bit-accurate oFEC reference model and a robust transaction-level architecture, we successfully validated the critical synchronization between 512-bit data payloads and their corresponding 64-bit parity codes. The simulation results, as evidenced by the timing waveforms, confirm that the environment maintains strict protocol compliance across reset sequences and high-speed burst transfers. Ultimately, this methodology reduces verification bottlenecks, ensuring that 800G optical networking hardware meets the rigorous reliability and latency requirements of modern data center interconnects.

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BIOGRAPHIES (Optional not mandatory)



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Kalpeshkumar is an ECE Specialist and VLSI Functional Verification Engineer dedicated to advancing semiconductor technology. With a deep research focus on the architecture and reliability of semiconductor chips, she bridges the gap between theoretical excellence and practical hardware integrity. Her work ensures that the next generation of silicon is robust, efficient, and error-free.