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Area and Power Optimized 8×8 Truncated and 8×8 Array Multiplier Using Hybrid 1-Bit Full Adders

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Abstract: Multiplication is a fundamental operation in digital signal processing (DSP), neural network accelerators, and embedded systems. Conventional parallel multipliers offer high performance but incur considerable area and power overhead, especially in deep submicron VLSI technologies. Truncated multipliers and Array multipliers are reducing hardware cost by omitting least significant partial product columns but introduce accuracy degradation. This paper proposes an area and power optimized 8×8 truncated and 8×8 array multiplier architectures employing hybrid 1-bit full adders implemented 90nm CMOS technology. The hybrid full adder utilizes a combination of transmission-gate and pass-transistor logic to achieve full-swing outputs with reduced transistor count. Variable-correction logic is integrated to compensate for removed partial products, enhancing accuracy while maintaining low hardware cost. Tanner EDA simulations demonstrate that the proposed architectures are achieve up to 27.2% area reduction and up to 57% power savings for the 1-bit adder, along with 9% power savings for the truncated multiplier compared to conventional full-adder-based designs. The proposed design is therefore well suited for DSP cores, filtering engines, and energy-efficient computing units.

Keywords: Hybrid Full Adder, Truncated Multiplier, Array Multiplier, Variable Correction Method, Low-Power VLSI, DSP Hardware Optimization.

1. INTRODUCTION

As CMOS technology continues scaling into nanometre regimes, reducing energy consumption and silicon footprint remains critical for portable electronics, signal-processing accelerators, and high-performance computing platforms. A significant portion of computational workload in these systems arises from arithmetic operations especially addition and multiplication. Full adders form the fundamental building block of arithmetic units; therefore, optimizing their performance directly benefits larger data paths such as multipliers.

Conventional n×n multipliers generate a 2n-bit output by summing n partial product rows. However, for many DSP applications, such high precision is unnecessary, and storing full-precision results increase register and memory overhead. Truncated multipliers provide an attractive alternative by generating only the most significant bits of the product, thereby reducing delay, area, and power at the cost of manageable accuracy loss.

Prior studies have explored various adder architectures for truncated multipliers, including ripple-carry, carry-select, and carry-save adders. However, these designs are limited by high transistor count and increased switching power. Hybrid full adders, consisting of XOR/XNOR logic constructed using a mix of transmission gates and pass-transistor logic, offer superior energy efficiency and full-swing operation even at low supply voltages. Motivated by these strengths, this work employs a hybrid full adder to construct an efficient truncated multiplier and array multiplier optimized by using 90nm CMOC Technologies.

2. HYBRID FULL ADDER DESIGN

The hybrid full adder is organized into two functional blocks: (i) carry generation and (ii) sum generation. Both blocks utilize pass-transistor and transmission-gate logic to reduce transistor usage while preserving full voltage swing.

2.1 Carry Generation Logic

Carry generation employs an AND-OR structure constructed using transmission-gate multiplexers. Depending on the input control, the module efficiently selects AND or OR logic to compute the carry-out. This mixed logic style ensures:

- Reduced short-circuit power,
- Minimal stacking of transistors, and
- Improved delay characteristics.

2.2 Sum Generation Logic

The sum output is generated using two cascaded XOR stages. Each XOR is implemented using pass transistors and transmission gates, satisfying required voltage-level conditions for correct operation. The architecture ensures full-swing XOR output even at reduced supply voltages. The hybrid adder, comprising only 22 transistors, ensures lower parasitic capacitance, leading to reduced propagation delay and dynamic power consumption.

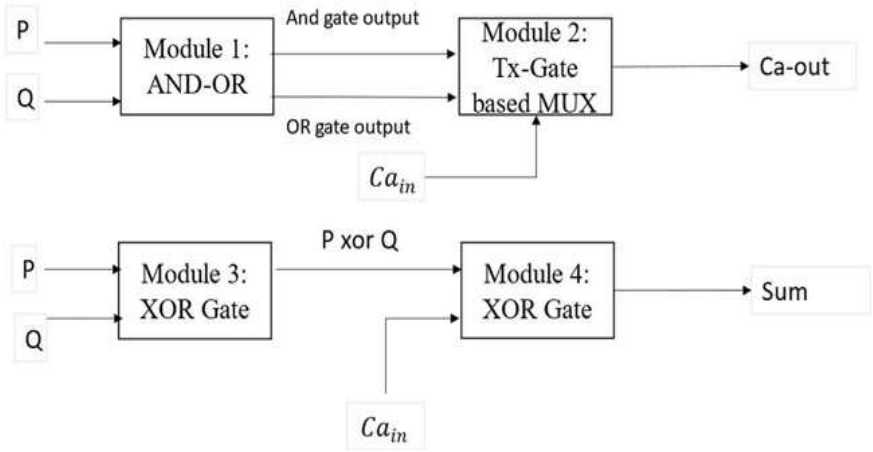

Fig 1: Architecture of 1-bit Hybrid Full Adder

3. TRUNCATED MULTIPLIER ARCHITECTURE

3.1 Truncation by Constant Correction

In the constant-correction method, the least significant product (LSP) columns are removed and replaced by a fixed correction constant. Although this approach achieves substantial hardware reduction, its error grows with operand size, making it unsuitable for precision-sensitive applications.

3.2 Variable Correction Method (VCM)

To improve accuracy, the proposed architecture adopts the variable-correction method. Here, the N−2 least significant partial product columns are discarded. The remaining $(N-1)^{th}$ column is added to the Nth column using hybrid full adders. This offers input-dependent compensation and preserves relevant carry information.

The truncated product is computed as:
$PVCM = trunc(SMSP + SLSPmajor + f(IC) + Kround)$
This approach yields higher accuracy than constant correction while maintaining low hardware complexity.

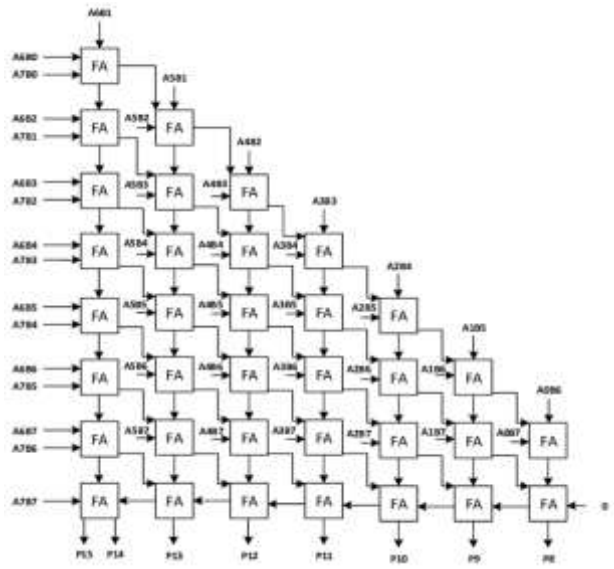

Fig 2: Architecture of Truncated 8x8 Multiplier

4. ARRAY MULTIPIER ARCHITECTURE

An 8 x 8 array multiplier takes two 8-bit input and generates an output of 16-bits. Let the multiplier and multiplicand be x0 - x7 and y0 - y7 and its outputs are S0- S15. The array multiplication process is shown the figure.

							y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
							x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0
							p_{70}	p_{60}	p_{50}	p_{40}	p_{30}	p_{20}	p_{10}	p_{00}
						p_{71}	p_{61}	p_{51}	p_{41}	p_{31}	p_{21}	p_{11}	p_{01}	
					p_{72}	p_{62}	p_{52}	p_{42}	p_{32}	p_{22}	p_{12}	p_{02}		
				p_{73}	p_{63}	p_{53}	p_{43}	p_{33}	p_{23}	p_{13}	p_{03}			
			p_{74}	p_{64}	p_{54}	p_{44}	p_{34}	p_{24}	p_{14}	p_{04}				
		p_{75}	p_{65}	p_{55}	p_{45}	p_{35}	p_{25}	p_{15}	p_{05}					
	p_{76}	p_{66}	p_{56}	p_{46}	p_{36}	p_{26}	p_{16}	p_{06}						
p_{77}	p_{67}	p_{57}	p_{47}	p_{37}	p_{27}	p_{17}	p_{07}							
S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Figure 3. Array Multiplication

In the array multiplier, most of the present inputs for computation of partial sum are depend on the previous output of the adders. Hence, many full adders are idle until the previous output is received from the adders. Hence the delay is more to compute the final product. To reduce the delay of adder, parallel computations of the inputs have to been done in the proposed multiplier. The partial products are added simultaneously and it reduces the number of full adder delays.

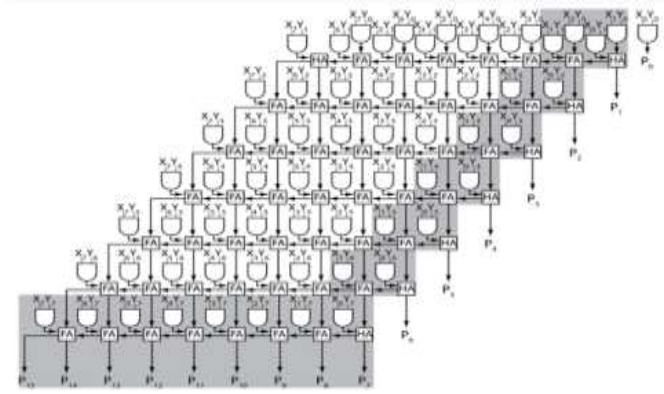

Figure 4: Architecture of 8x8 array multiplier

AND Gates:

Used to compute the partial products by multiplying each bit of the multiplicand with each bit of the multiplier. If the multiplicand is x=x7x6x5x4x3x2x1x0 and the multiplier is y=y7y6y5y4y3y2y1y0, then each partial product is obtained by performing the AND operation

Adders (Half and Full Adders):

The partial products are added using **Half Adders** (HA) and **Full Adders** (FA). The adders sum up the bits at each level to get the final result. For 8-bit numbers, you'll need 8 rows of adders to handle the summation of the shifted partial products.

Bit Shift:

Each row of partial products is shifted to the left (just like decimal multiplication) by one bit for every increase in the position of the multiplier bit.

5. SIMULATION RESULTS

Simulations were carried out using Tanner EDA for 90nm CMOS technologies. The full adders and 8-bit truncated multiplier were evaluated for area, transistor count, and power consumption. Representative waveforms were obtained for 1-bit hybrid full adders, 8×8 Truncated multiplier and 8×8 Array Multiplier.

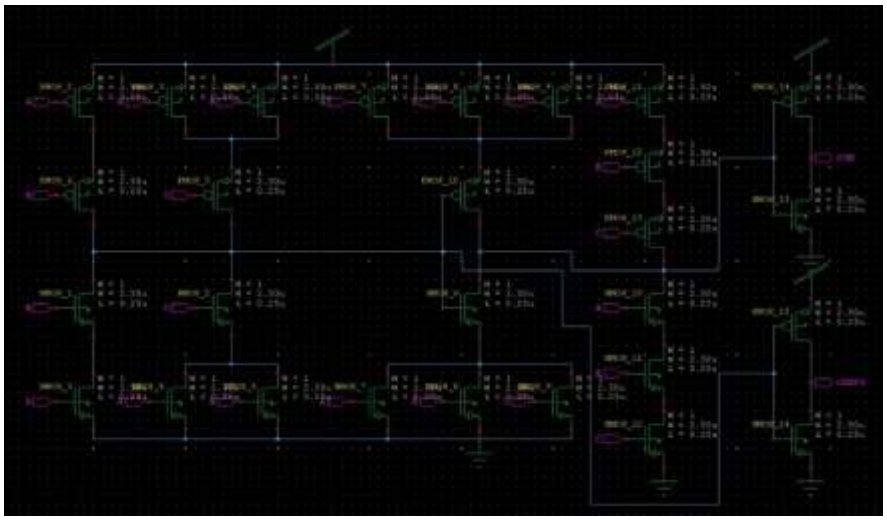

Figure 5: 1 Bit CMOS Full Adder Schematic Diagram

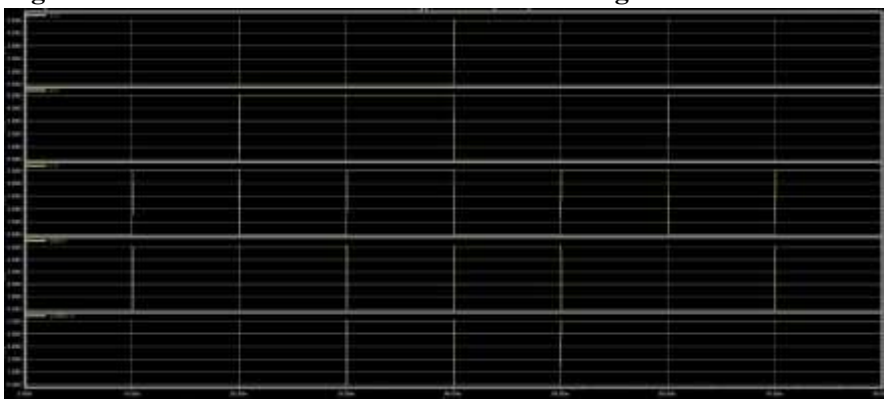

Figure 6: 1 Bit CMOS Full Adder Output Waveform

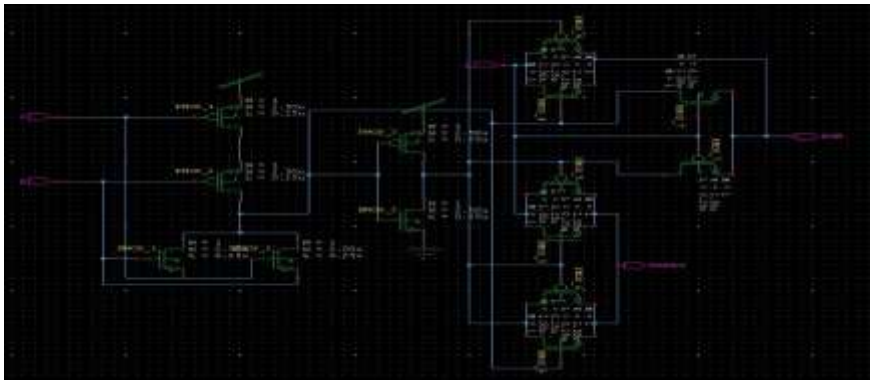

Figure 7: 1 Bit Hybrid Full Adder Schematic Diagram

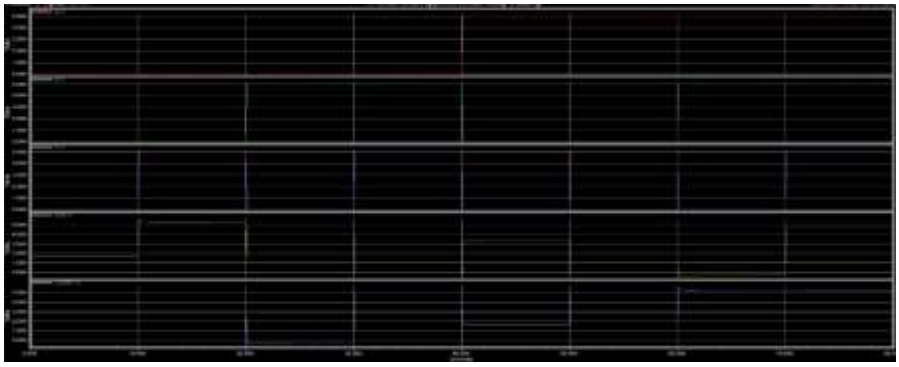

Figure 7: 1 Bit Hybrid Full Adder Output Waveform

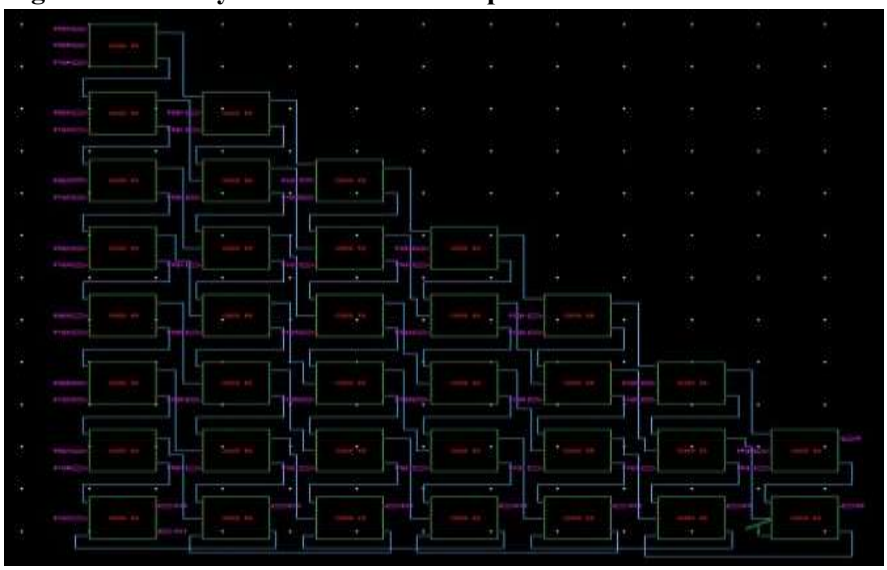

Figure 9: 8x8 Truncated Multiplier Schematic Diagram

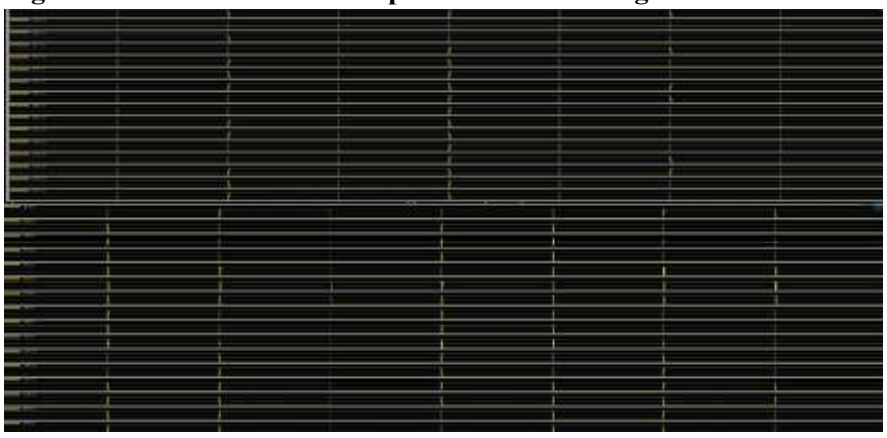

Figure 10: 8x8 Truncated Multiplier Output Waveform

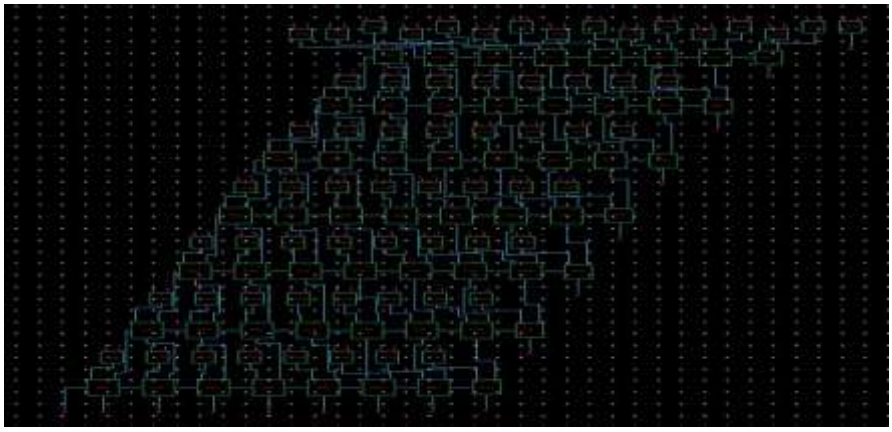

Figure 11: 8x8 Array Multiplier Schematic Diagram

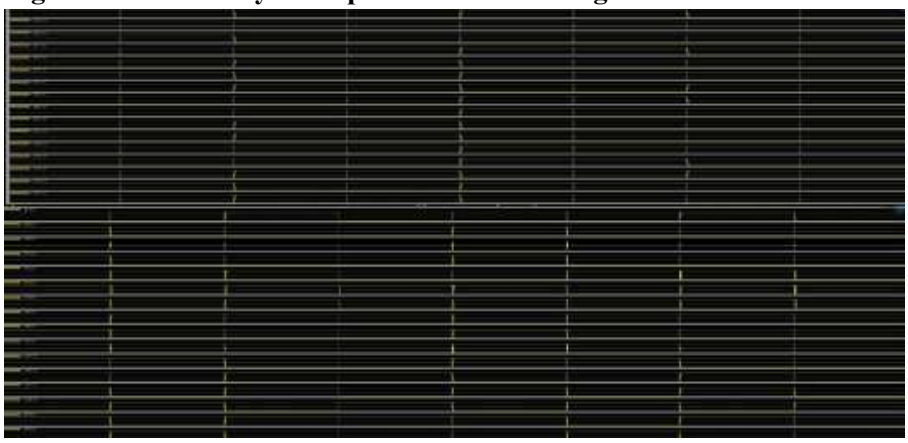

Figure 12: 8x8 Array Multiplier Output Waveform

6.1 Full Adder Comparison

Technology	MOSFET Count	Area (µm²)	Power (µW)
CMOS	28	0.584	1.518
Hybrid	14	0.352	0.640

6.2 8X8 Multiplier Comparison

Multiplier	MOSFET Count	Area (µm²)	Power (µW)
Truncated	654	25.248	28.302
Array	858	34.650	39.888

6.3 Performance Summary

- Area reduction for hybrid 1-bit adder: **27.2%**
- Power reduction for hybrid 1-bit adder: **57%**
- Truncated multiplier area improvement: **27.2%**
- Truncated multiplier power improvement: **9%**

Hybrid logic's reduced internal capacitance and minimized stacking significantly reduce propagation delay and power, validating suitability for DSP accelerators.

7. Conclusion

This paper presented a compact and energy-efficient 8×8 truncated multiplier using hybrid full adders in 16 nm and 22 nm CMOS technology. The hybrid logic approach significantly reduces area and power while maintaining good output drivability and full-swing performance. The variable correction method helps mitigate accuracy loss, making the design suitable for filters, DSP processors, multimedia applications, and embedded AI accelerators.

Future work includes integrating the design into FIR filters, convolution processors, and machine-learning inference units, followed by comparison with approximate multipliers and emerging logic families such as memristor-based arithmetic units.

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