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Area and Power Optimized VLSI Architecture of Approximate Multiplier

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Abstract - When it comes to error-resistant applications, approximation computing offers the ability to reduce design complexity while increasing performance in terms of size, latency, and power efficiency. This brief discusses an innovative design technique for approximating multipliers. When it comes to error-resistant applications, approximation computing offers the ability to reduce design complexity while increasing performance in terms of size, latency, and power efficiency. Within the scope of this short, a unique 4-2 approximate compressor is presented. This compressor is complimentary to existing compressors that have been developed in previous work. Additionally, A proposed multiplier is built using the compressors, a constant approximation, and error correction. The simulation results show that the designed approximation multiplier performs satisfactorily. Within the Xilinx-Vivado environment, the implementation, synthesis, and simulation are carried out and recorded using the verilog HDL programming language.

***Key Words*:** approximate multiplier, exact compressor, approximate compressor and Verilog HDL.

1. INTRODUCTION

Additionally, multipliers play an important role in the management of virtual signs and a variety of projects in the modern day. As time has progressed, numerous experts have endeavored and are currently attempting to design multipliers that provide both of the following plan targets: unnecessary speed, low power utilization, routineness of design, and consequently less area. Alternatively, they may combine these two design goals into a single multiplier, which would make them suitable for a variety of high-speed, low-power, and smaller VLSI executions.

A method for addressing the issue of NP-completeness in the context of an optimization problem is known as an approximation algorithm. Using this method does not ensure that the best answer will be found. The objective of the approximation method is to arrive at the ideal answer in polynomial time, or as near to it as feasible given the available information. Approximation algorithms and heuristic algorithms are the names given to these types of algorithms. To put it simply, we are using approximation approaches in order to boost the speed of the design. In addition, this helps to decrease the amount of space and power that the design requires.

An approximation compressor is the subject of this short study, which demonstrates the following contributions: It has been suggested that a new compressor with a small size, around 5-2, and just four logic gates be developed. The output of the compressor is prone to errors when specific input patterns are used. To mitigate the error likelihood associated with these input patterns, Esposito's compressors are coupled in a novel way. When used together, they lead to significantly better electrical performance and fewer mistakes. The proposed compressor serves as the foundation for an approximation multiplier with minimal resource requirements.

2. LITERATURE SURVEY

Writing for the journal “A.G. M. Strollo, E. Napoli, D. De Caro, N. Petra, and G. D. Meo described their findings in "Comparison and Extension of Approximate 4-2 Compressors for Low Power Approximate Multipliers." Recursive multipliers (RMs) are a form of low-power multiplier that provides a number of power-quality configuration choices. The main building blocks of this recursive architecture are 22 multipliers, whereas the majority of cutting-edge approximation recursive systems use 44 building pieces. Because of this, the investigation of the design space for AxRMs that use 2×2 multipliers is still a challenge that is actively being researched. It is necessary to have 2-bit multipliers that are both high-performing and low-area in order to include configurability and flexibility into the design of AxRMs.

Publications by T. Kong and S. Li concern the study and design of approximate 4-2 compressors for high-accuracy multipliers. Applications like as image processing, multimedia, and data recognition are examples of areas that might benefit from the use of approximate multipliers. These applications are error-resistant and have relaxed accuracy limitations. It is possible for such multipliers to achieve a commensurate improvement in electrical performance, even if such multipliers forfeit some precision. An examination of the architectures of compressors that have been suggested in the past is presented in this article in order to analyze the performance and accuracy of these compressors. The purpose

of this article is to provide five high-accuracy approximate 4–2 compressors that have improved delay, area, and power, as well as a superior performance–accuracy tradeoff performance.

3. PROBABILITY-BASED APPROXIMATE MULTIPLIER (EXISTING METHOD)

An approximately 16-bit multiplier is utilised in order to put the hybrid concept that has been outlined into action. The compressors that Esposito developed are utilised by this multiplier on both the first and third tiers. On the second level, two error correcting AND gates are carried out in order to cut down on the error distance without sacrificing an excessive amount of resources. Using the same truncation strategy, many compressors that were provided in and one that is presented in this brief are applied to the unified Dadda structure. This is done for the purpose of using an approximation multiplier with 8 bits. It is important to note that the suggested compressors are the only ones used by suggested. Additionally, the hybrid structure shown in Figure 1 is created and compared to the other structures. The implementation of 16-bit approximate multipliers comprises of six columns of constant approximation and ten columns of approximate compressors. In instance, the authors' intended outcomes are met by including and applying additional error correcting modules to their multipliers.

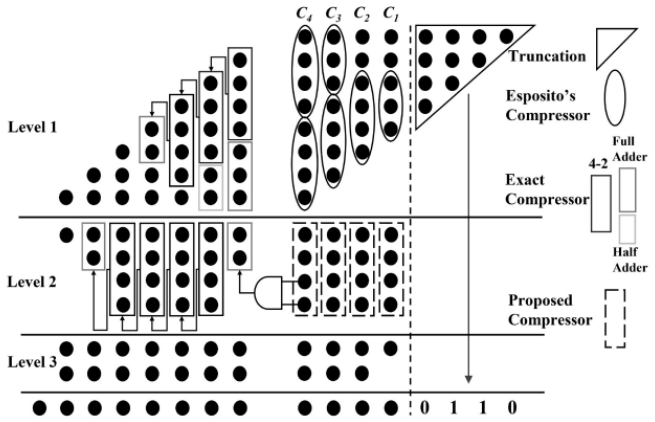

Fig.1. Existing approximate multiplier structure

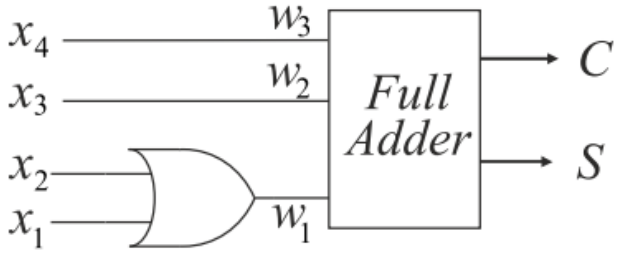

Fig.2. Esposito's compressor

4. APPROXIMATE MULTIPLIER DESIGN USING NOVEL 4:2 COMPRESSORS (PROPOSED METHOD)

Appropriate multipliers are the most effective technique to achieve energy efficiency in computing, particularly in applications that have a natural tolerance for error, according to a growing consensus. This is especially true in applications that have a natural tolerance for error. Nevertheless, the incorporation of accuracy as a crucial design parameter, in addition to performance, area, and power, makes the determination of the approximation multiplier that is the most appropriate rather difficult. According to the findings of this study, there are three primary considerations that should be taken into account while selecting an approximate multipliers circuit: (1) the kind of approximate area efficient compressor and dual quality compressor that were used in the construction of the multiplier, the design of the multiplier, within the main multiplier module, which can be either an array or a tree, as well as the placement of sub-modules that contain approximate and exact multipliers. On the basis of these factors, we conducted an investigation into the design space for the implementation of approximation multipliers at the circuit level. We used circuit level versions of some of the compressors that are being utilized the most often.

Area-Efficient Approximate 4: 2 Compressor

Figure 3 depicts the high-speed area-efficient 4: 2 approximation compressor that has been submitted for consideration. All of the inputs for the compressor are A1, A2, A3, and A4, and the outputs are CARRY and SUM. In order to create SUM, a design technique that is based on multiplexers (MUX) is used. When the MUX is on, the choose line is the output of the XOR gate. The selection of (A3A4) occurs when the choose line is high, while the selection of (A3 + A4) occurs when the select line is low. The suggested 4:2 compressor could be able to use an OR gate to decrease carry generation logic. To achieve this, we add an error to the truth table of the exact compressor with an error distance of 1. To implement the SUM and CARRY operations, you can find the corresponding logical formulas below.

$$SUM = (A1 \oplus A2)\, A3A4 + (A1 \oplus A2)\,(A3 + A4) \quad (1)$$

$$CARRY = A1 + A2 \quad (2)$$

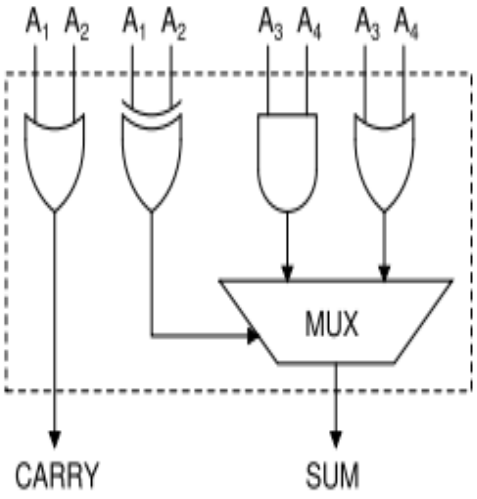

Fig.3. Area- efficient 4:2 compressor.

A_1	A_2	A_3	A_4	$CARRY$	SUM
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	**0**	**1**
0	1	0	0	**1**	**0**
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	**1**	**0**
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	**1**	**1**

Table.1. Truth table for proposed area efficient 4:2 compressor

Here, the design is separated into two parts: one is the Msb component, and the other is the Lsb part. The suggested multiplier architecture was created utilizing an area efficient 4:2 compressor, or gate, and a 4:2 precise compressor. Approximation compressors and gates are being used in the LSB portion of the design. These approximation adders are helping to decrease the amount of space, latency, and power consumption that the system requires. When compared to complete adders, the latency associated with the msb component was reduced because to the utilization of correct compressors throughout the design process. And lastly, the whole design was developed by using dadda structure. These structures minimize the amount of half adder usages, as seen in the image below.

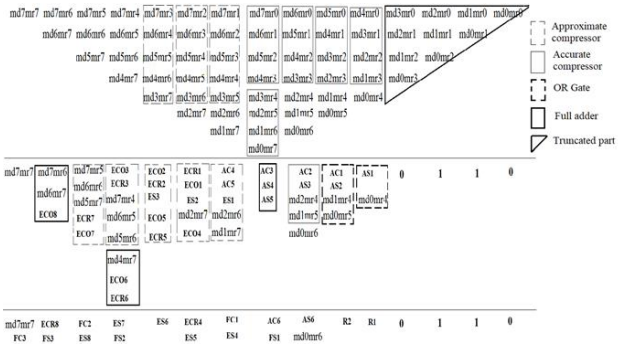

Fig.4. proposed approximate multiplier design

5. RESULTS

RTL Schematic: RTL stands for register transfer level, which is an abbreviation for the register transfer level schematic. This schematic represents the blueprint of the architecture and is utilized to verify that the designed architecture is comparable to the ideal architecture that we are yet to construct. The coding language known as verilog. vhdl is utilized in order to convert the description or summary of the architecture into the working summary. This is accomplished through the utilization of the hdl language. The RTL schematic even includes a description of the internal connection blocks, which allows for more accurate analysis.

The RTL schematic diagram of the intended architecture is depicted in the figure that serves as the representation below.

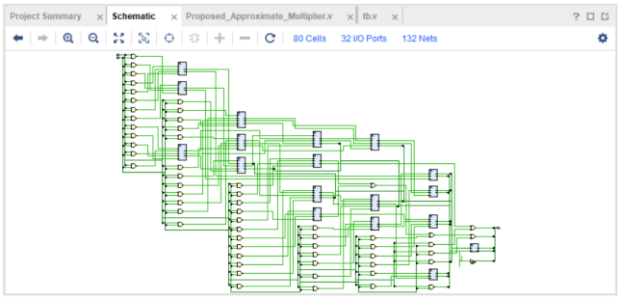

Fig.5. RTL Schematic of the Proposed Design

Technology Schematic: The representation of the architecture is made in the LUT format by the technology schematic. The LUT is considered to be the parameter o area that is utilized in VLSI for the purpose of estimating the architecture design. The LUT is considered to be a square, and the memory allocation of the code is represented in the LUTs that are present in the FPGA.

Fig.6. Technology Schematic of the Proposed Design

Simulation: As opposed to the schematic, which is the verification of the connections and blocks, the simulation is the procedure that is referred to as the final verification in terms of its functioning. During the process of transitioning from the implantation to the simulation on the main screen of the tool, the simulation window is activated. The simulation window is responsible for containing the output in the form of wave shapes. This is where it possesses the versatility of being able to provide a variety of radix number systems.

Fig.7. Simulation wave forms of proposed approximate multiplier

Parameter Comparison: Area, latency, and power are some of the elements that are taken into consideration when it comes to very large-scale integration (VLSI). In light of these criteria, one is able to evaluate one architecture in comparison to another. Verilog is the HDL language that is used here, and the tool Vivado is used to acquire the parameter. Additionally, the consideration of area power and latency is also taken into account.

PARAMETERS	Probability based Approximate multiplier	Proposed Approximate multiplier
No of LUT's	72	54
Power (Watt)	10.551	9.727

Table.2. Parameter Comparison

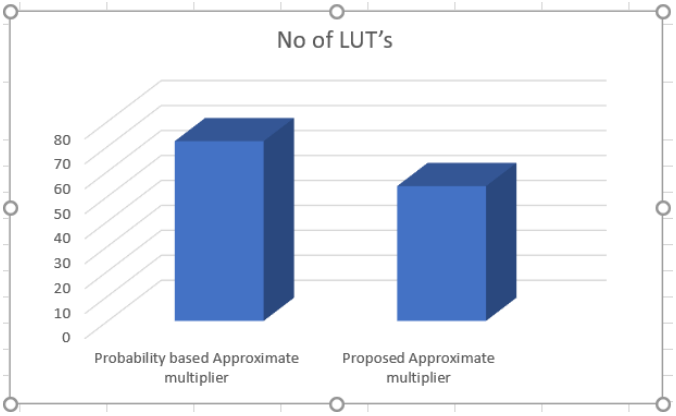

Fig.8. LUT comparison bar graph

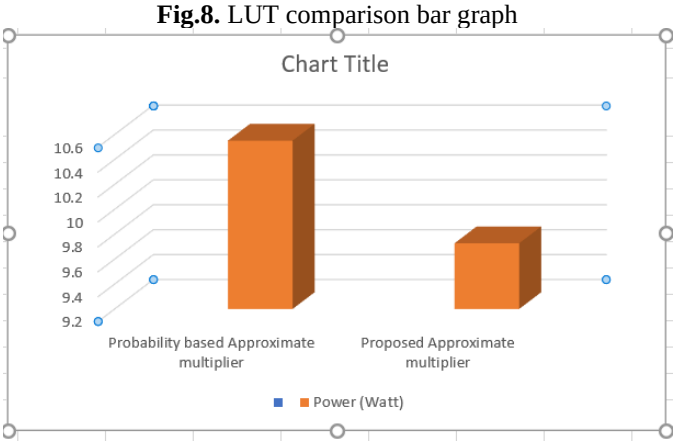

Fig.9. power comparison bar graph

CONCLUSION

A novel method to approximation 4:2 compressor structures is shown in this research, which also includes an approximate multiplier application. In the first place, a low power consumption and area efficient compressor architecture is proposed. This architecture was able to accomplish a significant decrease in area, delay, and power when compared to previous compressor designs that are considered to be state-of-the-art. There is a comparable level of accuracy in the proposed design .Consequently, the design that has been proposed decreases both the area power and the latency. An 8×8 Dadda multiplier function was included into the design in order to allow image processing applications such as image multiplication and smoothing. This structure was created to accommodate these applications. Compared to other multipliers that are presently in use, the hybrid approximation multiplier that has been created allows for a far more attractive compromise between electrical performance and accuracy The proposed approximation multiplier that was provided is also examined for the purpose of sharpening the image. In general, it is rather difficult to create an approximation multiplier that brings about absolute advantage, and the solution that is considered to be optimal is often the one that is most suitable for the application that is being targeted. The approximation multiplier design that we have developed provides a contender that has a competitive error-electrical performance tradeoff.

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